HEC LV Control System

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- Introduction
- HEC LV Power Supply
- HEC LV control system
- HV-LV Interlock System
- HEC LV FSM
- Conclusions

Introduction

- People involved

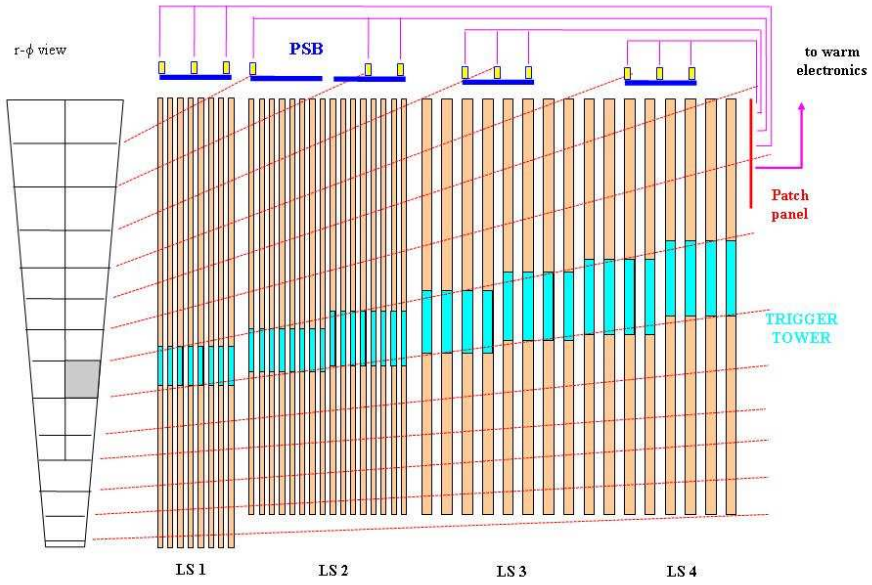
  Ascension Barajas-Velez, Alexander Fischer, Markus Fras, Jörg Habring, Peter Mooshofer, Emanuel Rauter, Teresa Barillari, Peter Schacht, Horst Oberlack, Wolf Cwienk

- In this talk I will try to summarize the status of the work (the hardware and the software, HW/SW) done for the HEC LV power supply

HEC Cold Electronics

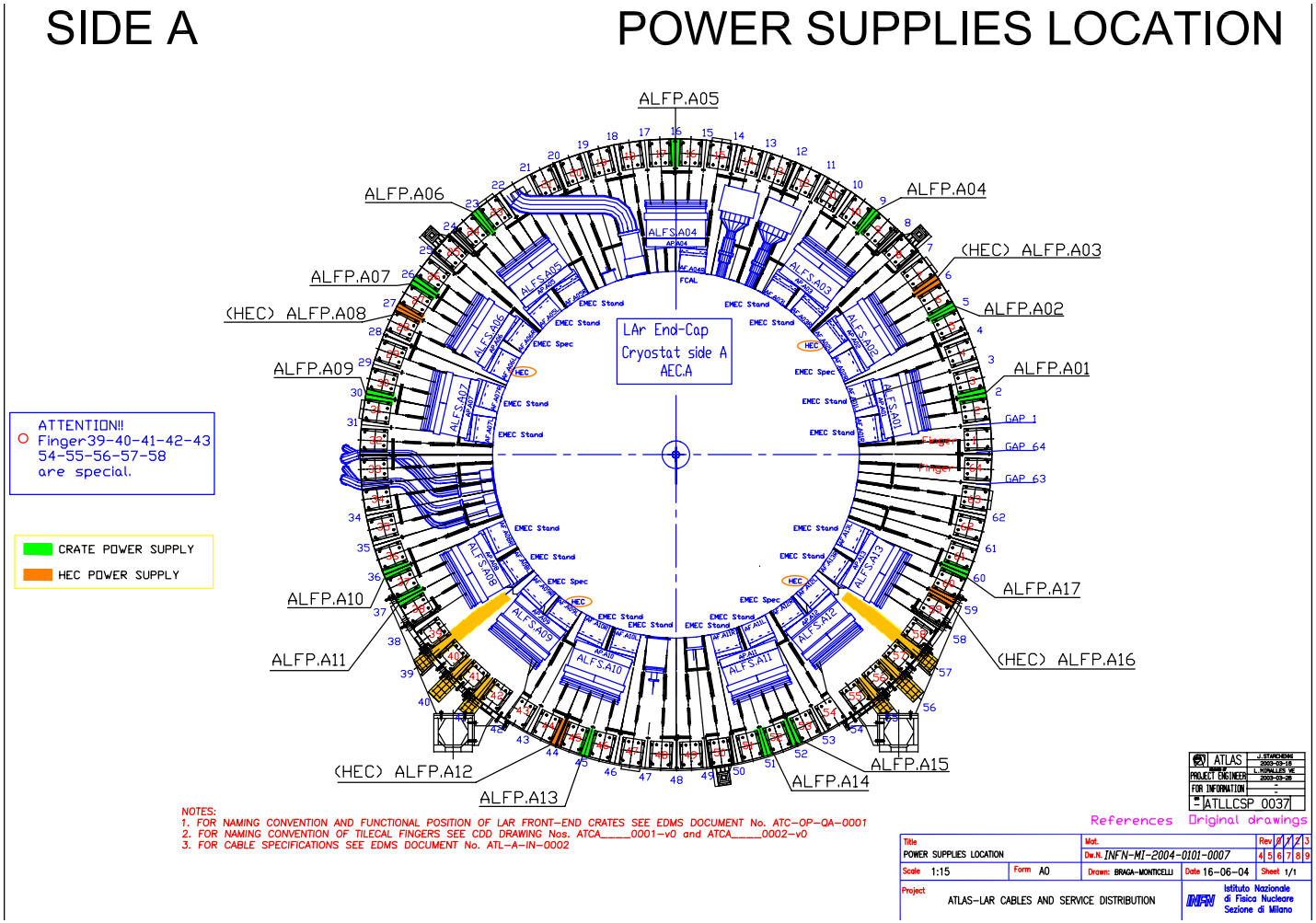
- In the HEC the first summation, and pre-amplification of the signal is done inside the cryostat in the cold, by the “cold electronics”
- This solution allows to achieve an excellent signal-to-noise ratio
- The cold electronics has been studied to work in an hostile environment. It has been developed completely at MPI for the HEC

- The pre-amplifiers are mounted on so called Pre-amplification and Summing Boards (PSB)
- Each ϕ-wedge of the HEC is read out by 5 PSBs



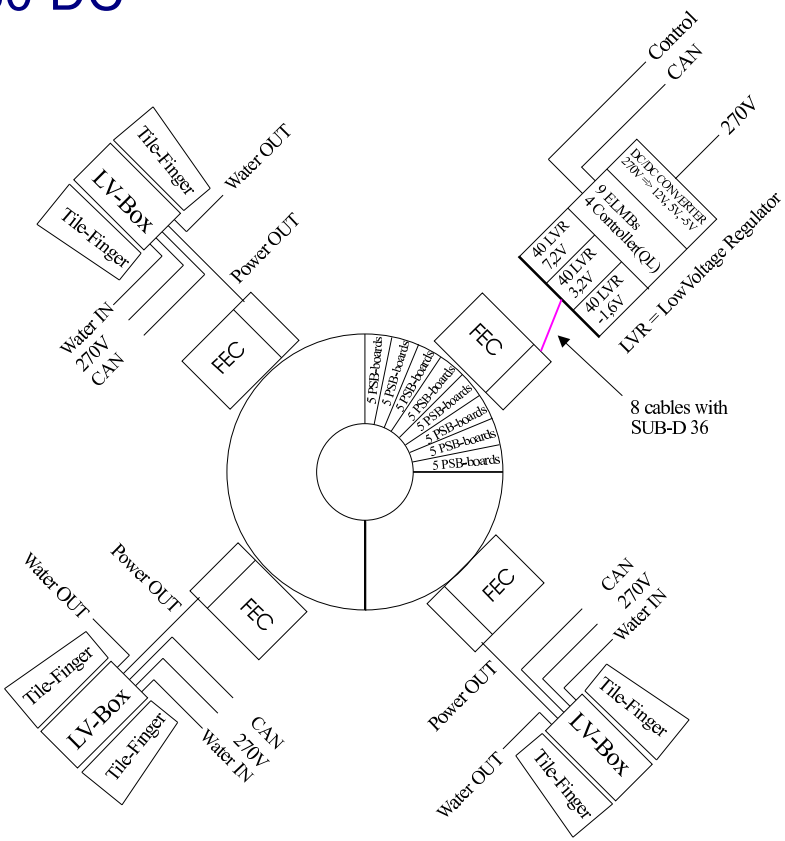
HEC LV Power Supply I

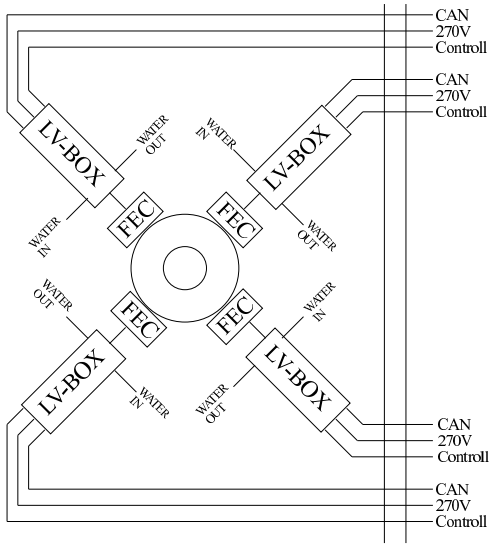
- The power supply system needed for the cold electronics, and for 1 HEC quadrant, is located between the fingers of the TILE calorimeter



HEC LV Power Supply II

- Each power box gets its input voltage (280 V DC, CAN bus, cooling water) from USA15. The input voltage is delivered from a power supply that converts 380 V AC to 280 DC

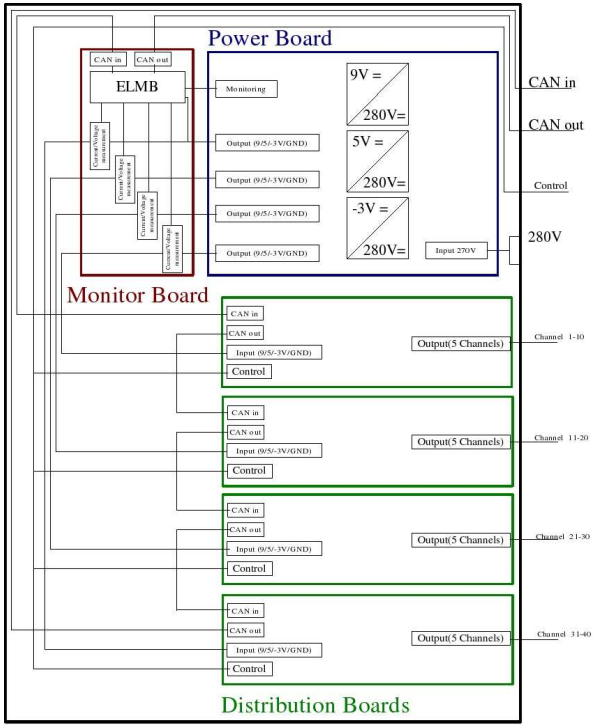


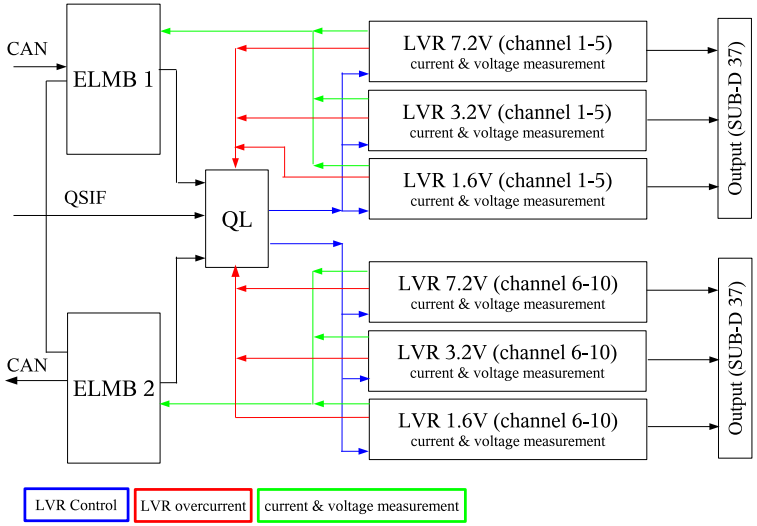


- Each box provides power supply to 40 PSBs, 1 quadrant and 8 $-\phi$ wedges of the HEC
- There is 1 CAN Bus connection for each box (8 CAN Buses for HEC A and HEC C)

LV Power Box

- The LV box consists of 1 power board, 4 distribution boards, and 1 monitor board





- There is one Embedded Local Monitor Board (ELMB), located on each Distribution Board, and 1 ELMB on the Monitor Board. A total of 9 ELMBs for each LV power box
- The ELMB is a general-purpose plug-on I/O module for the monitoring and control of sub-detector front-end equipment. The ELMB project is a collaboration between CERN, NIKHEF and PNPI
- The control and monitoring of the HEC LV, the currents, the voltages and the temperatures is made through the ELMBs

DCS SCADA with PVSS and JCOP Framework

- The HEC LV control system, for the ATLAS DCS, has been implemented with a SCADA (Survey, Control and Data Acquisition) product chosen from an Austrian Company ETM: PVSS
- Our project comply the LHC JCOP (Joint Control Project) Framework
- PVSS, the JCOP Framework, and our project are running on our rack mount PC in USA15 on NICE FC
- Characteristics of a standard ATLAS DCS PC:
  - Motherboard Intel ITSSE7520JR2-ATAD2
  - Xeon 3.0 GHz dual processor,
  - 2 GB memory,
  - $2 * 250$ GB disk shadowed (HW RAID), hot swap
  - 3 PCI slots,
  - Dual power supply hot swap,
  - Height 2U
  - Price about 3.3 kCHF
  - No keyboard, no screen
- The LV control system has been tested and used in the 2004 EMEC-HEC-FCAL test beam, in the 2005 HEC A and HEC C colds tests, in the HEC LV Boxes installation phase, and now in the LArg commissioning phase

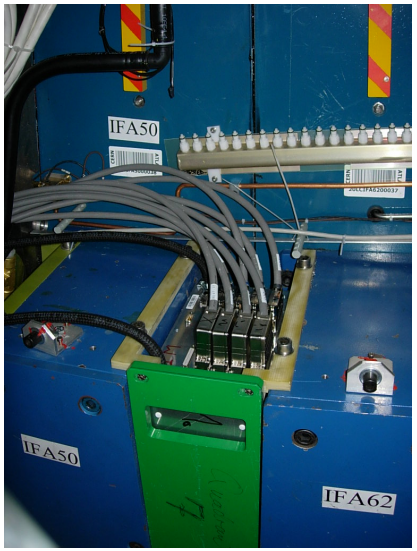
HEC LV control system I

- Our monitor and control software is based on a control script that runs in the background
- This control script check:
  - The state (ON or OFF) and status (OK, Warning, Error, Fatal) of each PSB (an ELMB channel).
  - It monitors the status of the ELMBs (alive, connected, or disconnected)
    - Everytime there is an HW problem, like the ELMB stops working for any reason, there is a cable problem (e.g. the CAN-Bus cable is disconnected), we are able to acknowledge all these problems within a few seconds on our control panels in PVSS
- The HEC LV project monitors and controls
  - The 3 voltages and 3 current of each PSB. We have a total of 320 PSBs in the HEC
  - The DC/DC In/Out voltages and currents
  - The temperatures in the power box
  - etc. etc.
- To protect the cold electronics inside the cryostat we have also developed a SW HV-LV Interlock system
- The HEC LV control system has helped to detect and fix several problems during the different test phases

HEC LV control system II

- The 8 HEC LV power supplies have been installed on the HEC wheels in UX15 at CERN. Our control system running on our rack mount PC in USA15, can now be used to monitor and control the whole HEC LV system

HEC C side in UX15



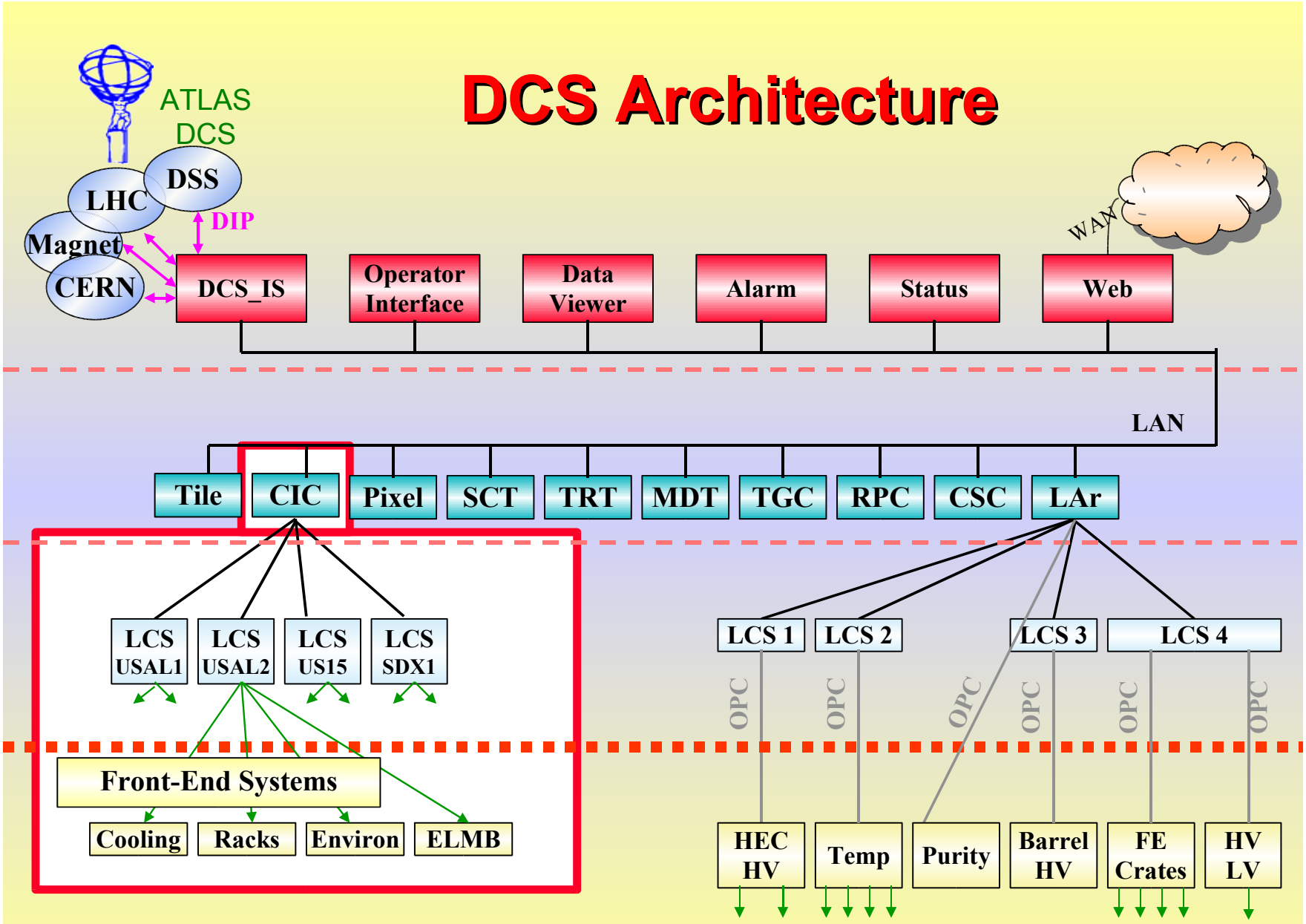
HEC LV Monitor Board

- With the “PVSS” software we can monitor voltages and currents
- Have trendings for voltages, currents, and temperatures plotted over the time
- Because the hardware was ready we could recently also develop the software to control the monitor boards in the power boxes:
  - We can now control all the HEC LV middle voltages ($9\ V$, $5\ V$, and $-3\ V$), the temperature in the power-box, the DC/DC In/Out voltages and etc. etc.
- It has been a big step forward to have the monitor board and the software ready
  - In general for the good “health” of the LV boxes it is very important to monitor the DC/DC In/Out voltage for each monitor board (each power-box). If this voltage is not ok, then also the whole power-box, 1 HEC quadrant, doesn’t work

HEC HV-LV interlock system

- We want to avoid that any of the PSBs in the cryostat get damaged. To minimize this risk it is required that the HEC HV channels stay off if the LV channels are off
- HV-LV channel mapping tables have being built to develop the HV-LV interlock system
  - The HV-LV interlock system has been studied, implemented, and tested so that the HV channels are switched off if some LV channels have problems: set the interlock
    - If one ELMB in the LV system stop working, after about 10 minutes the interlock is set on corresponding HV channels, these HV channels will be automatically switched off
- The HV-LV interlock system has the feature that if a LV channel is ON it will be impossible to switch this channel OFF if the corresponding HV channel is not OFF first. Also if the HV channel is OFF its voltage has to be below 100 *V* before to be able to switch OFF the LV channel
- A watch-dog features to check the network connection between the HV and the LV system has also been added (and not tested) to the software

ATLAS DCS


DCS Architecture
ATLAS DCS
LHC
DSS
DIP
Magnet
CERN
DCS_IS
Operator Interface
Data Viewer
Alarm
Status
Web
WAN
LAN
Tile
CIC
Pixel
SCT
TRT
MDT
TGC
RPC
CSC
LAr
LCS USAL1
LCS USAL2
LCS US15
LCS SDX1
Front-End Systems
Cooling
Racks
Environ
ELMB
LCS 1
LCS 2
LCS 3
LCS 4
OPC
HEC HV
Temp
Purity
Barrel HV
FE Crates
HV LV

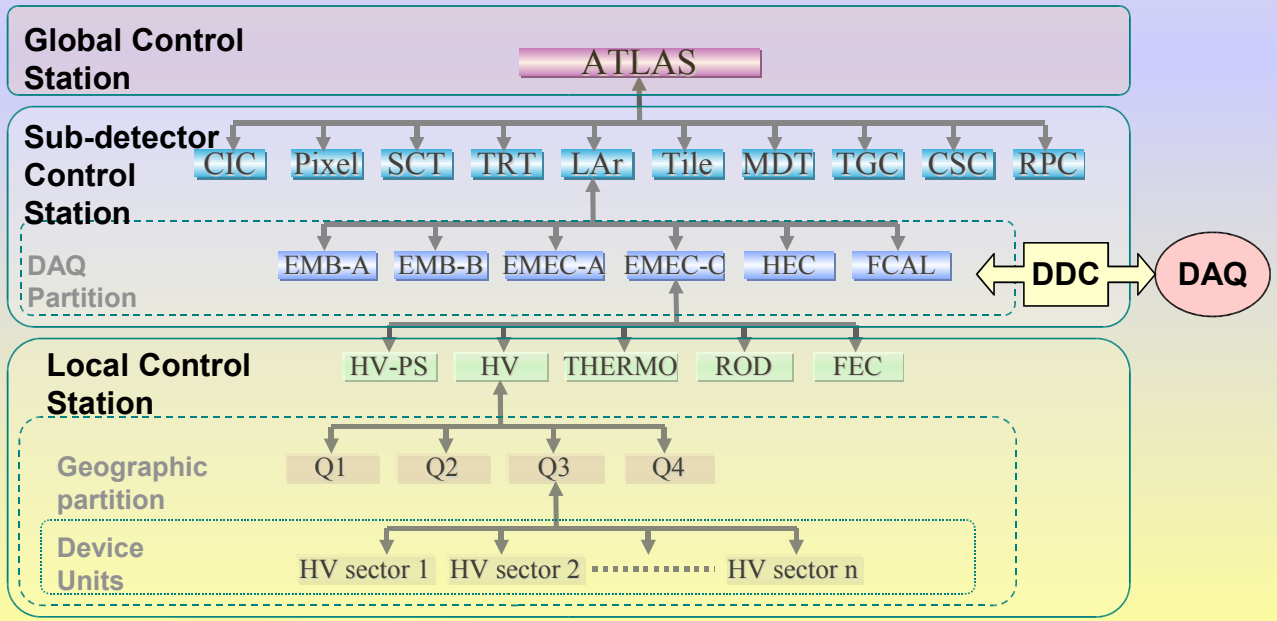
ATLAS FSM

See A.Barriuso talk at the ATLAS DCS Workshop on the 23 March 2006

ATLAS DCS

Operator Interface
Finite State Machine (FSM) Architecture

- **The FSM is the main tool for the implementation of the full control hierarchy in ATLAS**
- **It is envisaged that the shift operators will operate DCS ONLY through the Operator Interface (based on the FSM) and the PVSS alarm screen**



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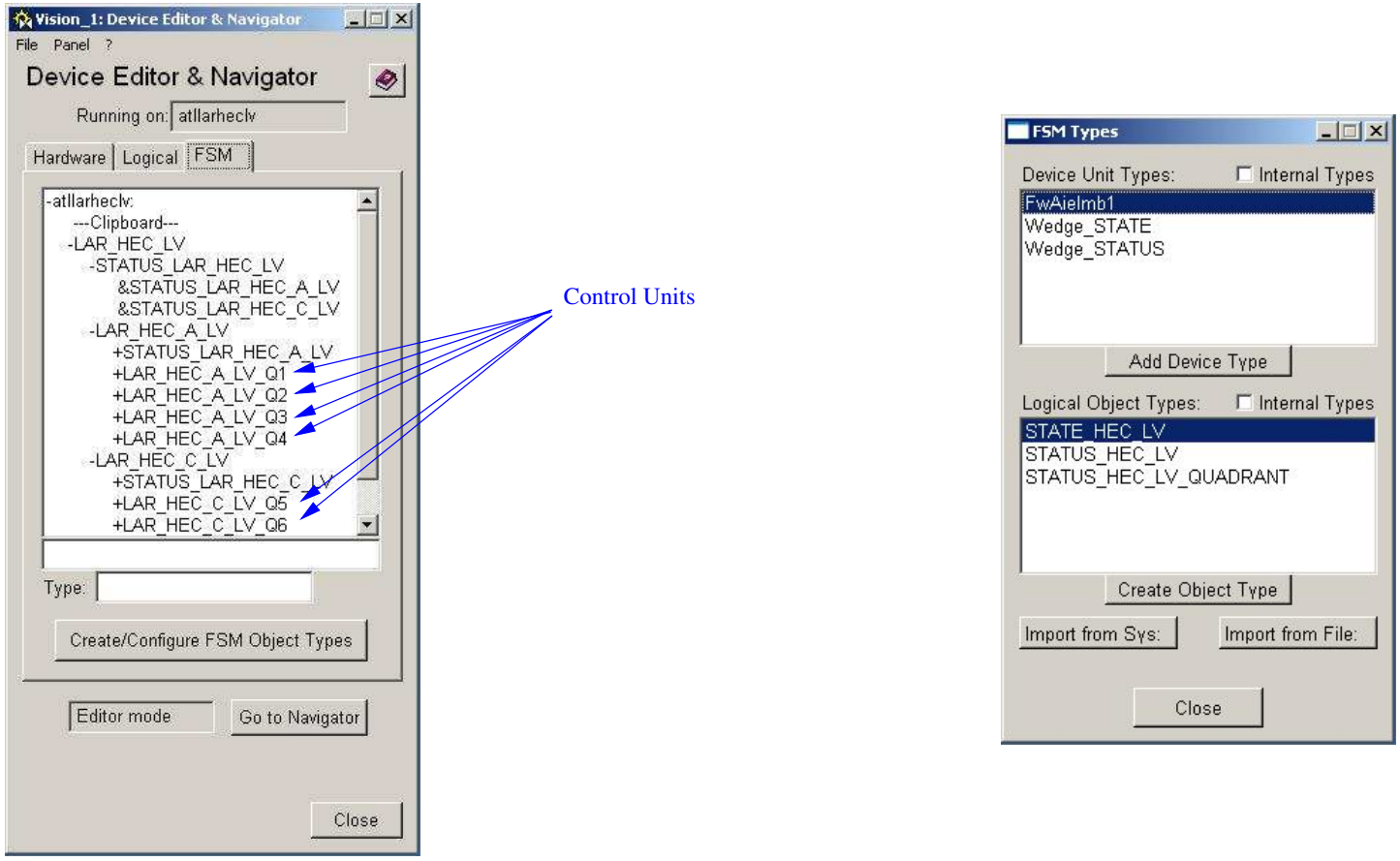
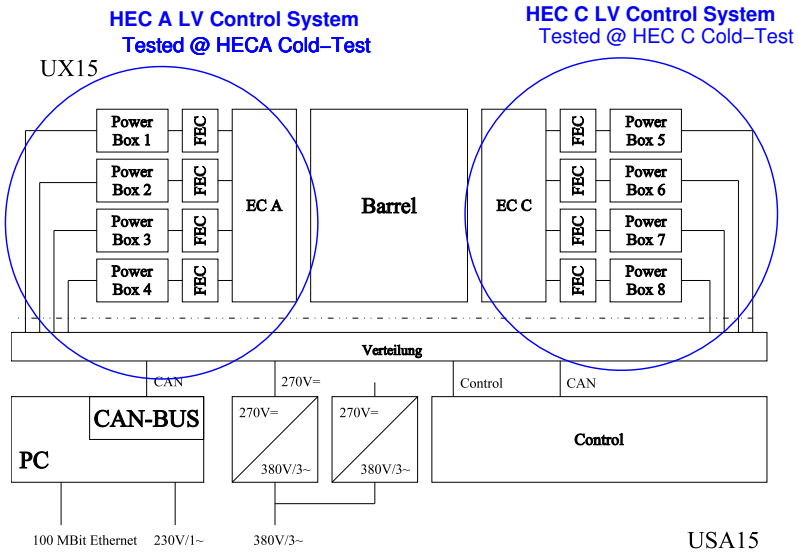
HEC LV FSM for ATLAS DCS

- To fullfil the ATLAS DCS integration needs and rules, we need to develop the HEC LV FSM system and panels:



- At the moment we have some basic scripts for State List: ON, OFF, UNKNOWN and for Status List: OK, WARNING, ALARM. The plan is to have a first prototype of HEC LV FSM running, and then implements better these scripts
- We are starting to build the final panel for the HEC LV FSM

HEC LV control system status ... so far



- What we have done:
  - In the HEC LV system we have a total of 72 ELMBs and 8 CAN-Buses
  - We are running PVSSII on Windows XP and NICEFC
  - Our HEC LV project comply the JCOP Framework
  - We have an HV-LV Interlock system
  - We are using our own warnings and alarms system
  - We are archiving data on ascii files
  - The LV control system has been tested/used in the 2004 *H6* testbeams, in the 2005 HEC A and HEC C cold-tests, and now in the LAr Commissioning phase
- What we need to do:
  - Develop a PVSS and JCOP Framework alert system
  - Connection and use of Configuration Database
  - Connection and use of Condition Database
  - Integration of the HEC LV system in the FSM DCS system

- Higher safety requirements (details to be given by Jörg Habring)
  - Serial interfaces for the control of the power box
  - Redundant system at the ELMB level, for the HEC LV control system

Conclusions

- We have a stable and working LV control system for the 2 HEC wheels
- For the final intergration of the HEC LV in the ATLAS DCS system there is still some work and tests that need to be done:
  - Setup of the Configuration and Condition Databases
  - HEC LV FSM integration into ATLAS DCS
  - ...
  - A final documentation for the operator to help him/her to use the HEC LV control system