DEPFET Mini-matrix readout
Status Report

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1. Current Status

All electronics boards are manufactured, assembled and debugged. Case and connection cables are manufactured. Software for sequencer configuration and basic data analysis was developed. Photos of the hardware are in Figures 1 – 6. First measurements with the DEPFET mini-matrix were done and the system was calibrated.

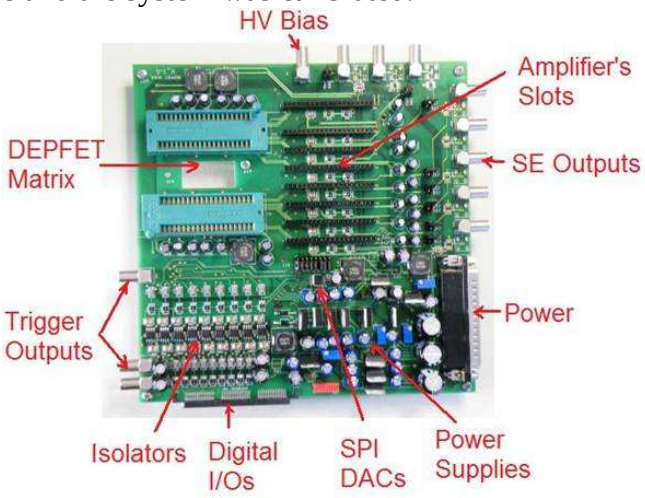

Figure 1 – Motherboard Top View

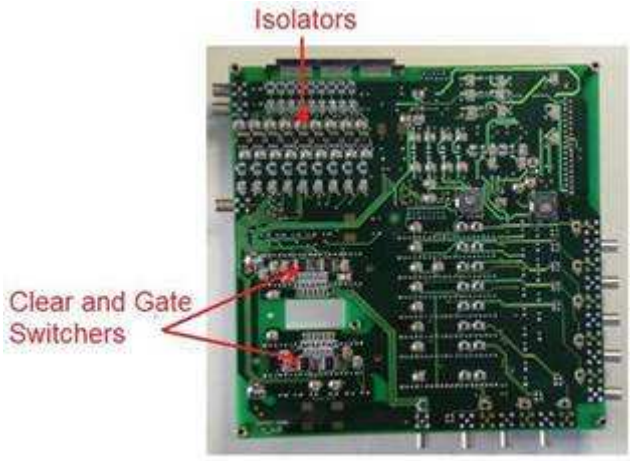

Figure 2 – Motherboard Bottom View

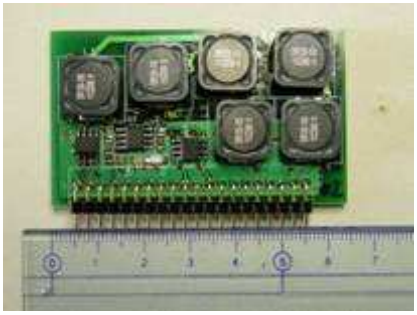

Figure 3 – Current Amplifiers

Figure 4 – X-Board and Mima Case

Figure 5 – X-Board and Mima Case

2. Current readout amplifiers

Figure 6 shows output characteristic of the Amplifier #1. Transimpedance is:

$$R_1 = 65.1 \text{ mV/uA}$$

Figure 7 shows slope of transimpedances of all 8 amplifiers. Offset is added manually.

$$R_2 = 63.6 \text{ mV/uA}$$
$$R_3 = 63.7 \text{ mV/uA}$$
$$R_4 = 64.4 \text{ mV/uA}$$

R_5 = 64.0 mV/uA
R_6 = 64.0 mV/uA
R_7 = 64.3 mV/uA
R_8 = 64.6 mV/uA

Gain variances are software corrected.

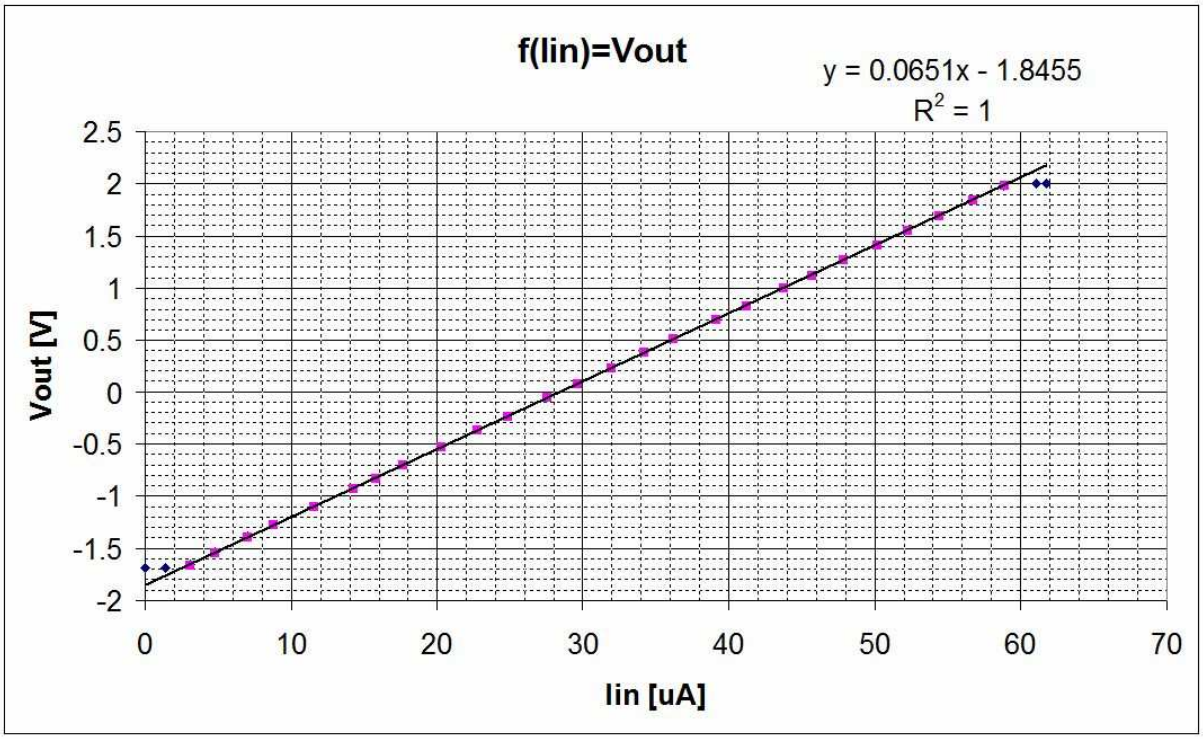

Figure 6 - #1 Amp Output Characteristic

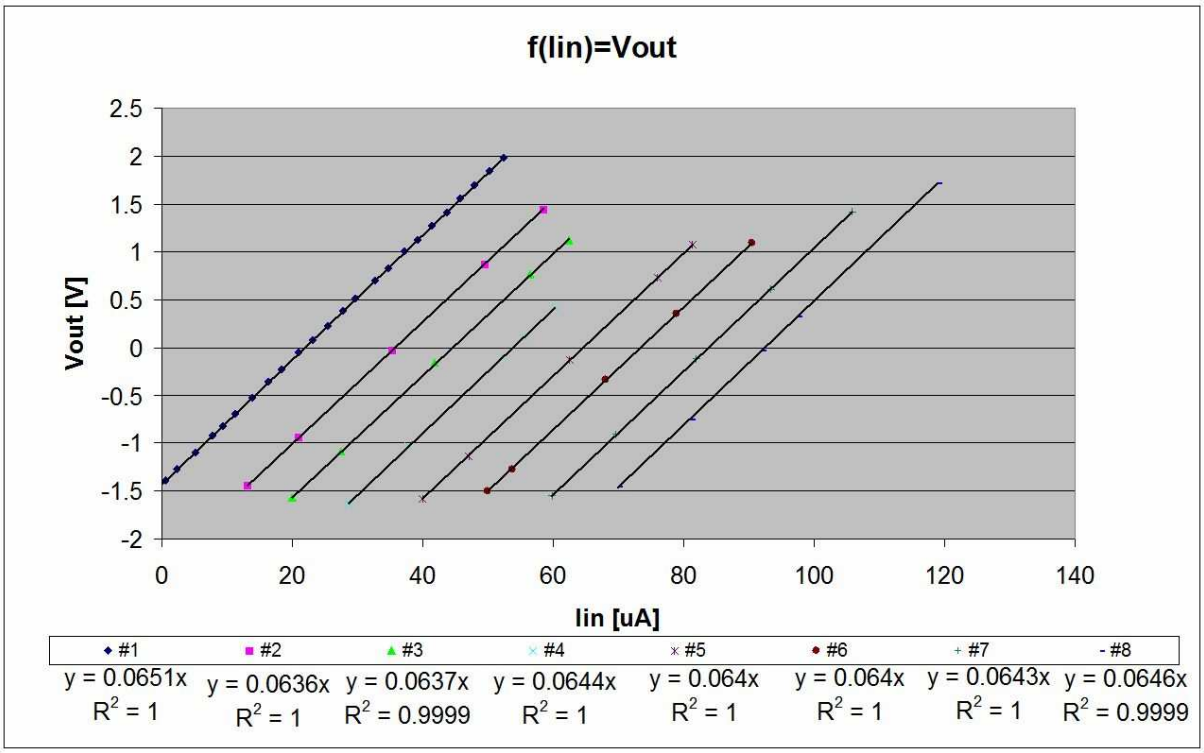

Figure 7 – Slope of Amps Transimpedances

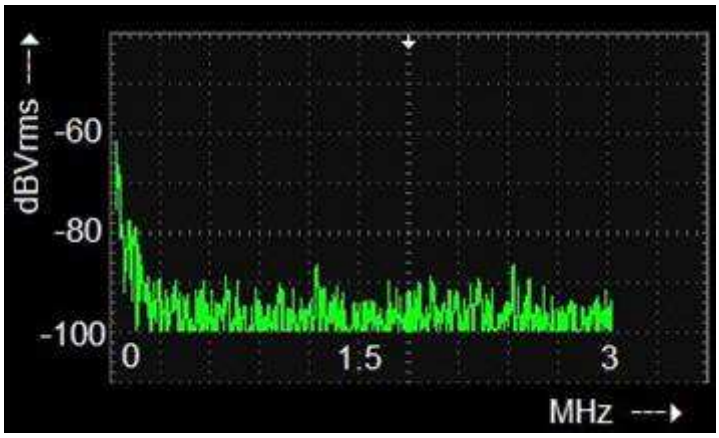

Figure – 8 Amplifier Output-referred Noise Spectrum

Noise of the amplifiers was measured. Figure 8 shows foremost part of the Amplifier Output-referred Noise Spectrum.

- Measured total output-referred noise (10 MHz BW)
  - **1.1 mV** RMS (18nA ENC RMS)
  - 1/f and white components
- Averaging
  - 4-sample: ~ 0.5 mV RMS (8.1 nA ENC RMS)
  - 10-sample: less than 0.2 mV RMS (3.2 nA ENC RMS)

Averaging of 90 samples is used in the DAQ system. The noise contribution of the amplifiers is less 3.6nA what is 1ADU of the 14-bit digitizing system.

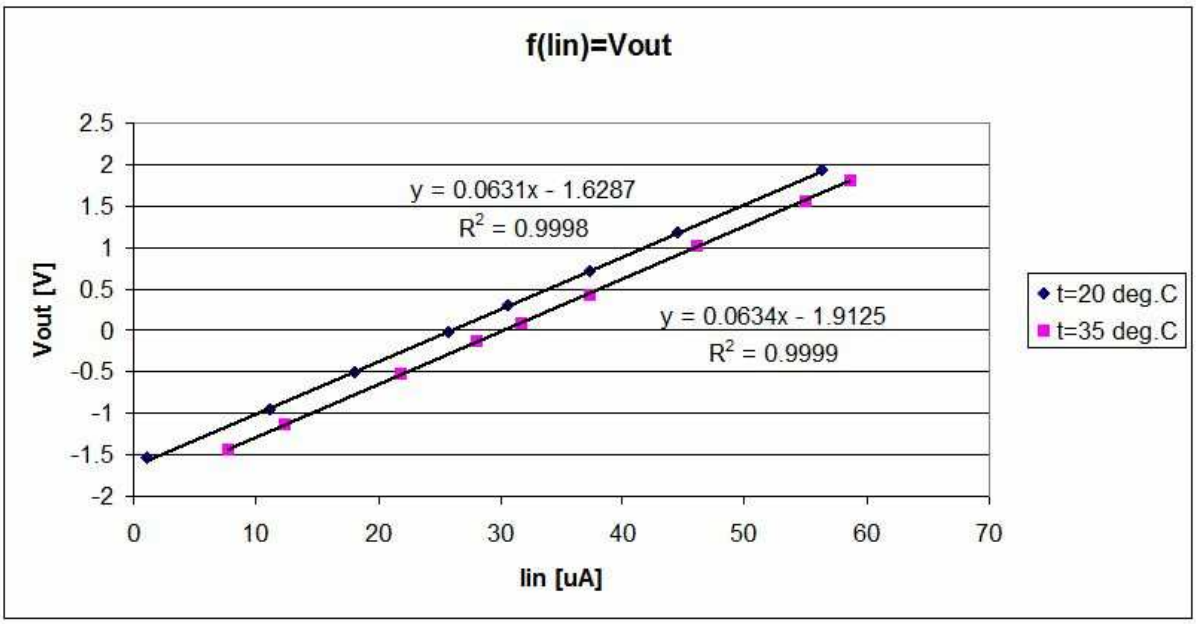

Figure 9 - Thermal Calibration

Thermal calibration for two temperatures was done (Figure 9). Offset drift is:

-18.6 mV/°C

It is not causing any problems because of the differential measurement and wide output range.

Thermal gain change is:

$$20\ uV/uA°C$$

This means that even 15°C change wouldn't cause higher relative error than 0.5 %.

3. Configuration and DAQ Software

Figure 10 shows frame structure. Frame length is approx. 26 us. GATE_ON signals are approx. 100ns overlapping for each matrix lines to make a continuous drain current flow. It prevents saturation of amplifiers.

Figure 10 – Sequencer Configuration Software

In Figure 11 are displayed results of the DAQ monitor. Frame is triggered by one hardware trigger generated by sequencer. Whole frame is recorded and signals for each line are software-triggered. Samples are taken before and after CLEAR signal. They are indicated by blue stripes in the "Full monitor with soft triggers" window in Figure 10. Complete data set can be saved in ASCII format with: ADU, hexadecimal or mV float formats.

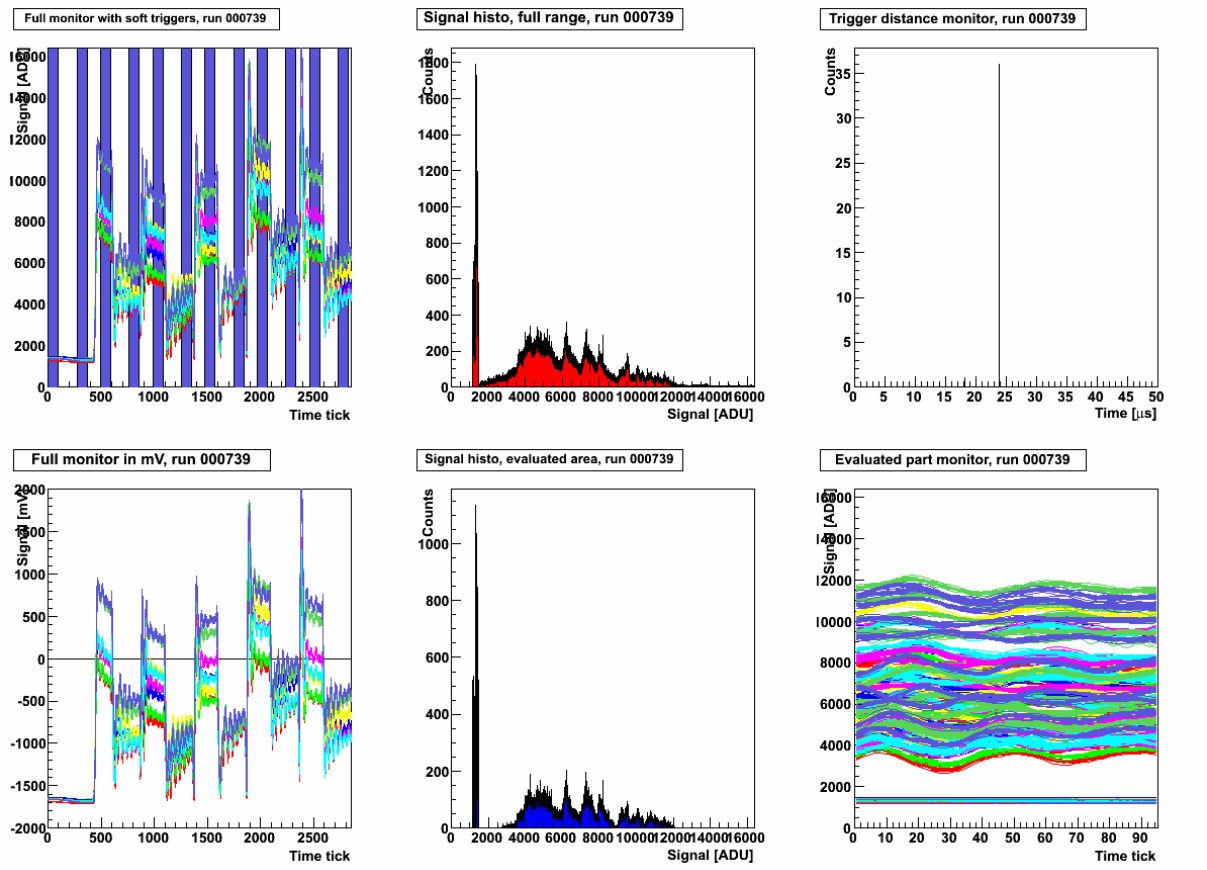

Figure 11 - DAQ Monitor

4. Measurements with the DEPFET Mini-matrix

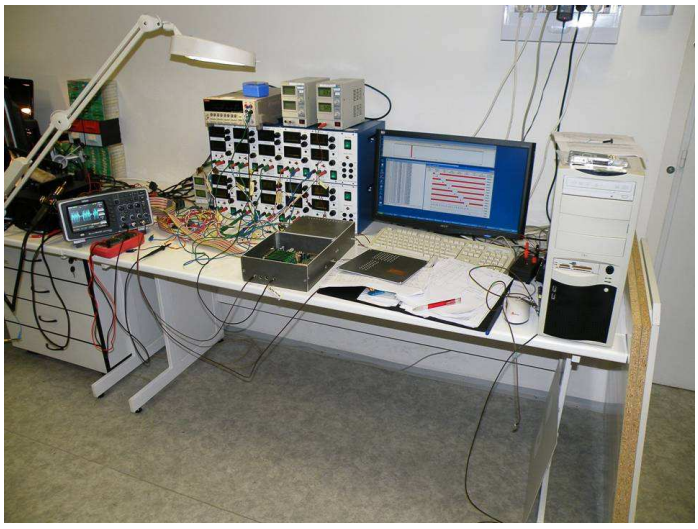

Figure 12 – Lab Measurements

Responses of non-illuminated and light illuminated DEPFET matrix are in Figures 12 and 13. First blue strip indicates previous matrix line readout. Then the next line is witched causing drain current swing. The next blue stripe is evaluated data (90 samples). Average value gives signal before clearing. Then CLEAR signal is applied and in the next blue stripe data is taken. Average value gives signal after clearing.

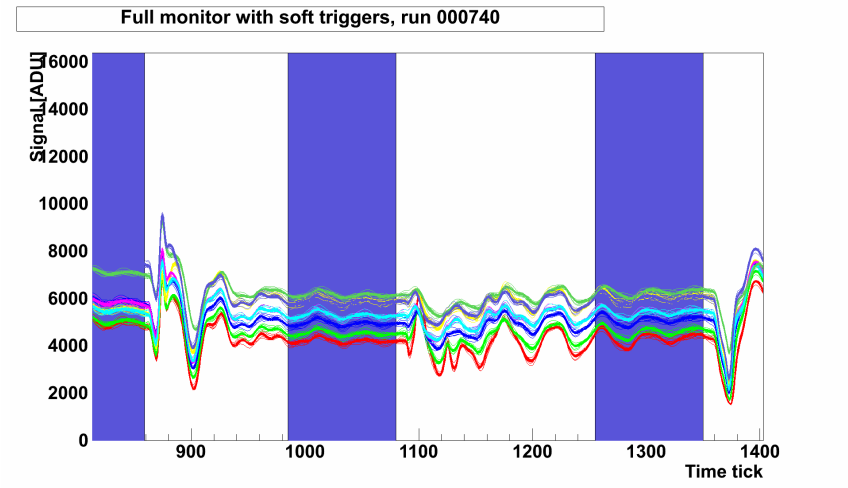

Figure 12 – DEPFET Response without signal

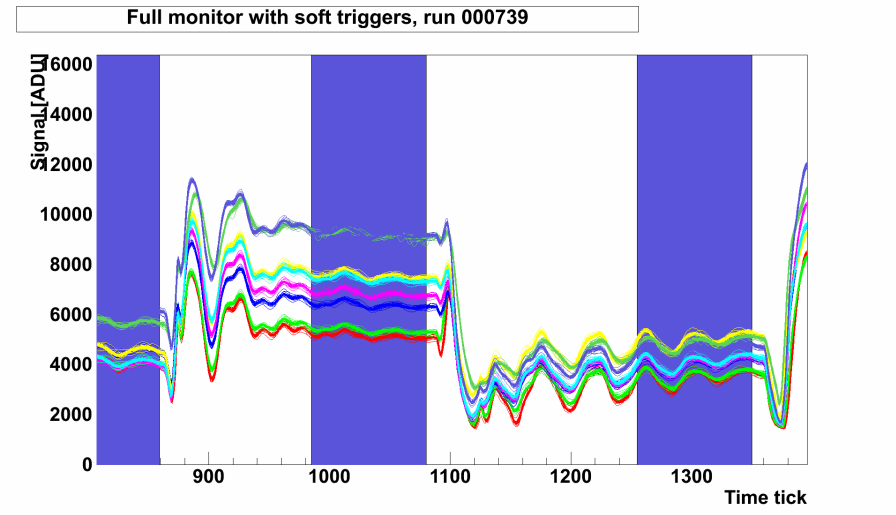

Figure 13 – DEPFET Response of Illuminated matrix

The remaining oscillations in the evaluated areas are caused by standing waves in the relatively long switchers connections. These waves are time constant so evaluation gives good results. The working part of the detector gives results with input-referred current noise about 360 nA. Figure 14 shows illuminated matrix response and noise in ADUs.

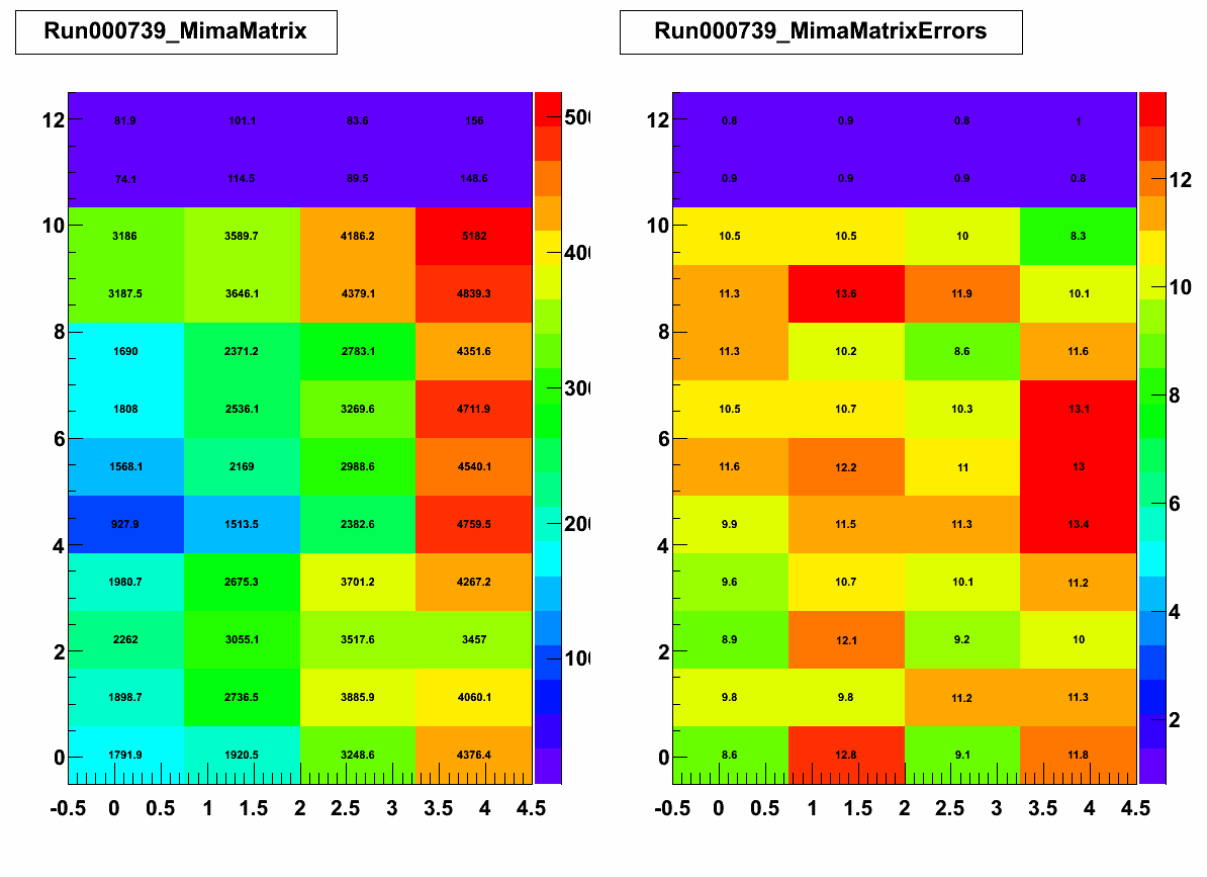

Figure 14 – DEPFET Matrix Response and Noise

5. Used Voltages

Bulk = 10V
Source = 0V
CCG = -0.5V
Drains = -7V
GATE_ON = -4V
GATE_OFF = 6V
CLEAR_LOW = 3V
CLEAR_HIGH = 5.6V (matrix problems!)
HV BIAS = -130V

Matrix was fully depleted a sensitive for light for higher HV bias voltage than -120 V.

6. Mini-matrix sensor problems

1)

The GATE0 terminal seems to be broken through from the beginning. Gate signals flows directly to the drains.
The GATE0 was disabled by isolating the terminal.
The consequences: Two lines are dead. Amplifiers are in saturation during readout of these lines. It's causing a signal distortion. It won't appear with the good matrix.

2)

Applying higher CLEAR_HIGH voltages then 5.6 V is causing breaking through to the output signals and HV BIAS current limitation. It is indicated in the output readouts in Figure 15 by a read arrow.

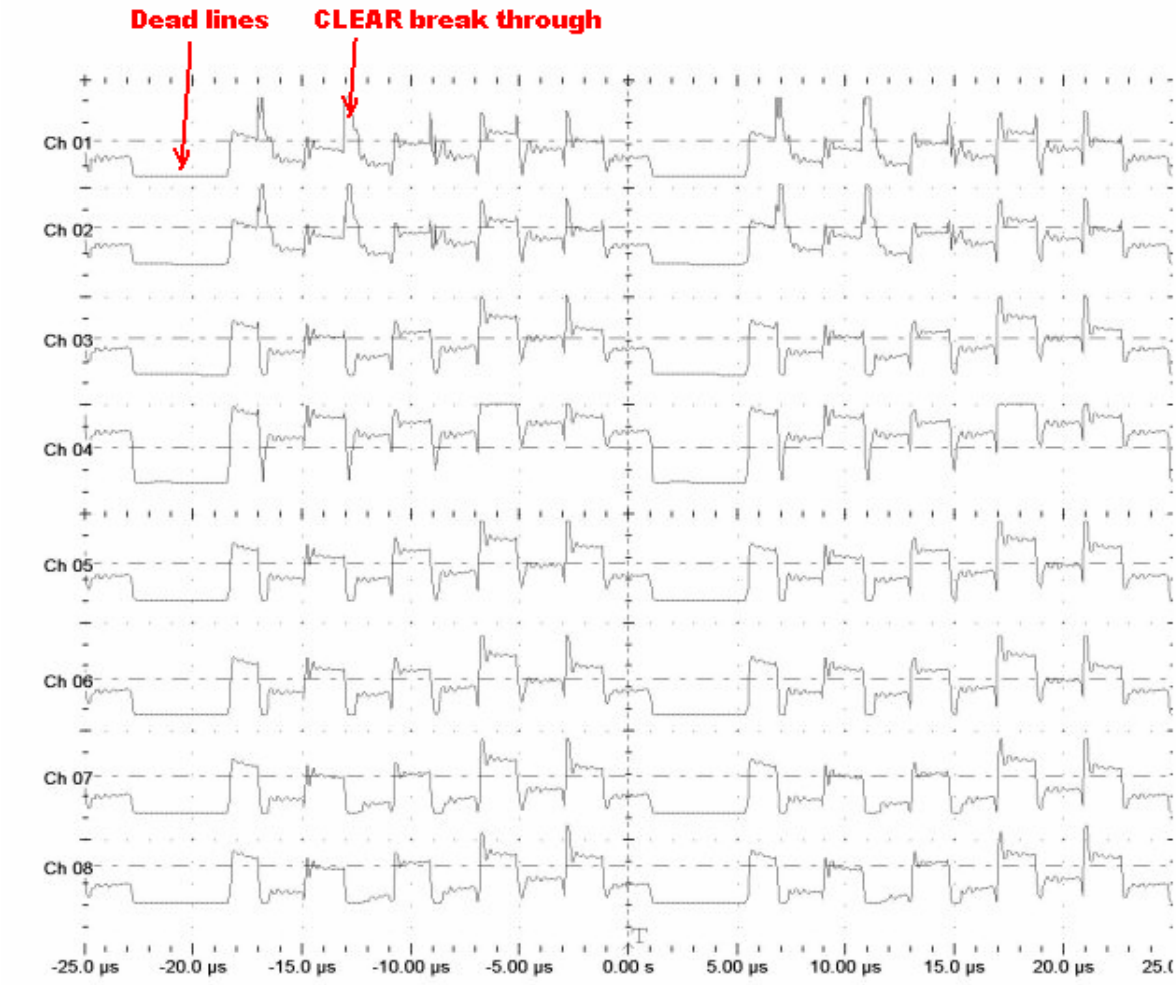

Figure 15 - Matrix Readout Problems

3)

After few-week operations DEPFET burned. The Figure 16 shows photo of the damaged matrix. The CCG metallization was overburned and active structure was locally damaged. It seems to be the same area that wasn't working well. Investigation didn't show error in booting procedure or wrong voltages. It might be caused by manufacturing failure or ESD.

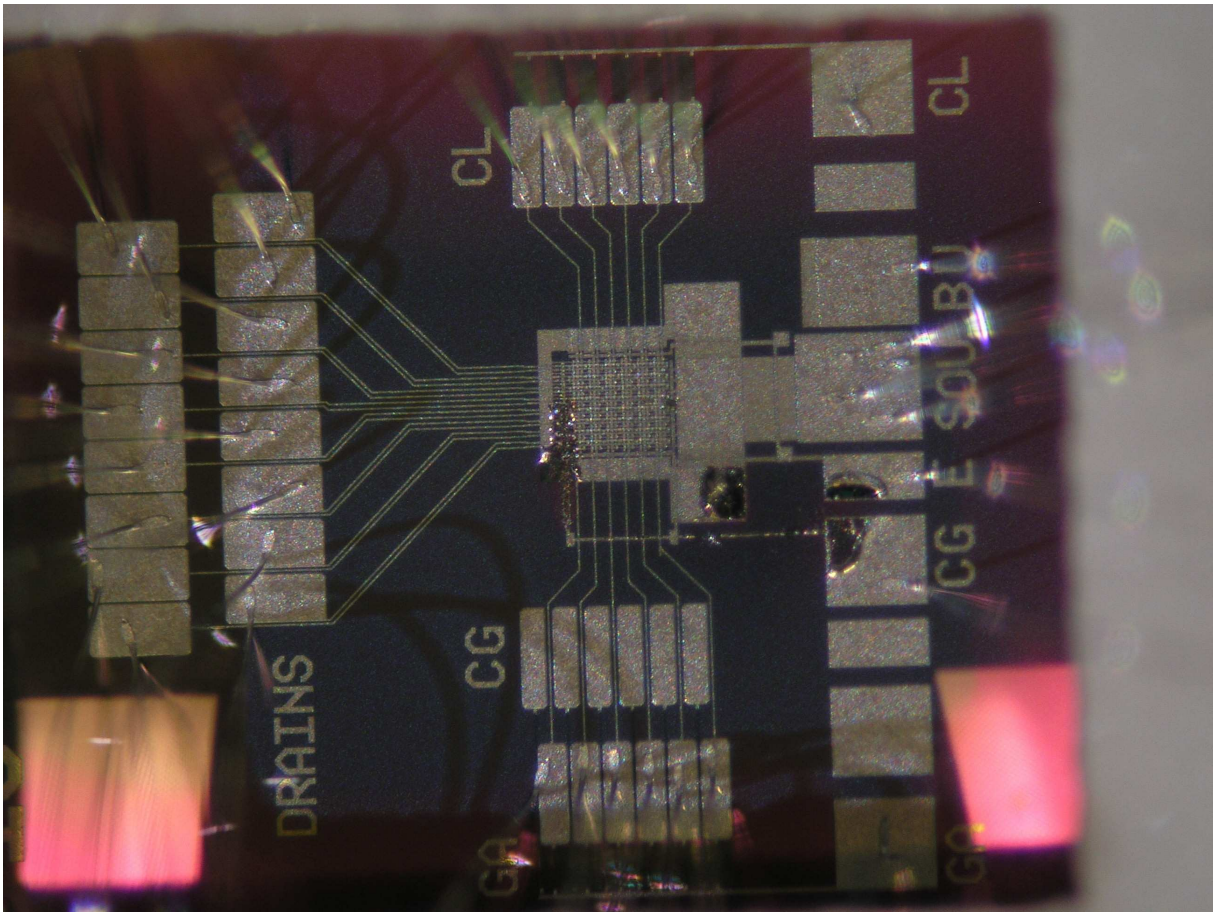

Figure 16 – Photo of the burned matrix

7. Conclusion

The system is functional now. The sequences are reconfigurable and system has relatively low noise about 60e-. The pedestal current is individually adjustable for each channel. A digital FIR filter is still missing in the system. The data acquisition card is able to apply a FIR filter with 20 taps. About 200 taps are required for desired filter response. It has to be applied in the post-analysis. The highest noise contribution is added by switchers and switching processes in the DEPFET structure. Hopefully the noise will be lower in the good matrix. FIR filter also decrease noise. Thermal analysis and calibration need to be done.