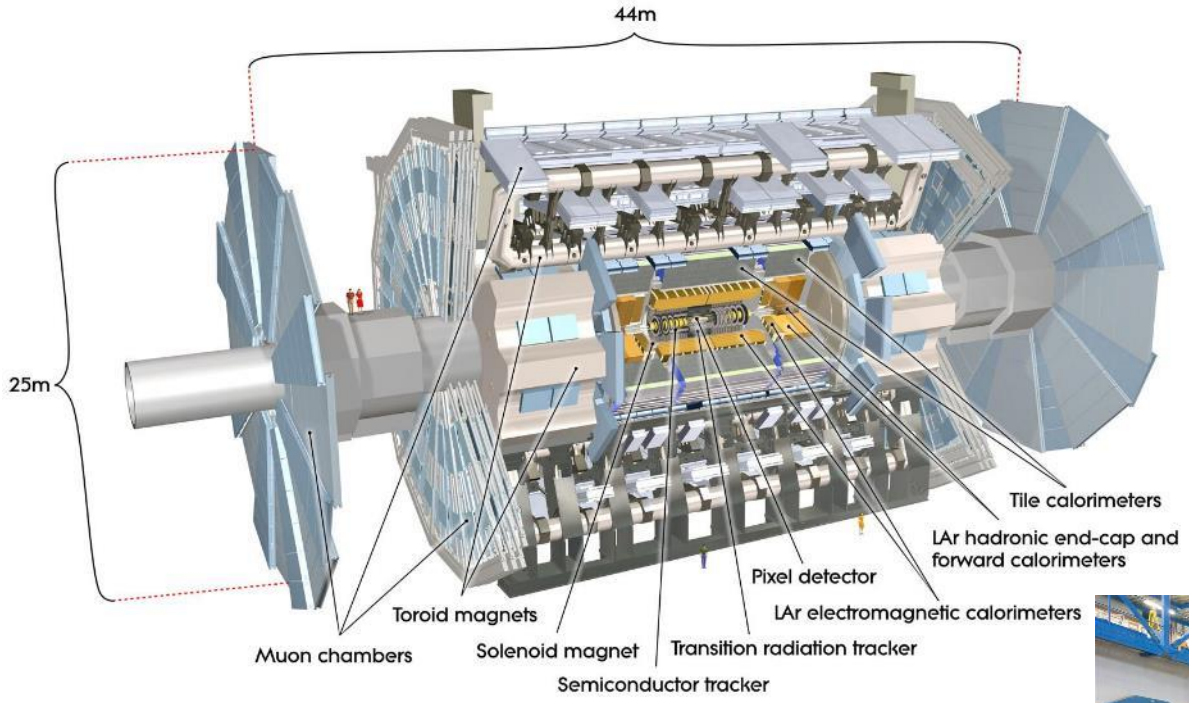
Study on the impact of the new read-out electronics of the ATLAS muon spectrometer at high counting rates

Andreas Grasser, 29 June 2020

Agenda

- Quick overview over the project
- General information about the chip
- About the different testing modes
- Results of the chip tests
- Current problems and further plan

What are we talking about?



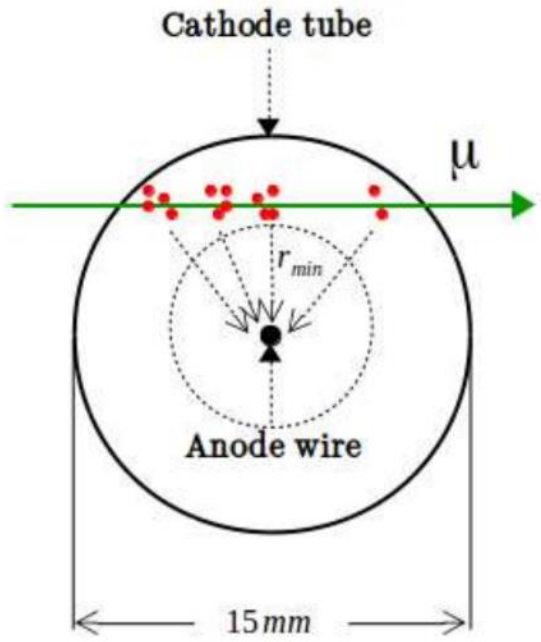
- HL-LHC upgrade
- New sMDT tubes

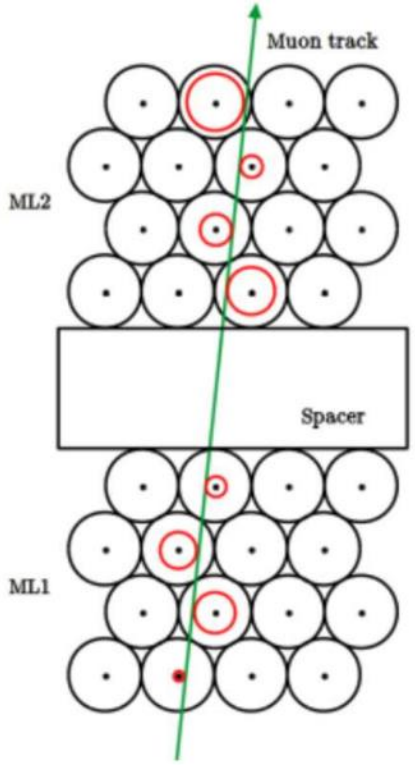
→ new electronics needed

→80k new ASD2 chips

- Part of the level 1 trigger system

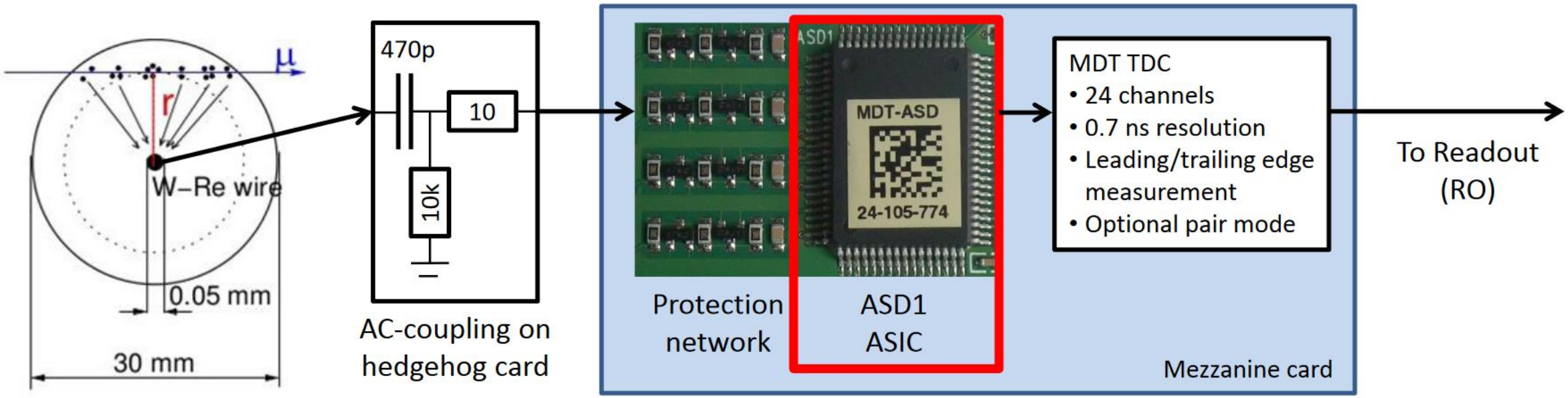
Principle of the drift tubes





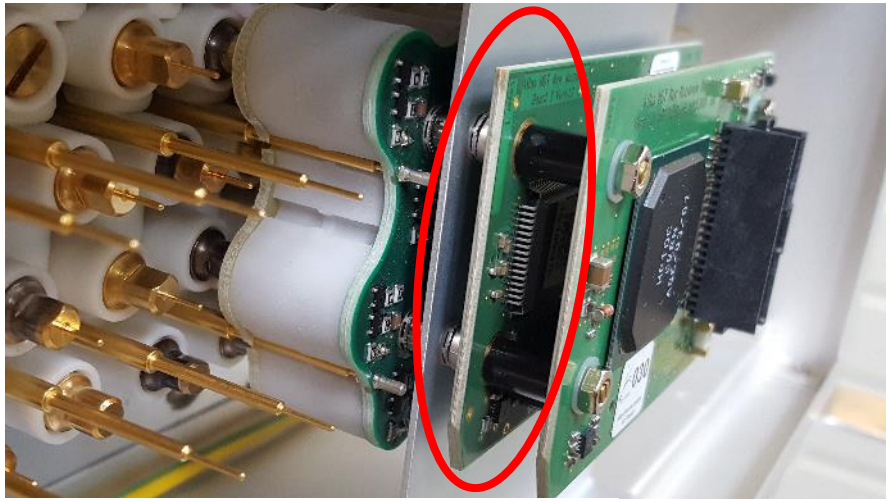
- Tubes are a capacitor with a voltage of nearly 3000V
- Filled with Ar and CO_2
- Myons produce a small charge in the tube
- Charge depends on the myon path

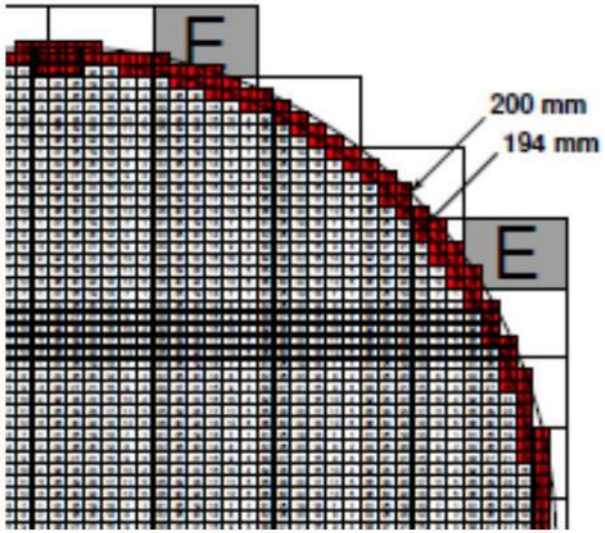
Principle of the drift tubes



Chip is AC-coupled with the tube

General information about the ASD2 chip





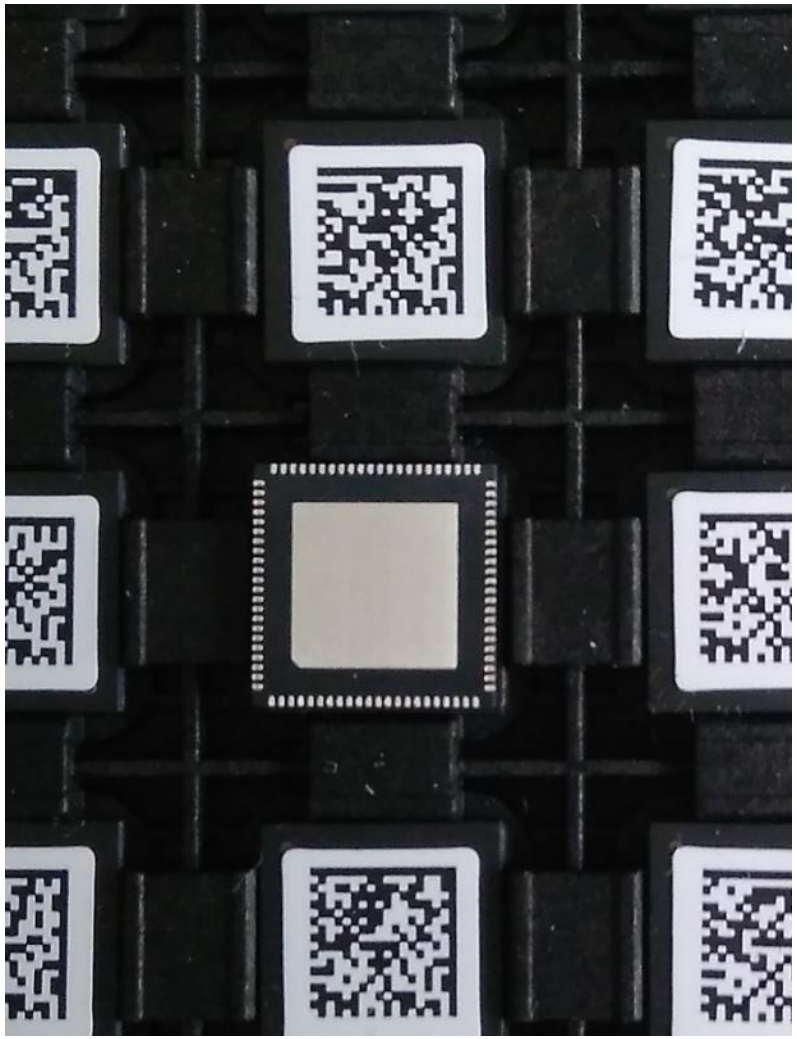
- ASD: Amplifier Shaper Discriminator
- Current chips: 500nm technology
- New design: 130nm

→~3500 chips per wafer

(with 24 wafers: 84000 chips)

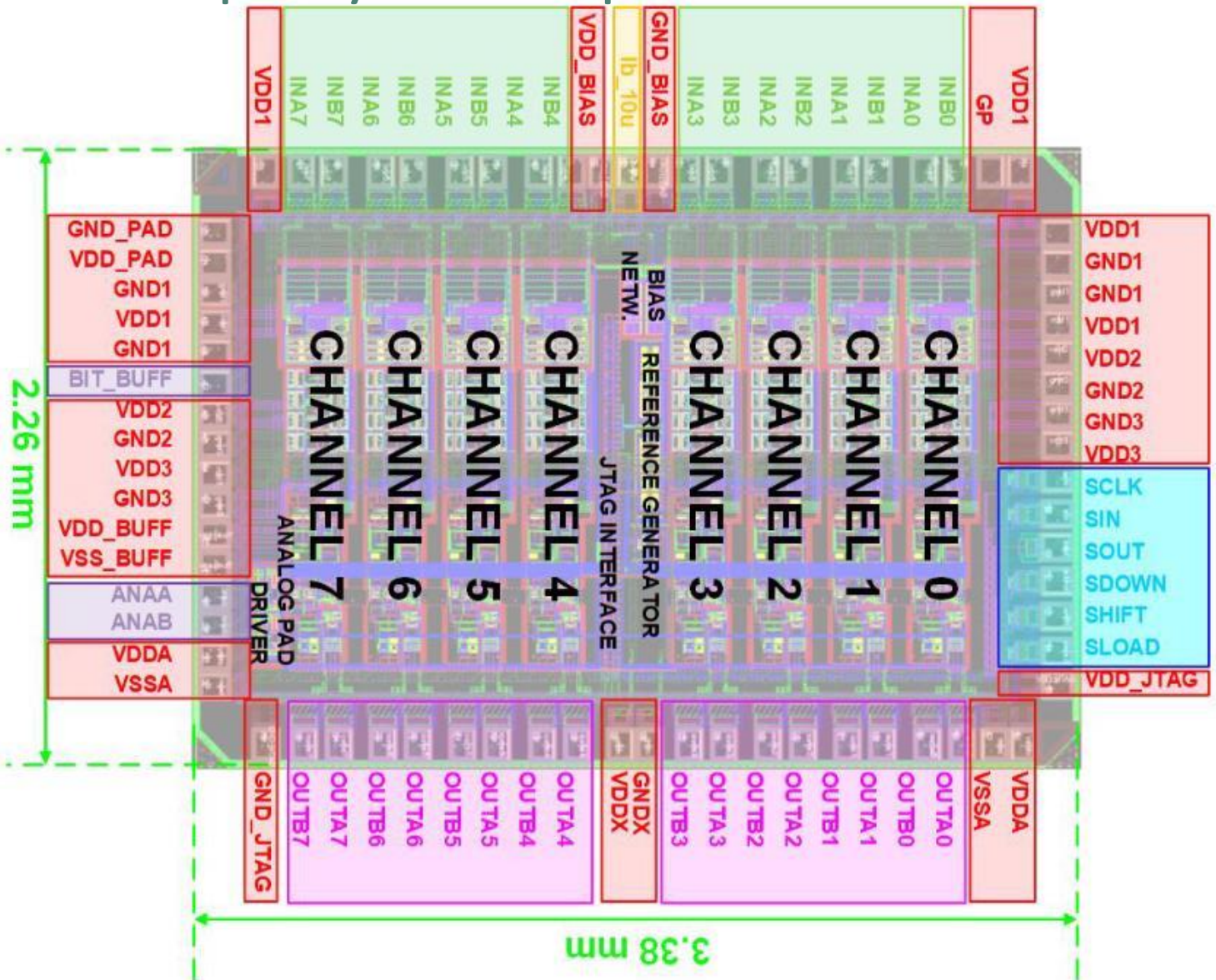
- Chip has two modes: ToT and ADC
- JTAG (Joint Test Action Group) for simple change of operating values

General information about the ASD2 chip



- SMD Chip (QFN: Quad Flat No Leads Package)
- Sticker with an individual ID for simpler testing and managing

Amplify - Shape - Discriminate



DIGITAL I/O PADS	6
POWER SUPPLIES PADS	32
BIAS NETWORK PAD	1
ANALOG INPUT PADS	16
ANALOG OUTPUT PADS	16
BUFFER PADS	3

	74

Amplify - Shape - Discriminate

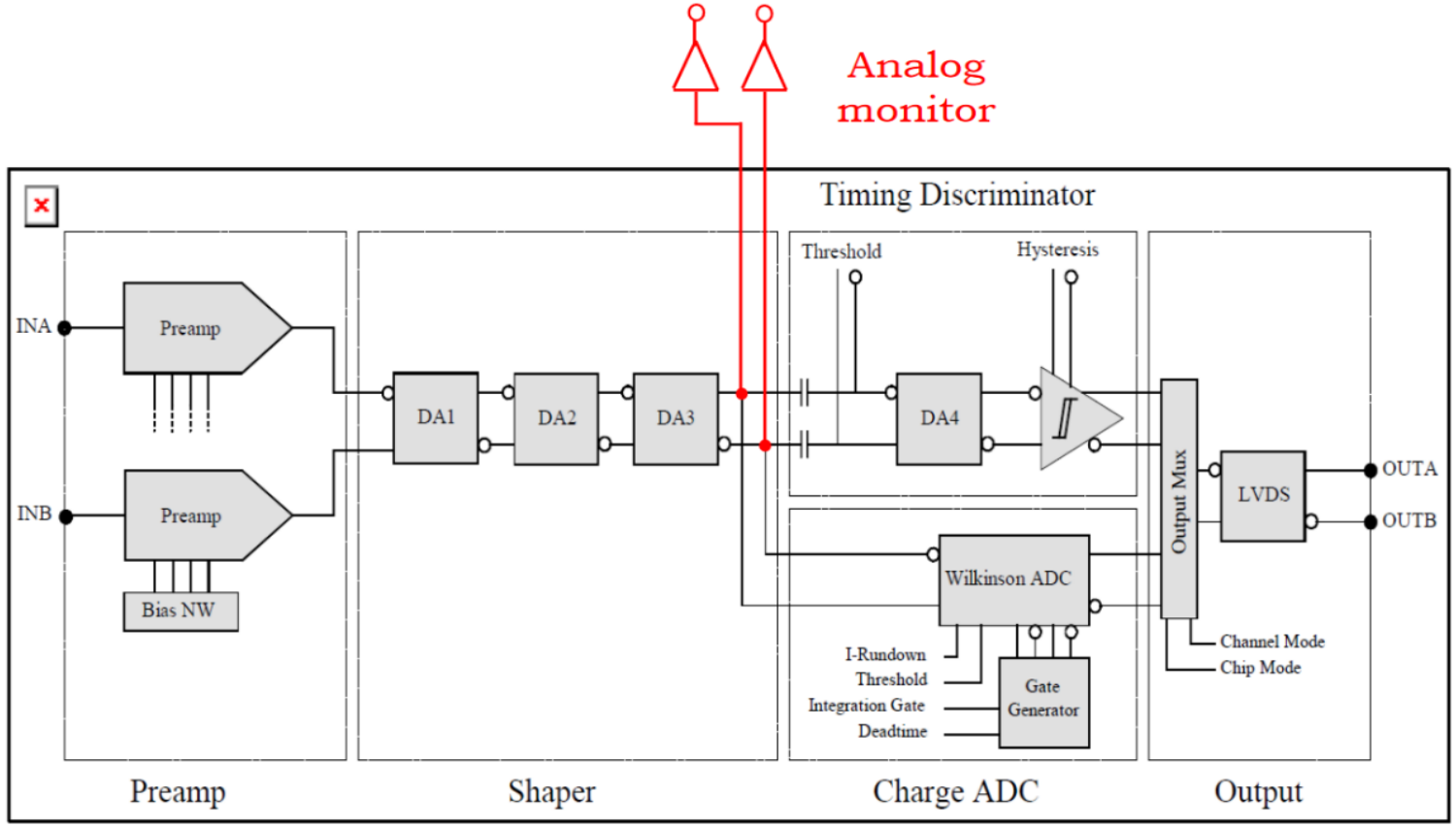
Input Contacts

Amplify

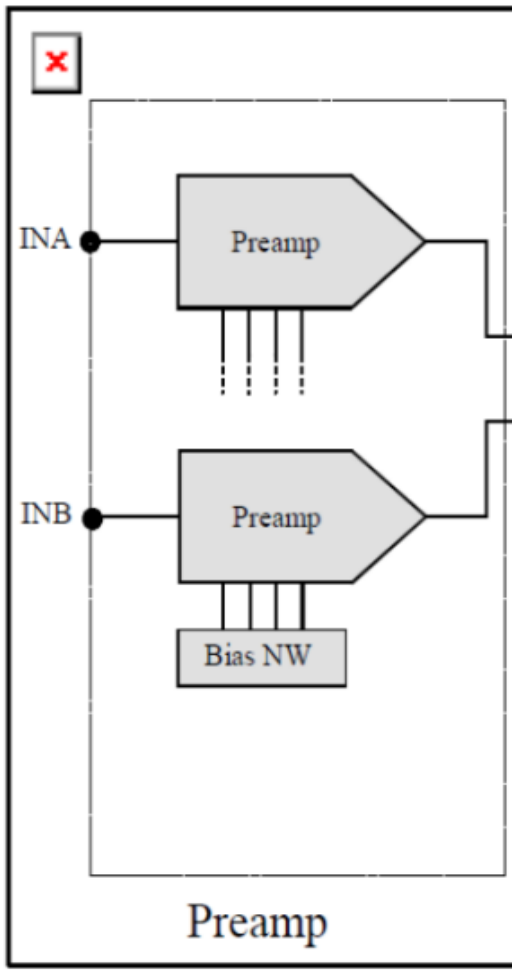
Shape

Discriminate

Output Contacts

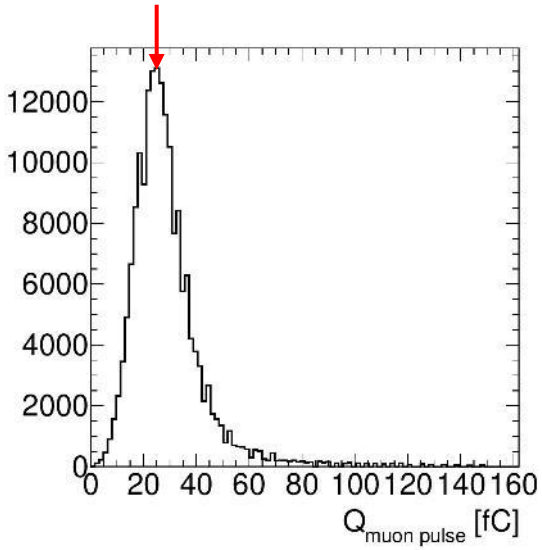


Amplify - Shape - Discriminate

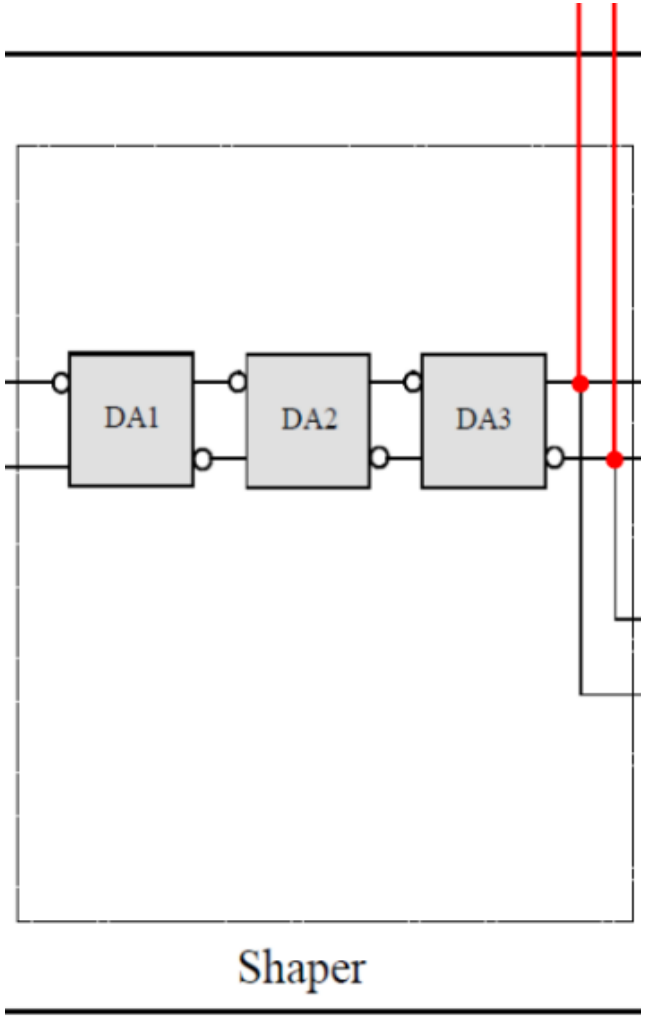


Amplification:

- Converts the charge into a voltage signal
- Needed due to the extremely low charges of ~30fC
  ($e = 1{,}6 \cdot 10^{-19} C$)



Amplify - Shape - Discriminate

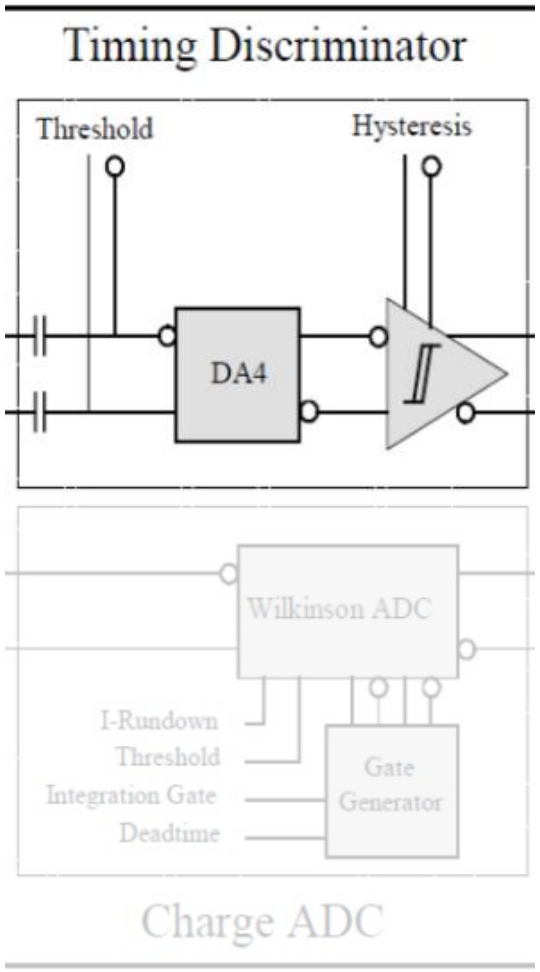


Shaping:

- Differential Amplifiers (DA)
- Amplification of the *difference* between the two inputs

→ Noise reduction

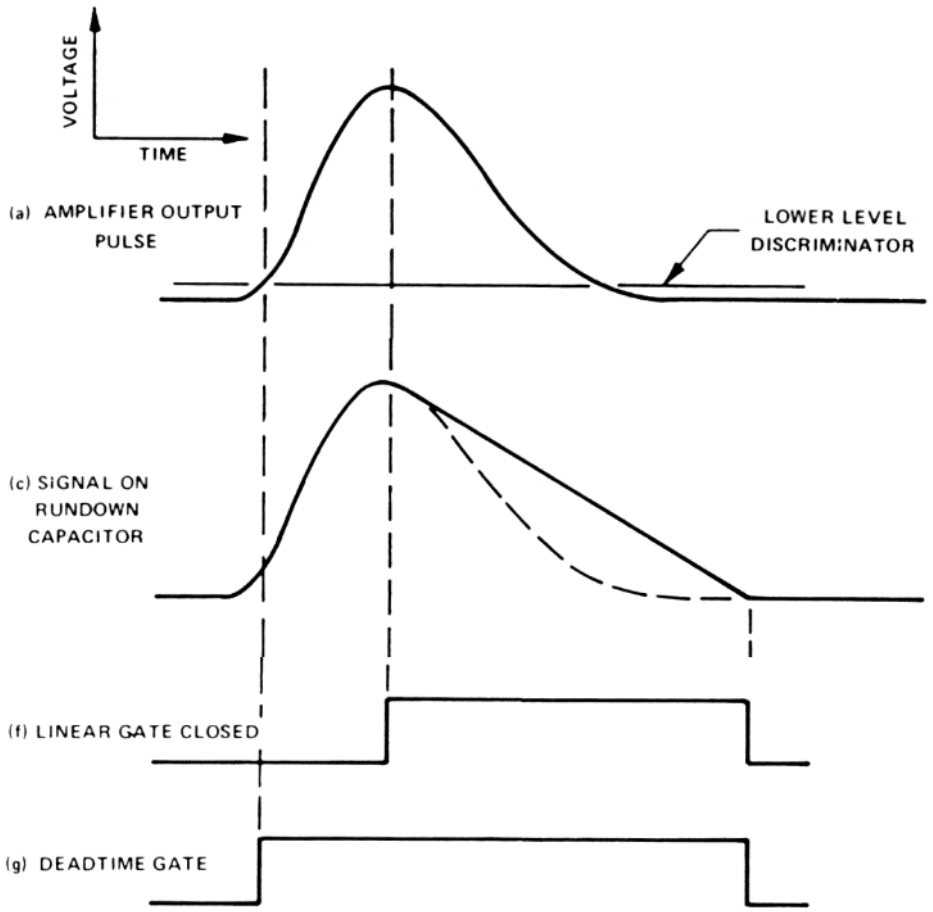
Amplify - Shape - Discriminate



Discriminating:

- Filters Pulses with a level over a certain threshold

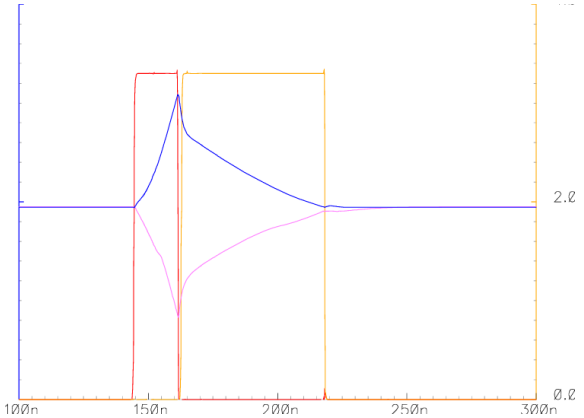
Amplify - Shape - Discriminate



Wilkinson ADC:

- Charges a capacitor with the pulse and discharges it with a constant current

  → outputs a digital signal with a length corresponding to the input charge
- only active in ADC mode
- Better time accuracy



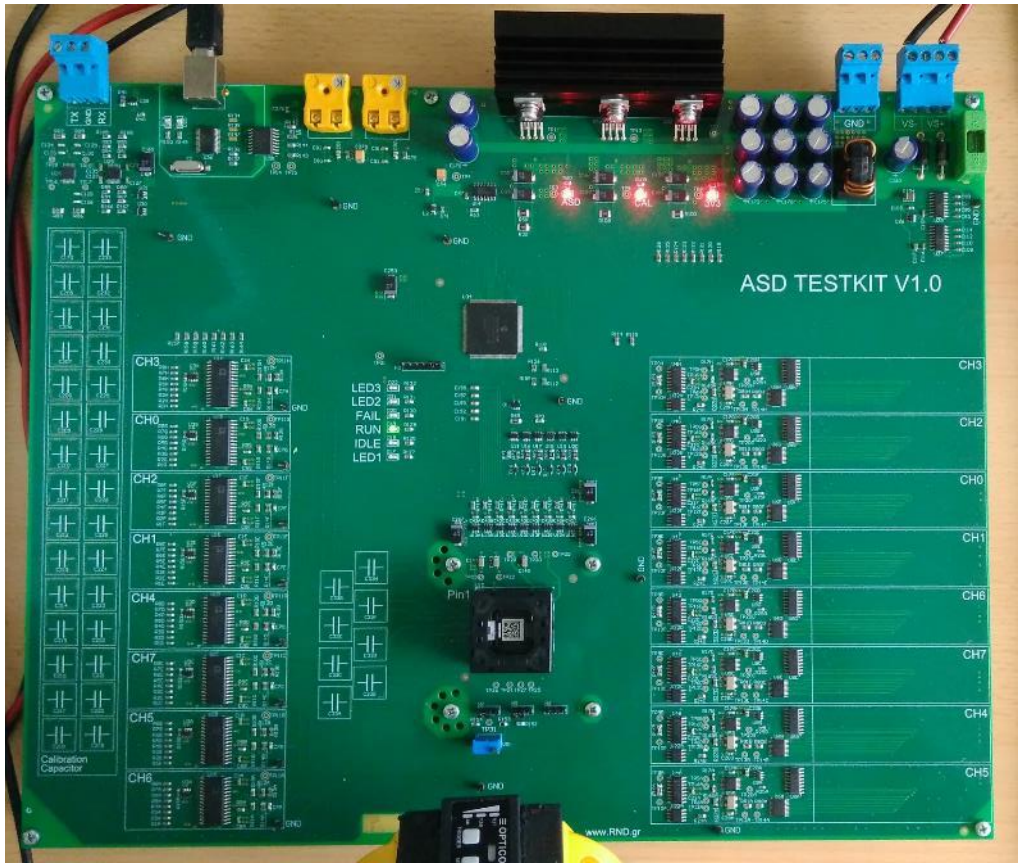
The different tests

- **Basic Health Test**
- **Dead Time Test**
- **Single Pulse Test**

Tests with a few different parameters (~2 min per test) were done with 1041 chips

Intense testing with different voltages, charges and chip-modes (~20 min per test) was performed on 33 chips

The tester

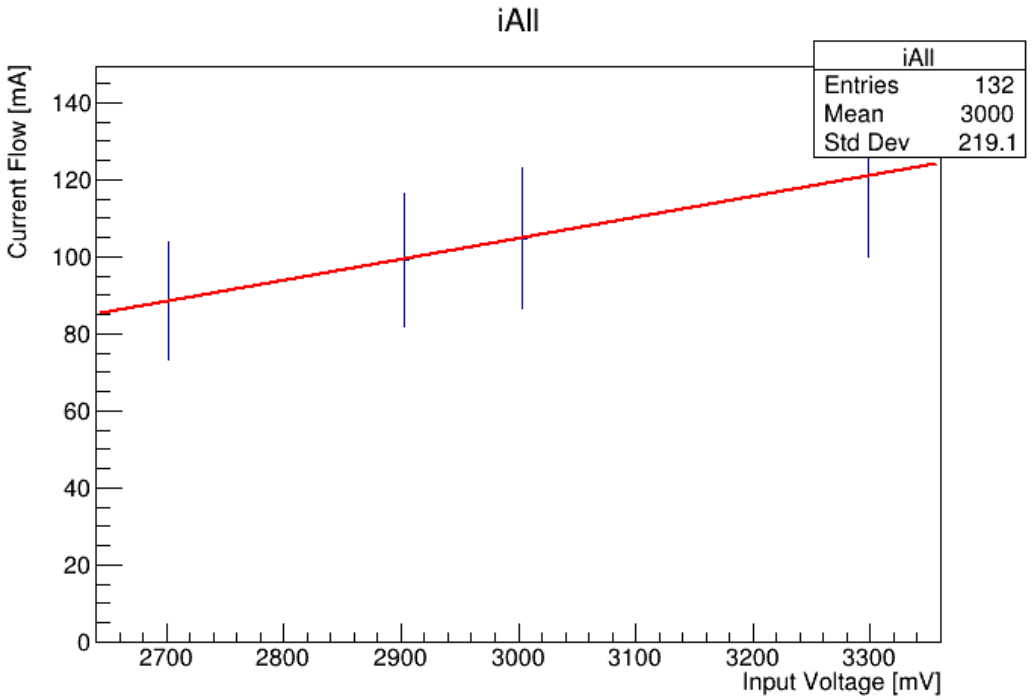


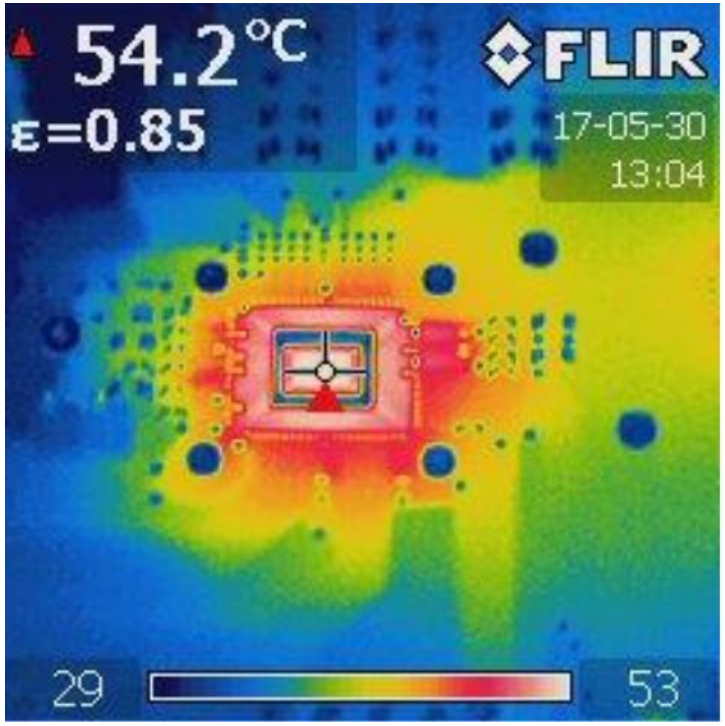
Main Components:

- Socket for the chip
- 8 Input- and 8 Output-Channels
- Power Regulators
- USB connector to PC

Basic Health Test

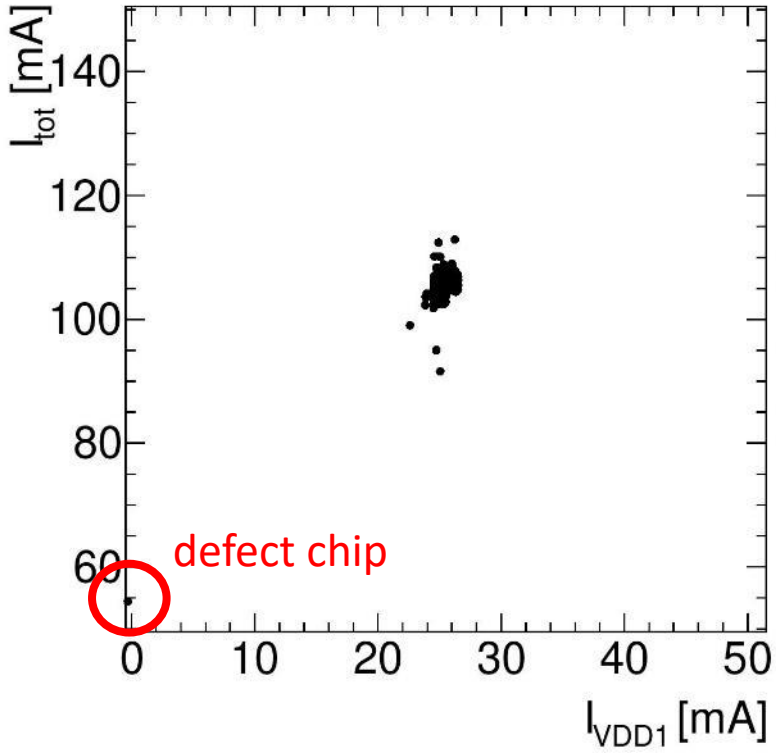
Current-Voltage relation helps to estimate the power consumption
→ Linear relationship according to Ohms law

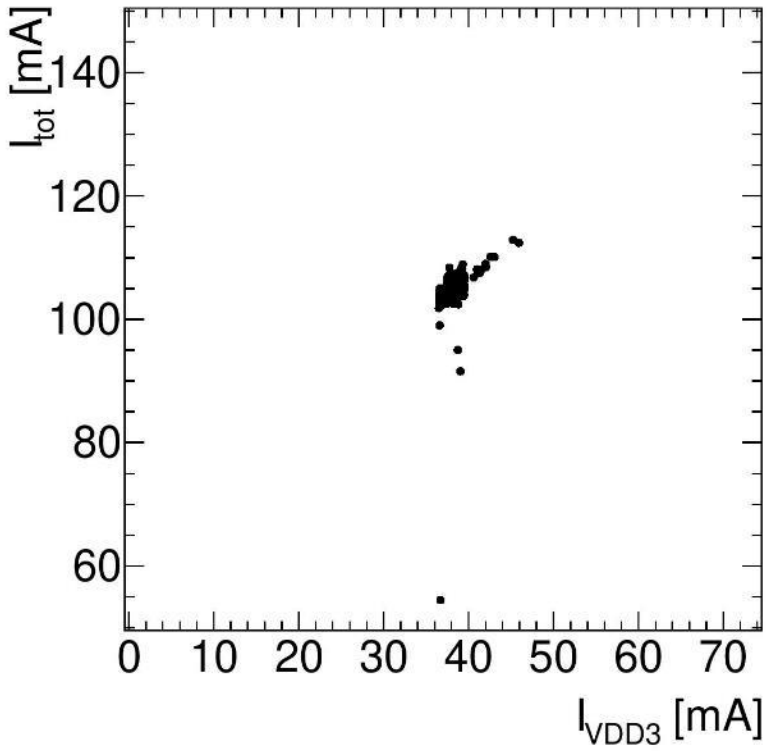


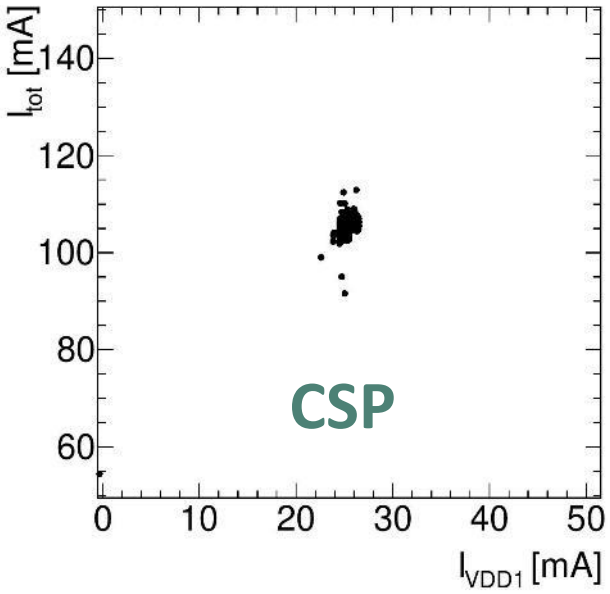


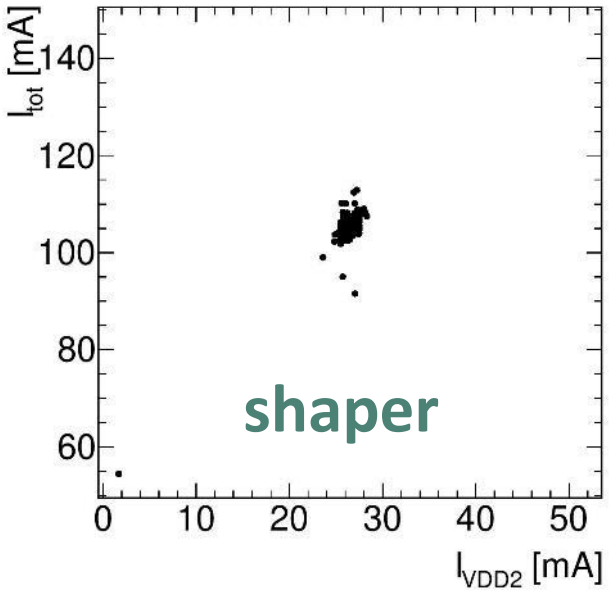
Basic Health Test

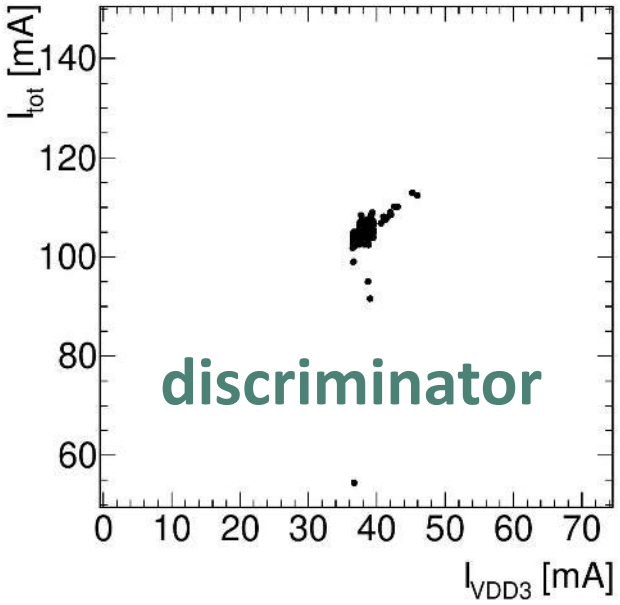
- General Health information about the chip
- Study of the input current helps to detect dead chips

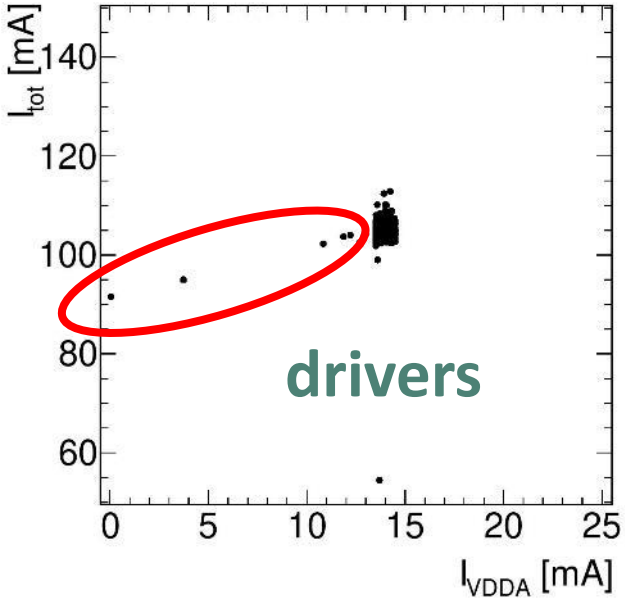












It‘s even possible to detect the malfunctioning part of the ciruit!

Dead Time Tests

- After a pulse, the chip needs some time to process other signals

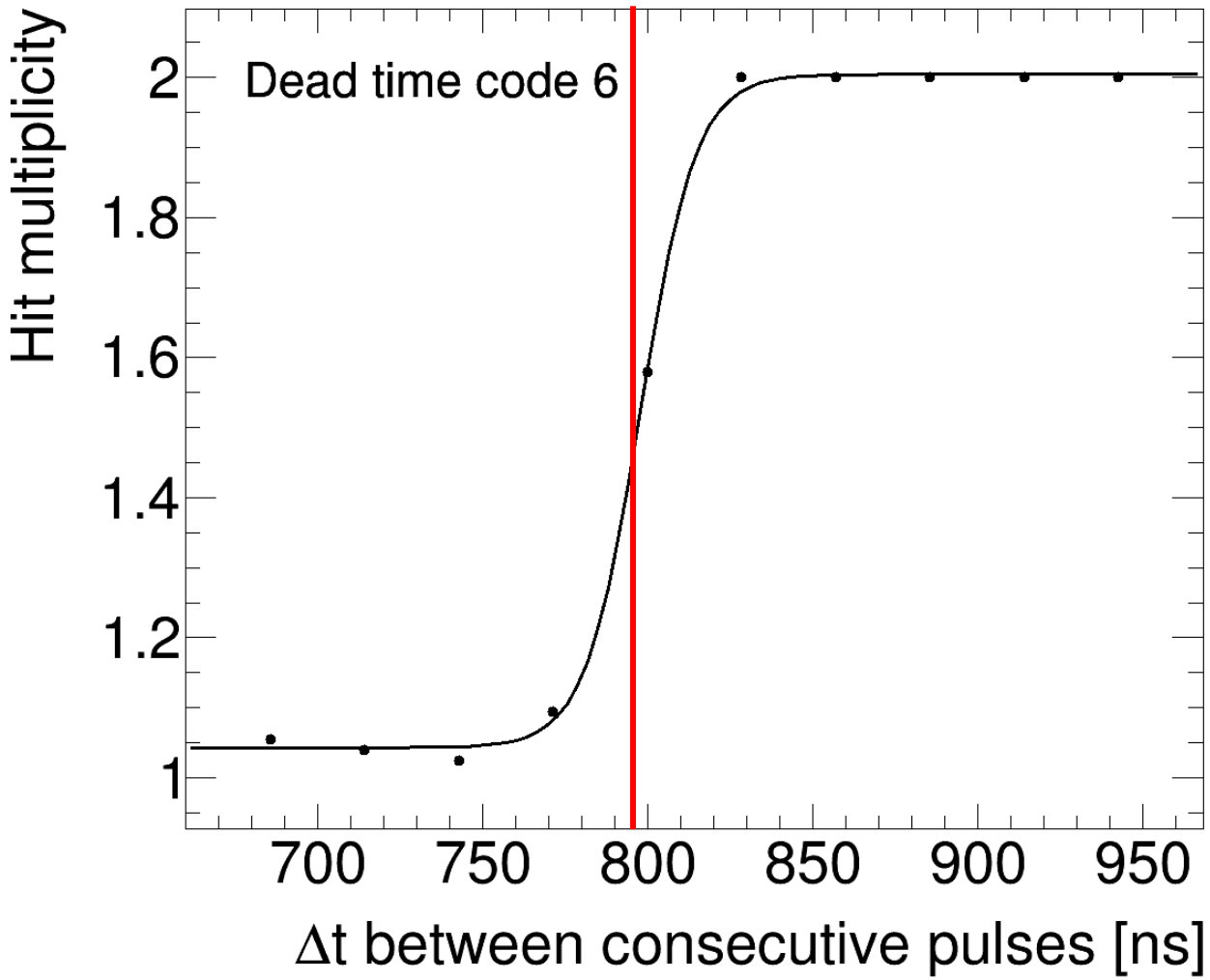
→ Critical for high counting rates

- But also: Signal pile up, detecting two signals as one big peak

How to measure?

→ Simulating two peaks short after each other and analyzing the output

Dead Time Tests



With a small Δt: one pulse is lost

Fitting via a fermi function and saving the threshold value

Dead Time Tests

About the dead time codes:

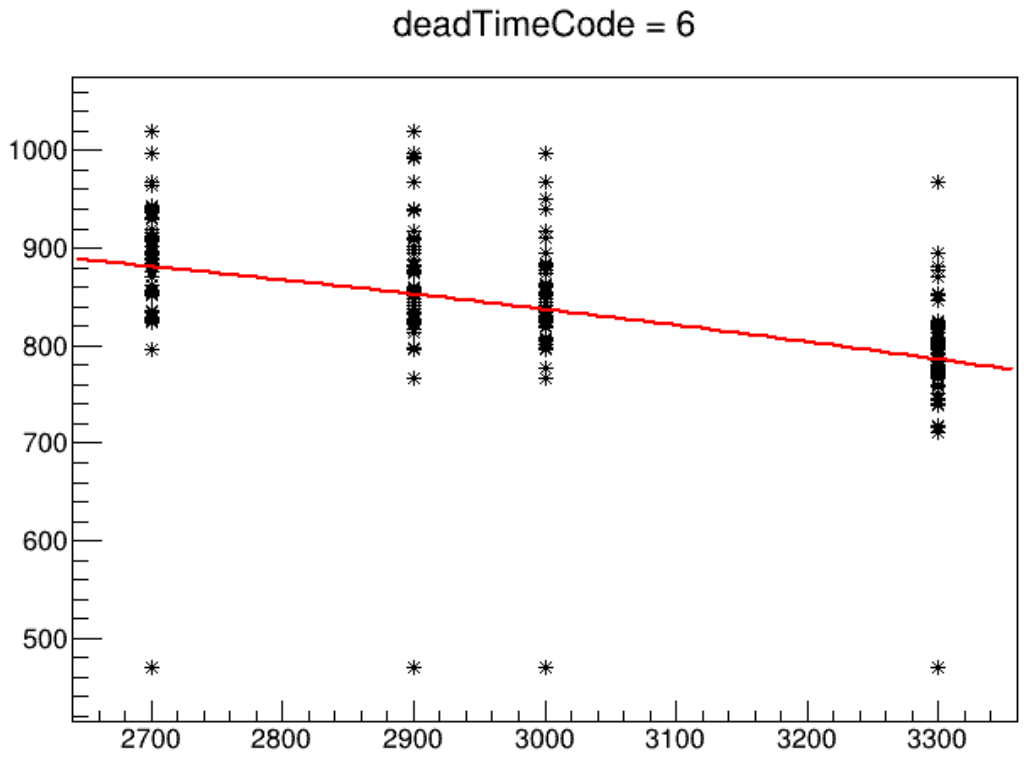
- ASD chip has programmable registers for different values
- One byte for adjusting the dead time
- In theory: linear relation

$$dead\ time = A \cdot n + B$$

Dead Time Tests

For many chips and different voltages, a decrease of the dead time can be seen at higher operating voltages with a fixed dead time code

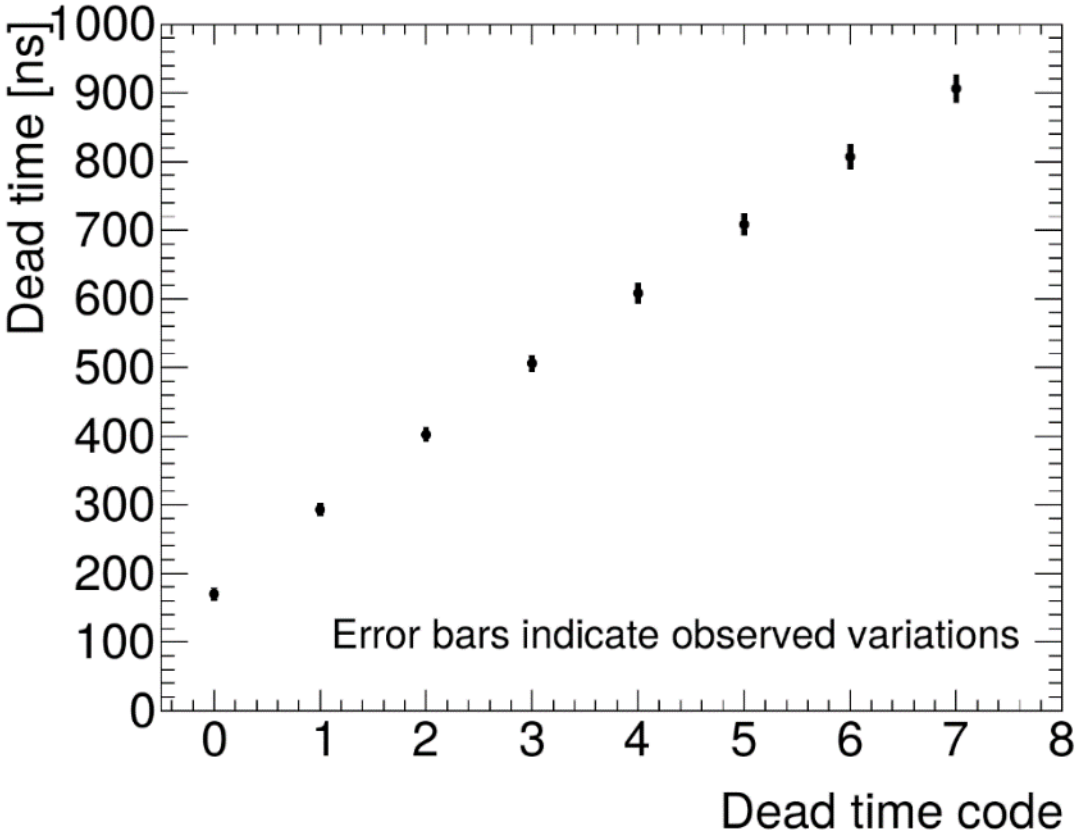
$$dead\ time(U) = A(U) \cdot n + B(U)$$



Bias current varies with the voltage!

Dead Time Tests

And is the dead time code relation linear?



Yes, the relation can be expressed with

$$dead\ time = 171ns + 105ns \cdot dtc$$

with good accuracy across all chips
(V = 3.0V)

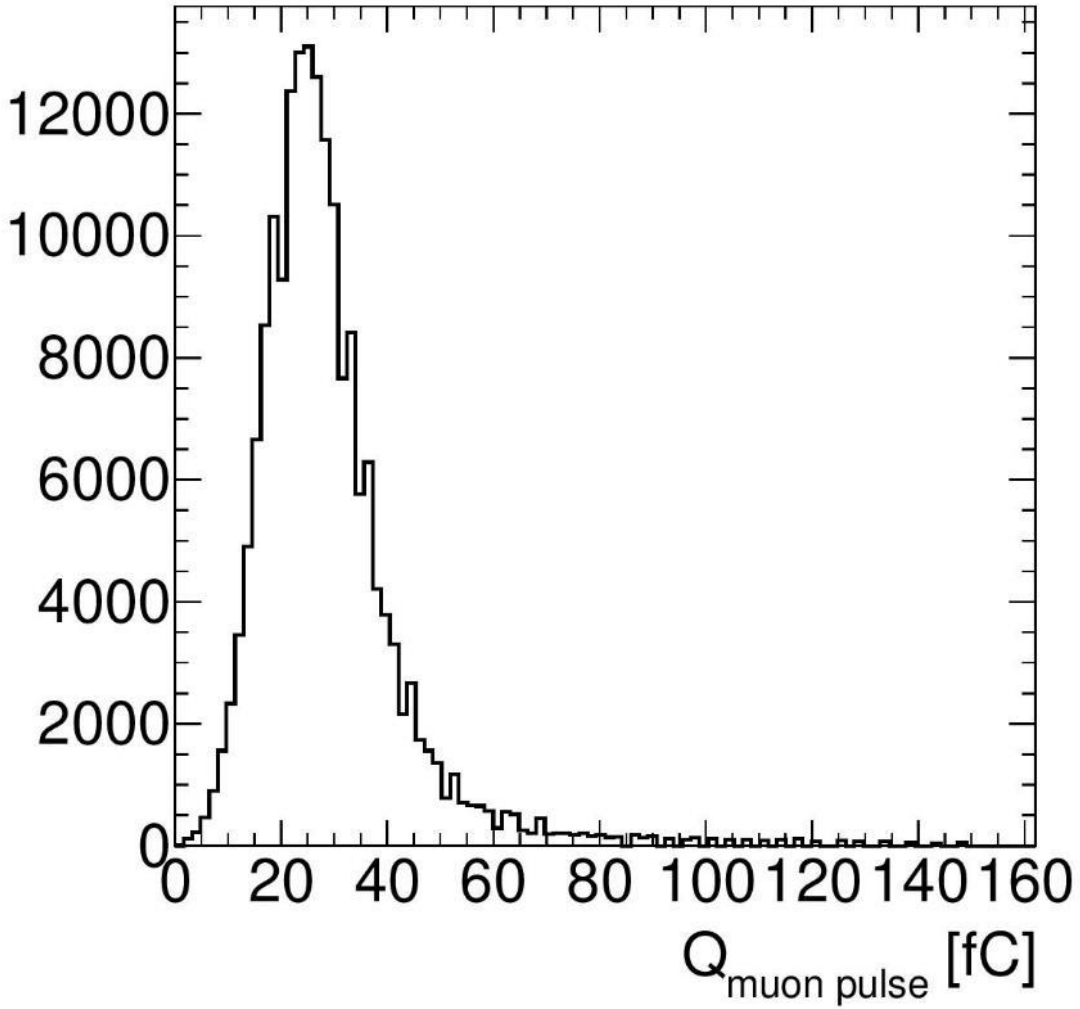
Single Pulse Test

What pulses to simulate?

→ Looking at real data from ATLAS

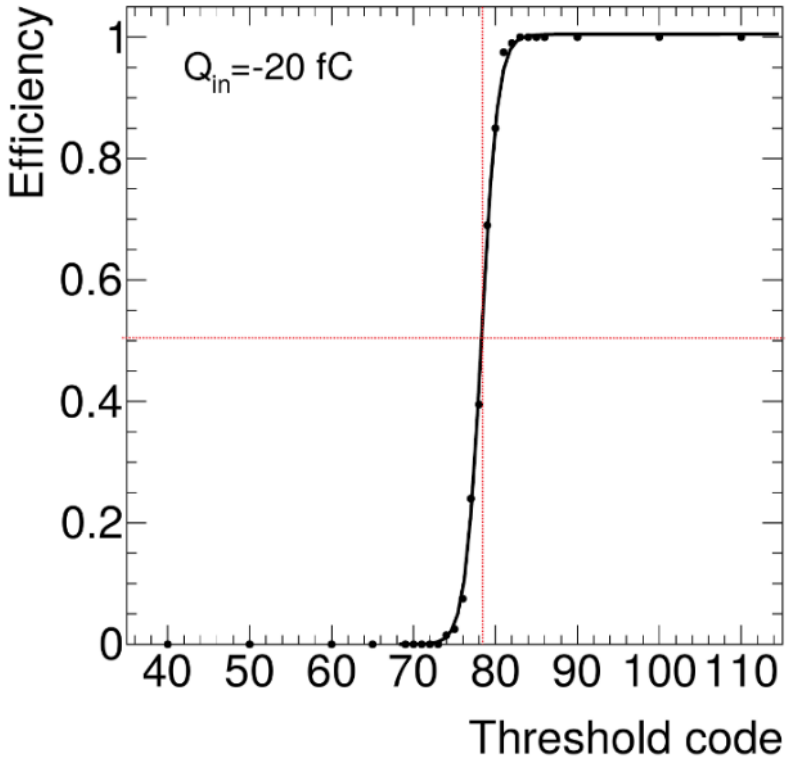
→ Most pulses are between 10fC and 50fC

→Simulating pulses with **20fC** and **40fC**



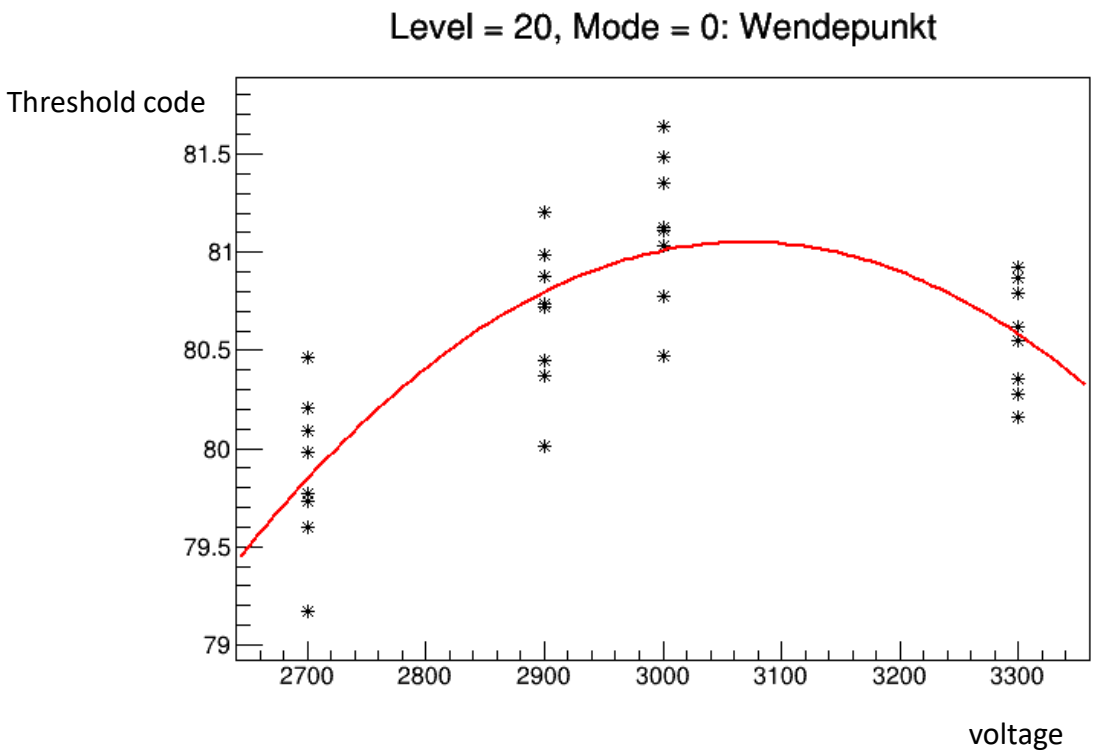
Single Pulse Test

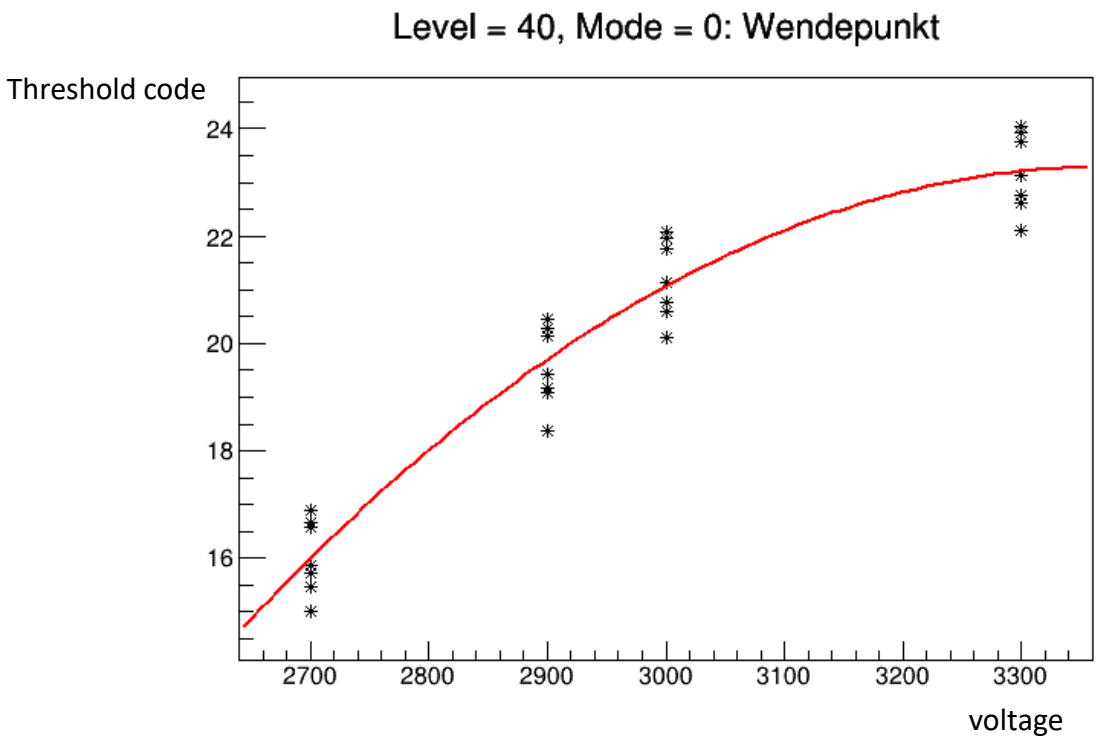
- Measuring the threshold code for different charges
- Fitting the data with a fermi-function



Single Pulse Test

- Plotting the inflection point against the voltage

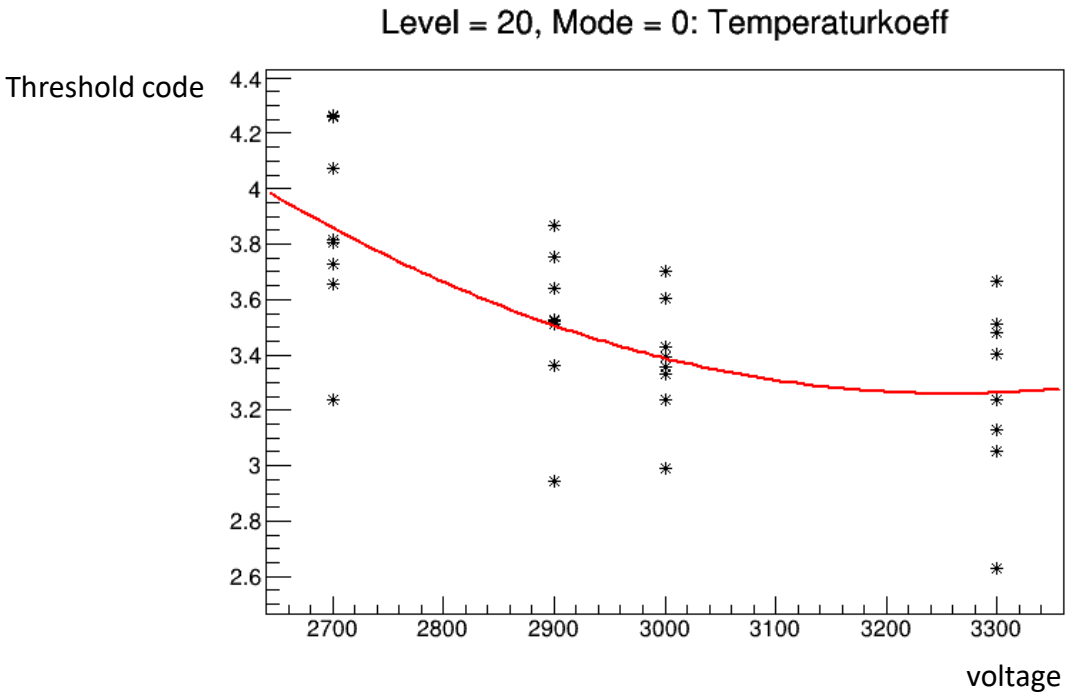


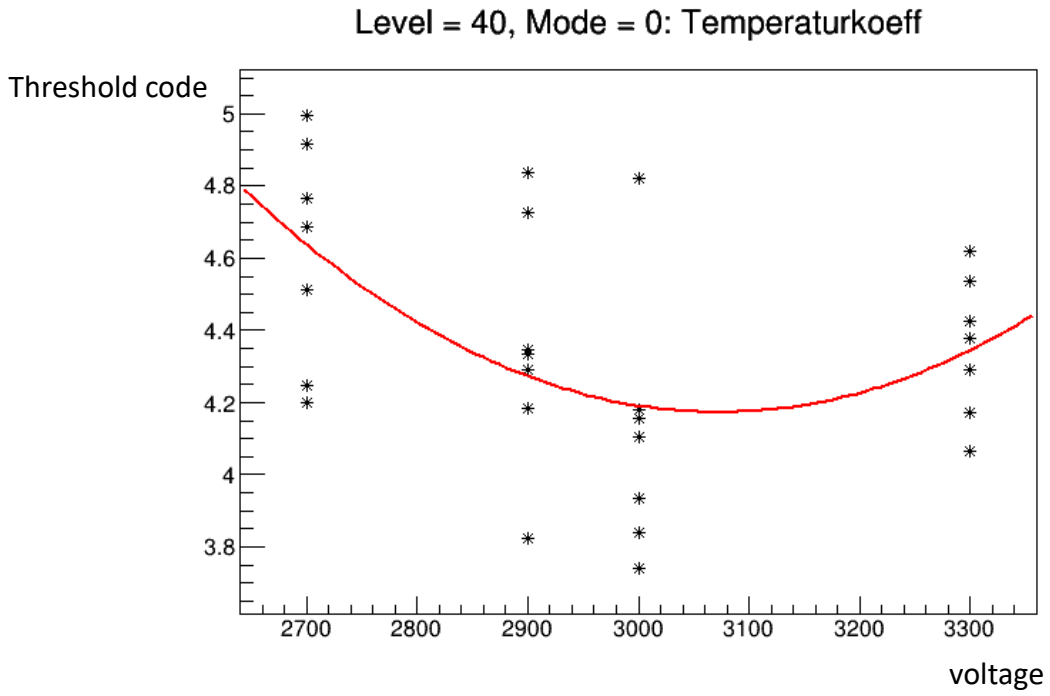


Single Pulse Test

- Same procedure with the sharpness of the fermi function

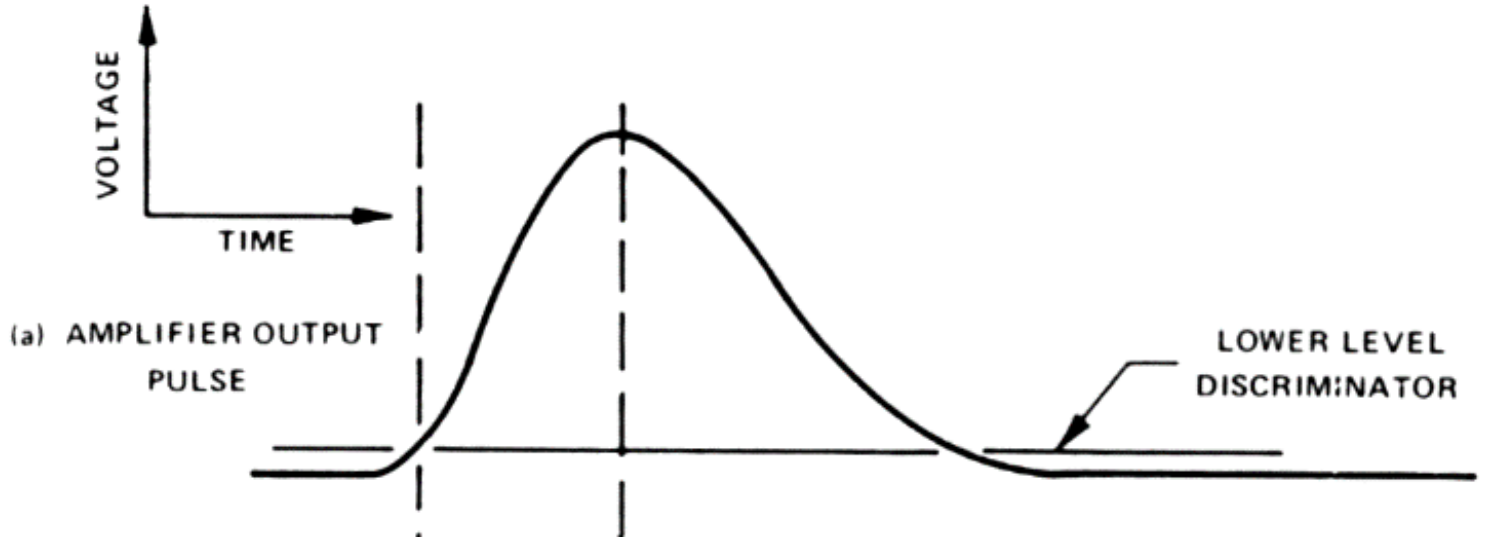
→ Sharpest edge at a voltage of ~3.1V



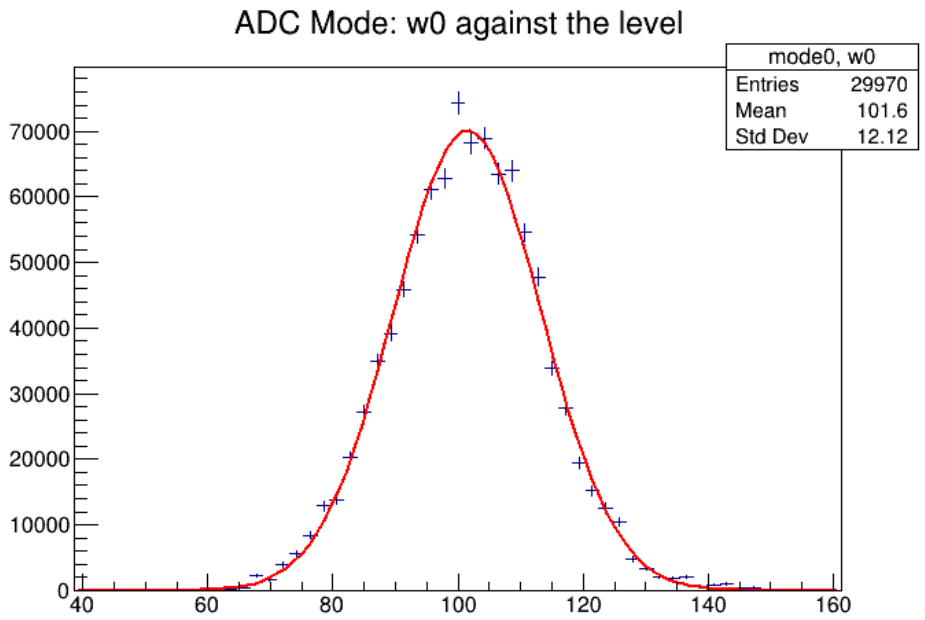


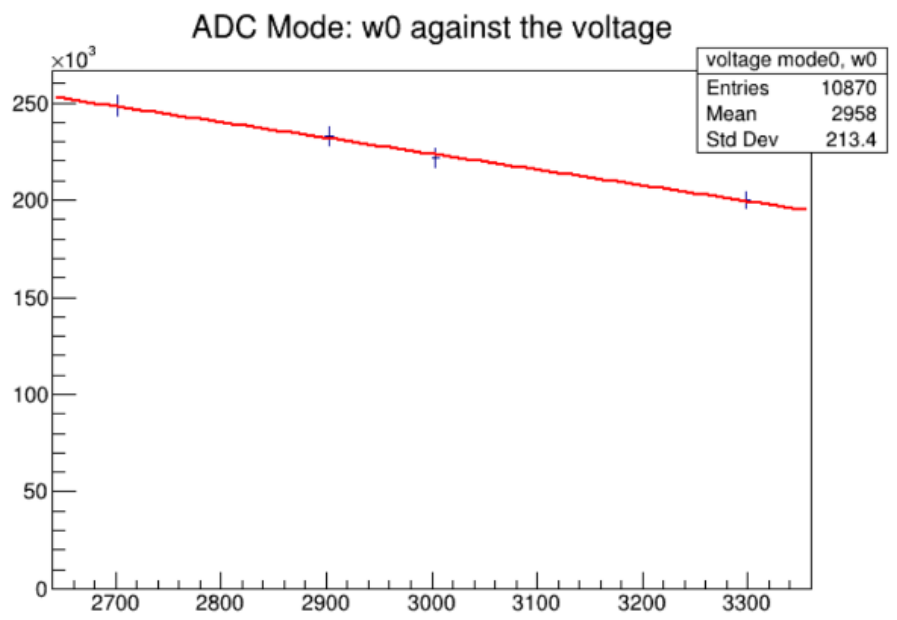
Single Pulse Test

- w0 - w7 values: Measured charges of the Wilkinson ADC after the rise time (15ns after passing the threshold)



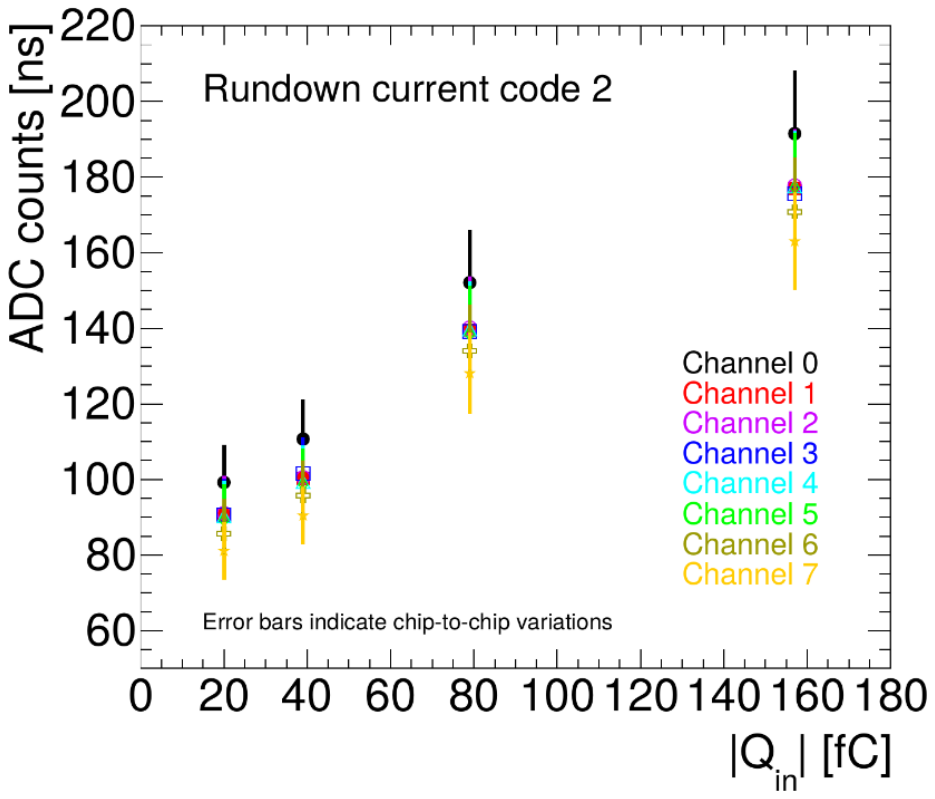
Single Pulse Test





- Gaussian curve
- Width decreases linearly with a higher voltage

Single Pulse Test



Slight differences between the different channels (especially channel 0)

Current Problems and Further Plan

- Currently tests with optimized testing parameters on ~1200 chips

  (V = 3.0V, pulses with 20fC and 40fC, only ADC-mode)

- Combined test of the whole mezzanine board
- Preparation of automated testing