RUPRECHT-KARLS-
UNIVERSITÄT
HEIDELBERG

SWITCHER-B

Report on Submission

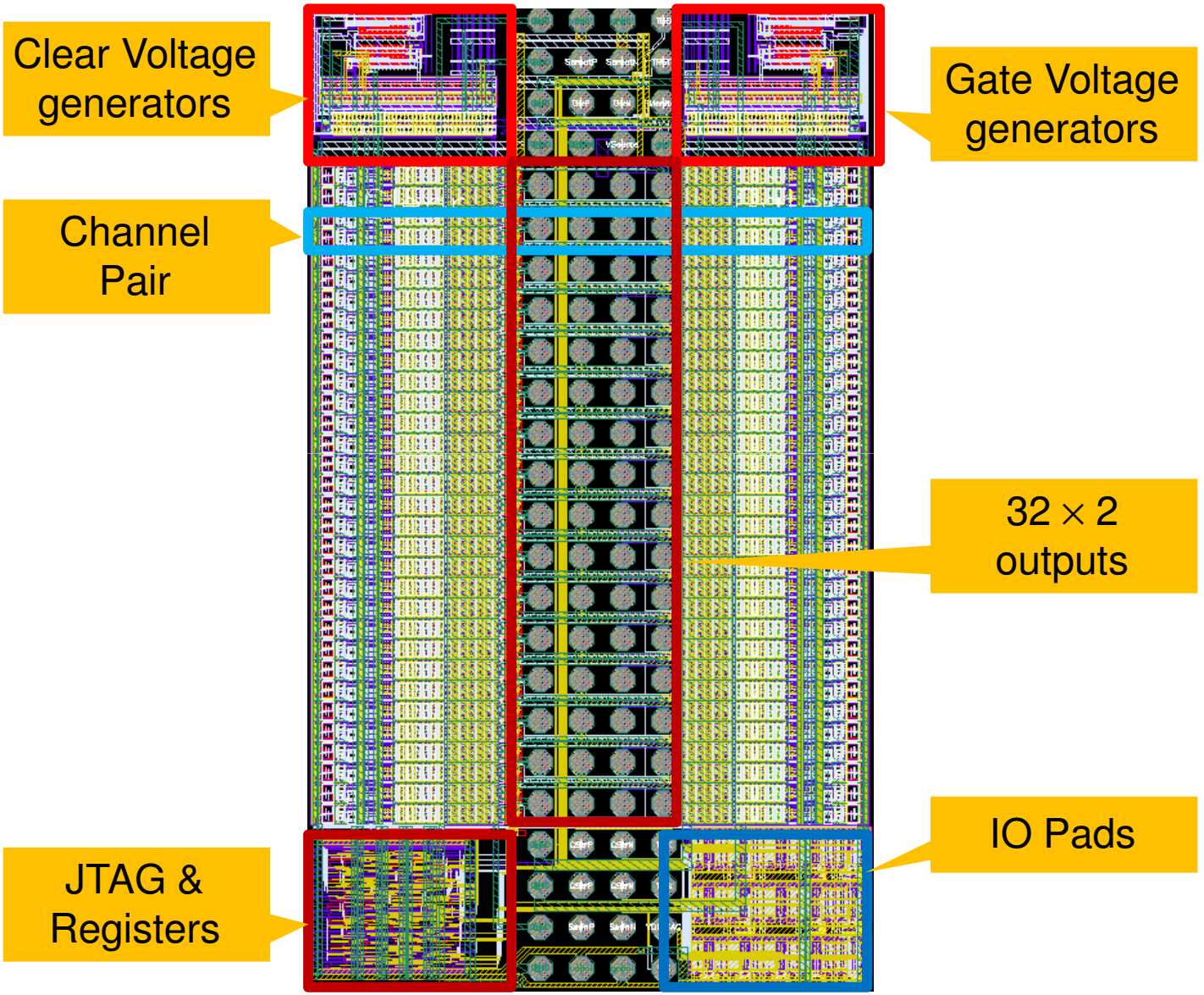
P. Fischer, I. Peric, Ch. Kreidl, J. Kinzel
Heidelberg University

Summary

- Switcher-B has been submitted to AMS on 15.2.2010

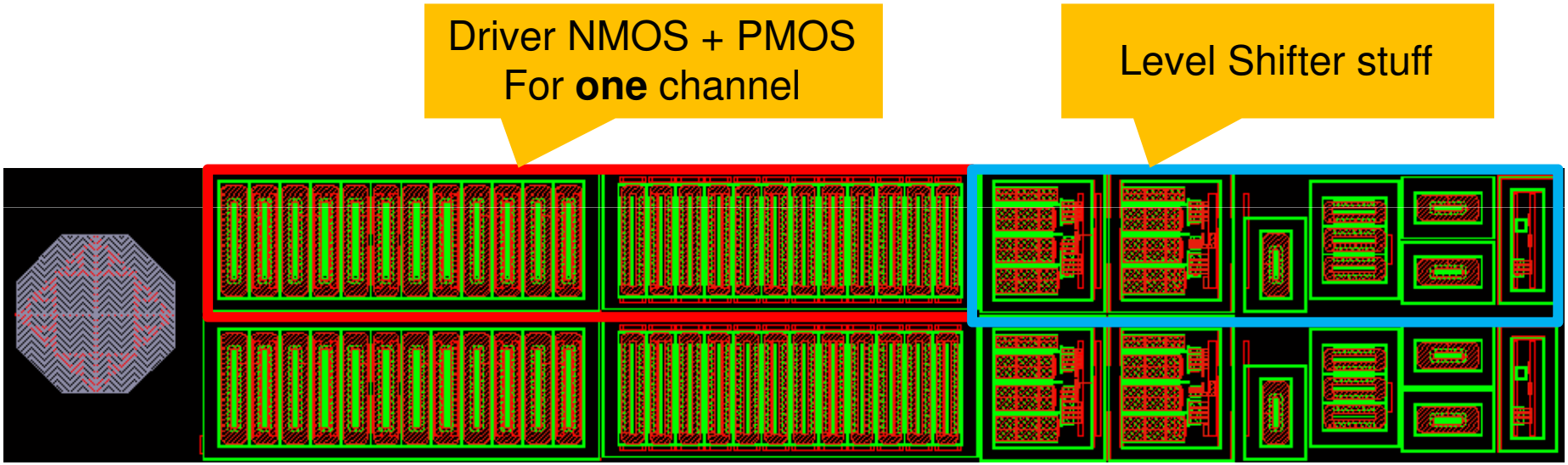
- Main features:
  - 32 × 2 channels
  - 3600 × 2035 µm^2 (wider than planed, HV transistors!)
  - Fast HV switches up to 30V, Rad. hard-proven design
  - Internal generation of auxiliary voltages
  - JTAG Interface, IO Voltage of 1.2 – 3.3 V
  - Registers with triple redundancy
  - Bump bonding only, compatible to balcony layout (hopefully…):
    - 32 x 2 outputs
    - 32 pads for power / control
    - 150µm pitch, 80µm pad opening

Chip Layout


Clear Voltage generators
Gate Voltage generators
Channel Pair
32 × 2 outputs
IO Pads
JTAG & Registers

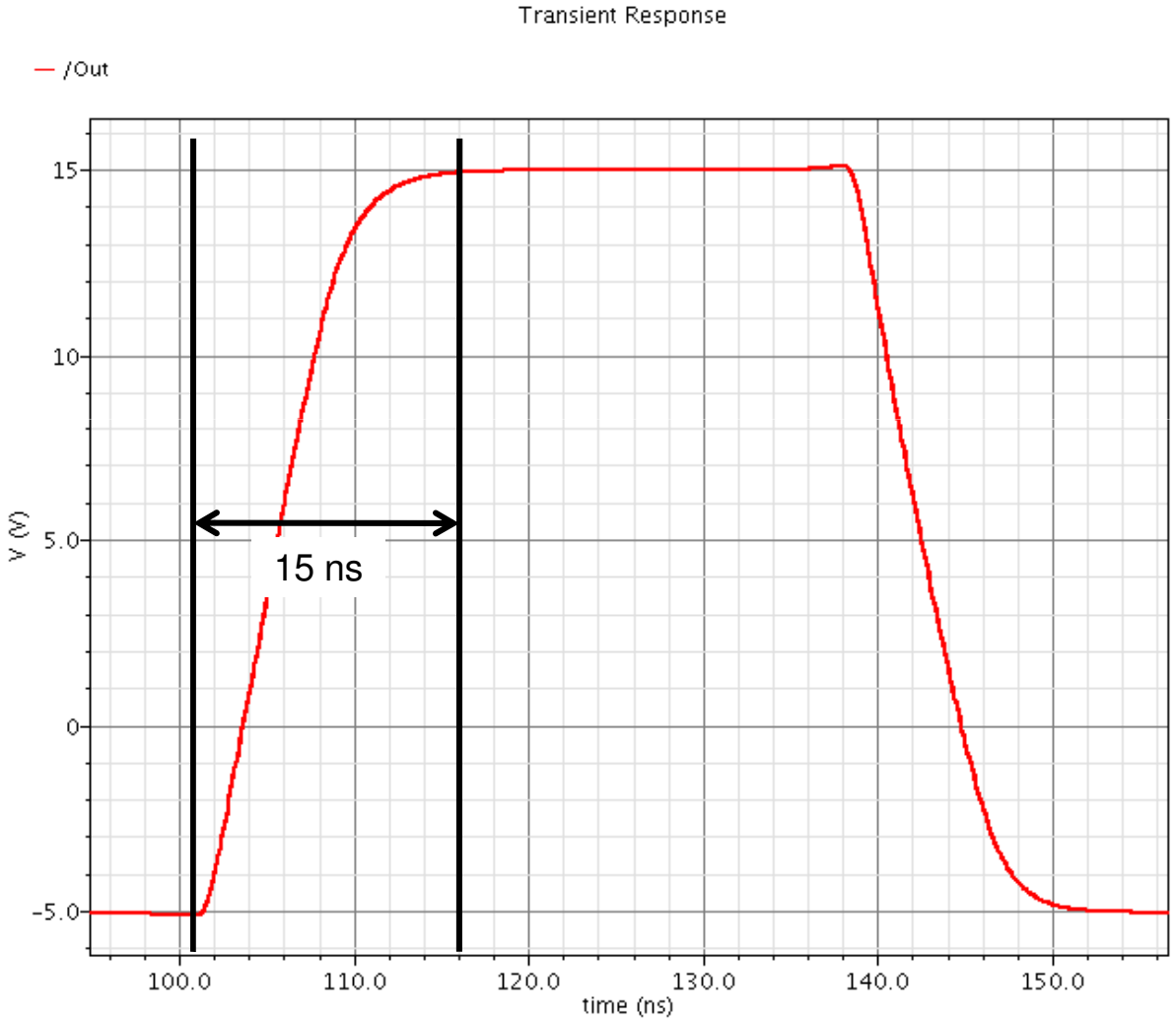
HV Channel

- Chip width determined by required size of HV driver transistors to switch large capacitive loads of 50pF fast.



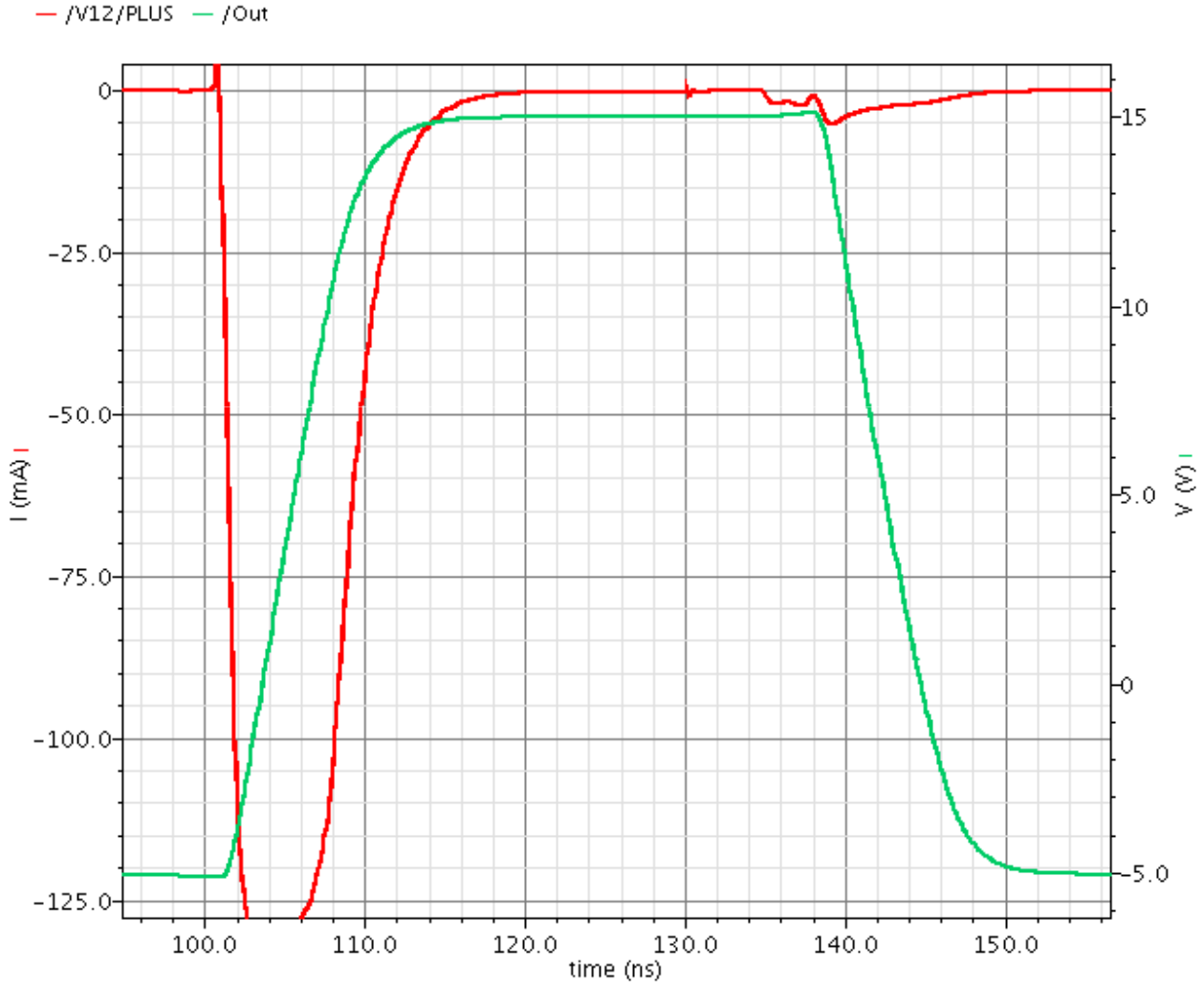
Speed

- Simulation of 20V clear pulse into 50 pF:



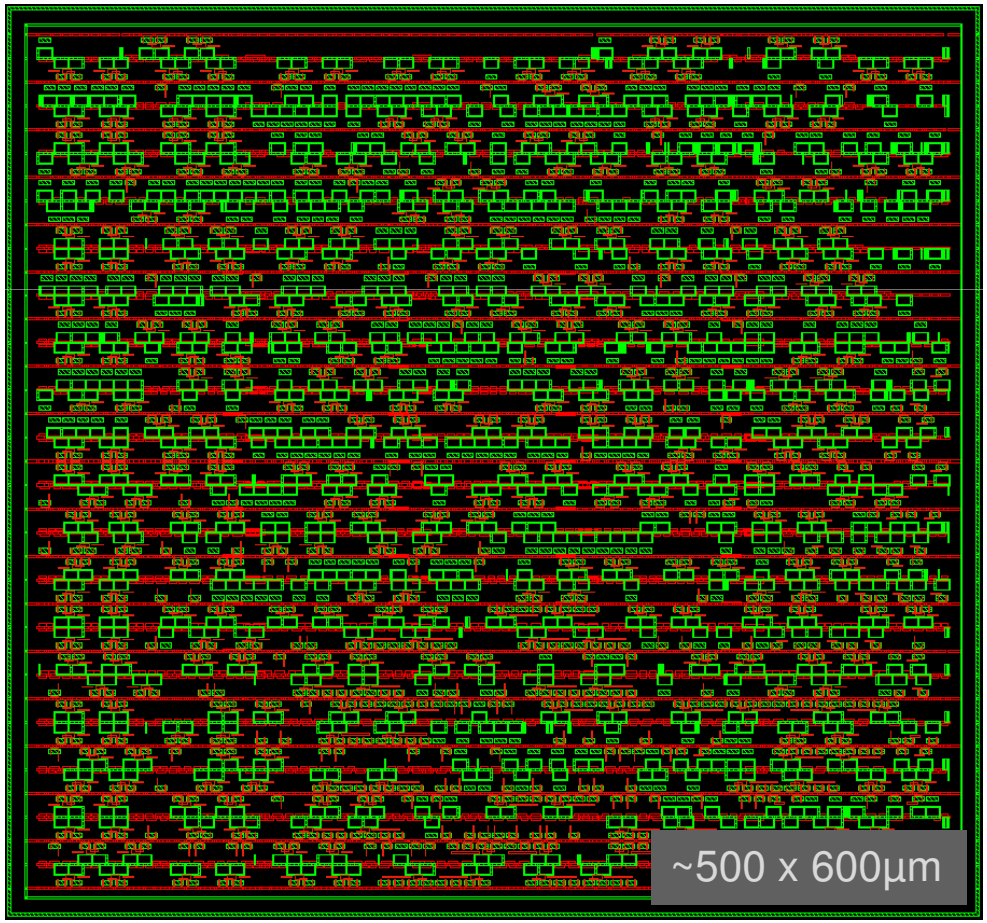
Supply Current Spike

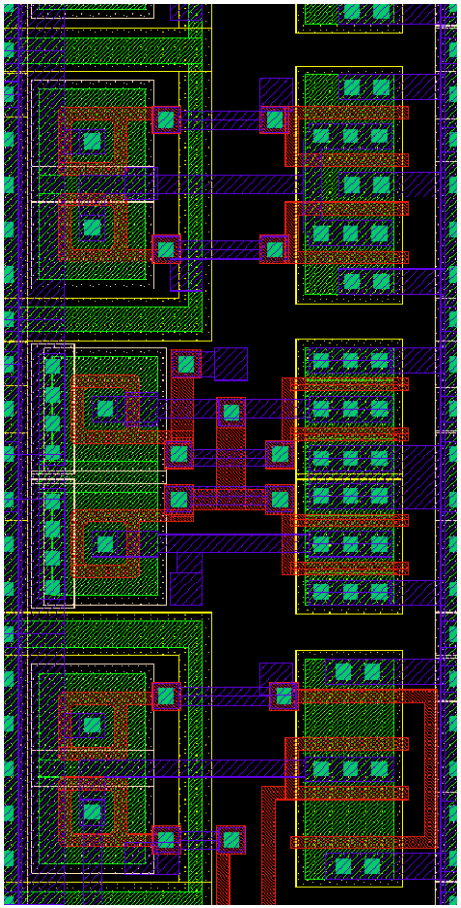
- $Q = C \times U = I \times T \rightarrow I = C \times U/T = 50p \times 20V / 10n = 100\ mA$ (!)



JTAG

- Self made rad hard lib (Peter) characterized by Cadence tools (Jochen & Michael Ritzert)
- Synthesized interface w. boundary scan, registers (Jochen)





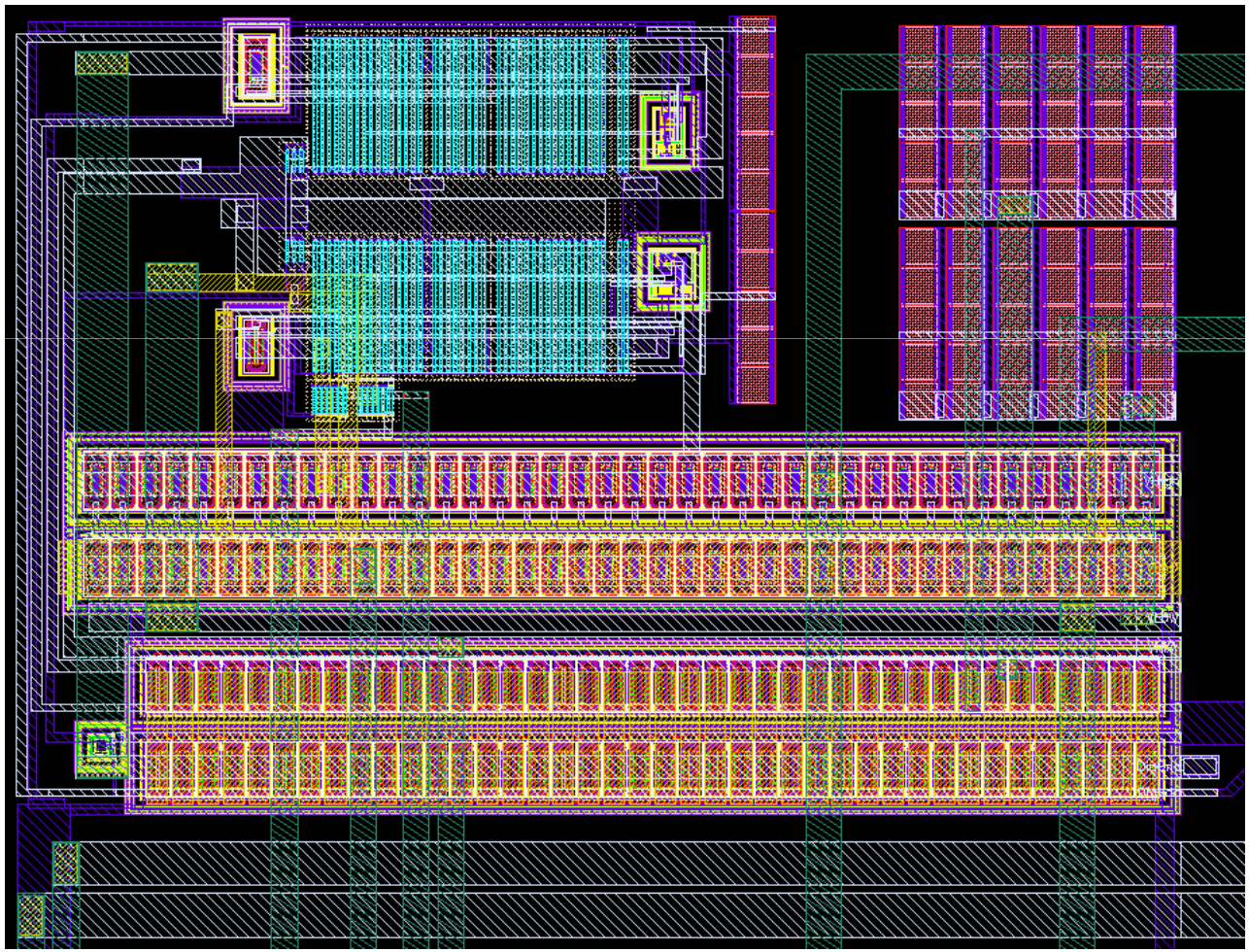
JTAG Functionality

- Full JTAG protocol, including RSTb
- Boundary Scan of all cells
- All pins have level shifters and pull down resistors
- Internal registers are triple mode redundant.
  16 available, only 4 used so far:
  - 2 x Bias of level shifter in idle mode
  - 2 x Bias of level shifter in boosted mode

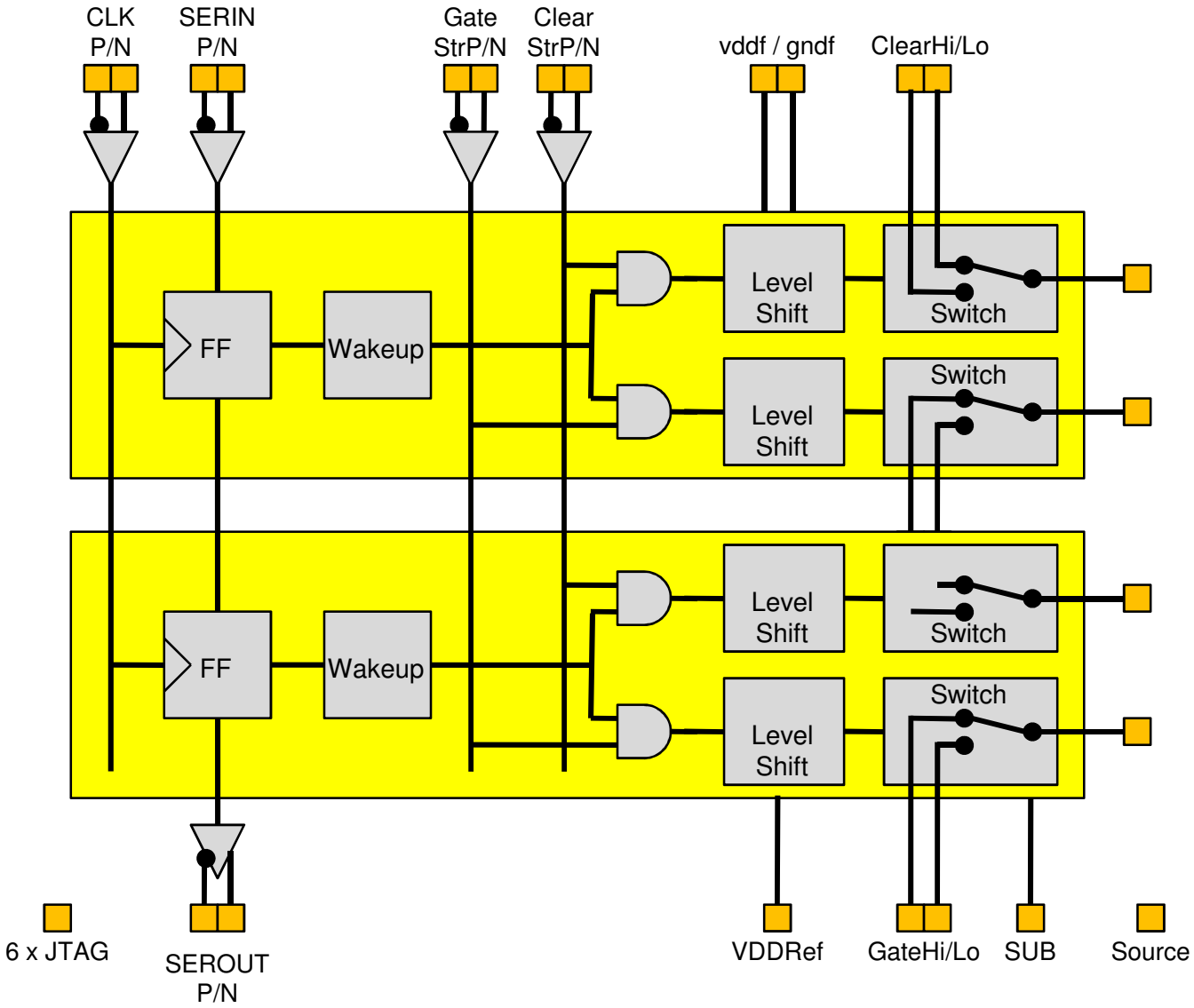
- Later:
  - Termination resistors
  - Current in LVDS drivers / receivers

Regulators

- Generate voltages 3.3V above VLO and 3.3V below VHI
- VDDRef = 3.3V reference must be supplied! (wrt. gnd!)



Simplified Block Diagram



Signals / Pins

Signal	Signals	Pads	Function
Substrat (gnd!)	1	1	
Floating VDD and GND	2 x 2	4	
VDDRef (gnd! + 3.3V)	1	1	For aux. voltages
ClearHI / ClearLO / GateHI / GateLO	4 x 2	8	Switch HV Voltages
VSource	1	1	For decoupling
Shift register: Clk, Serin, Serout	3 x 2	6	LVDS
Gate_Strobe, Clear_Strobe	2 x 2	4	LVDS
JTAG: TCK, TMS, TDI, TDO,TRSTb	5	5	
VDDJTAG	1	1	
unused	1	1	Reserved for monitor
Sum		32	

NOT implemented

- Due to lack of time, some desired features could NOT be implemented:
  - No termination resistors
  - Serial output has no real LVDS pad (one pad = ½ VDD, other pad = CMOS)
  - No decoupling to Vsource (no significant layout space available, need to make regulators and IO cells compacter)
  - No monitor

- Should be perfectly usable for our first tests!

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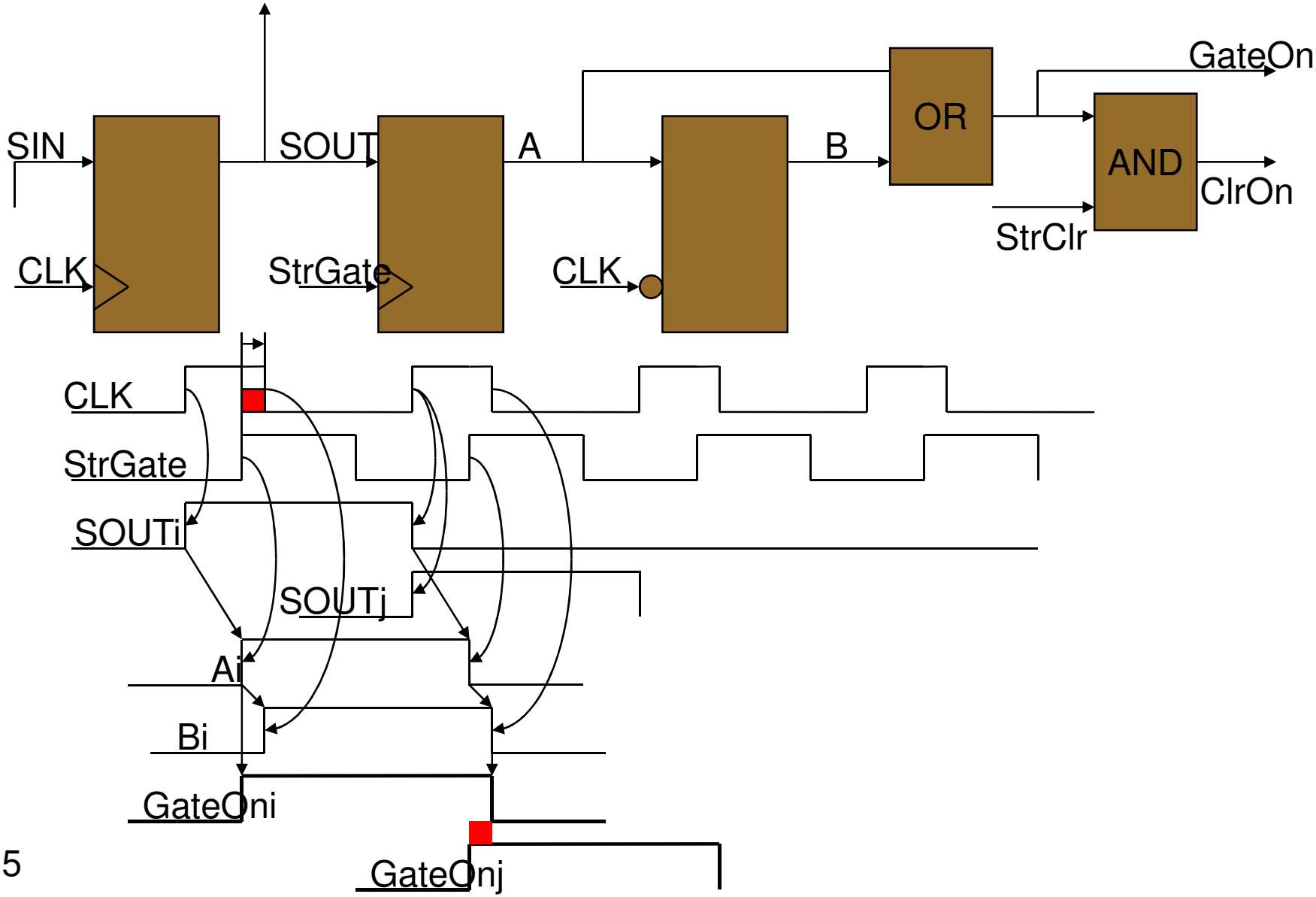
Improvements on next (‘final’) iteration

- Alignment marks for bumping
- Reduced input protections & smaller layout, move IO cells to bump pads
- Re-layout voltage regulator with wider traces
- Decoupling caps for Vsource
- Programmable termination resistors
- Real LVDS driver with variable current
- Maybe
  - Test circuit to check selectable output via monitor
  - Extra small pads for KGD probing

Timing Control Logic

- As presented by Ivan in Prague
- For details see next 2 slides

Control logic – standard operation



Control logic – skipping of channels