DPG 2010 – T60.3
Extraction of Parasitic RC Parameters of a DEPFET Pixel Matrix

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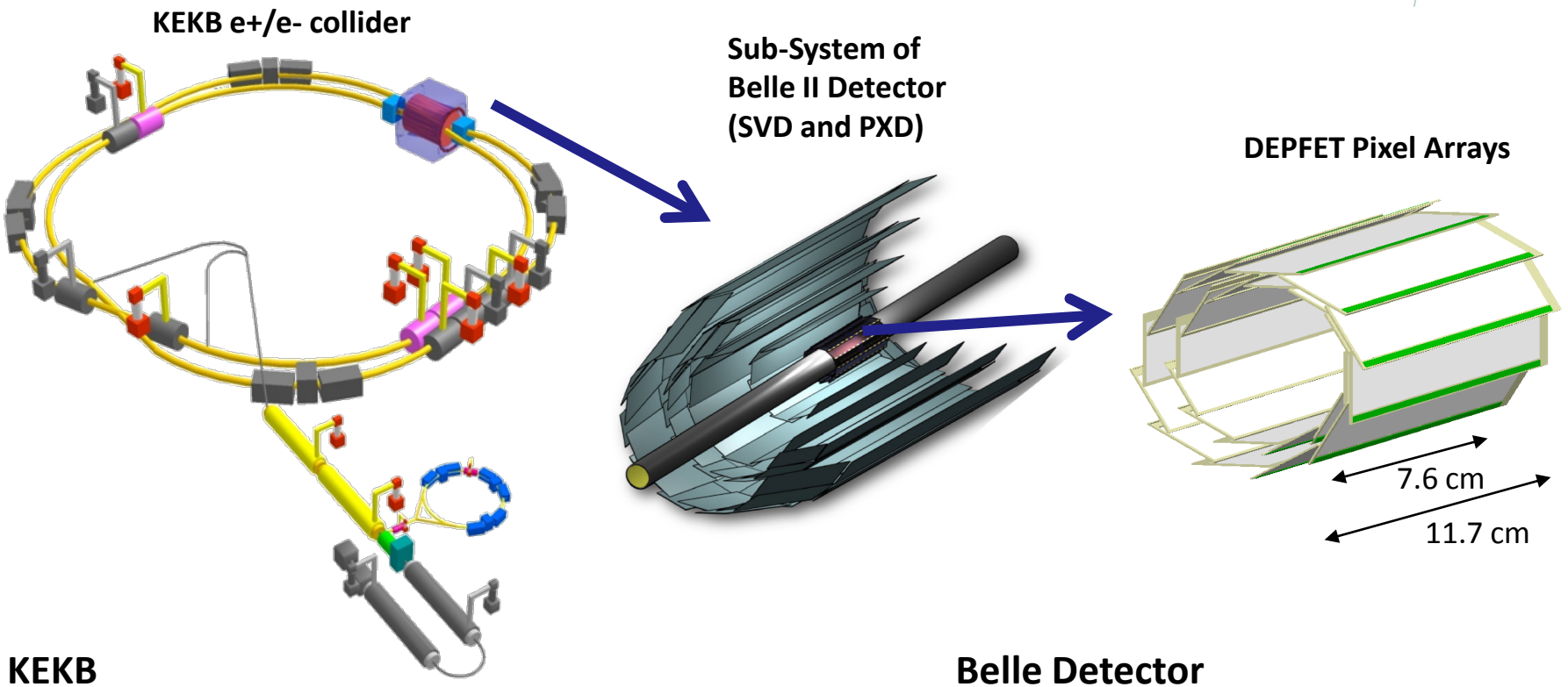
Overview

- DEPFET Pixel in the Belle-II Detector @ SuperKEKB
- DEPFET Pixel and Operation Principle
- DEPFET Pixel Matrix – Array Layout
- Why Parasitic RC Parameter Extraction?
- Method and Tools of the Parasitic Extraction
- First Results of DEPFET Matrix Simulation incl. Parasitic RCs
- Summary & Outlook

DEPFET PXD for Belle II Detector @ SuperKEKB



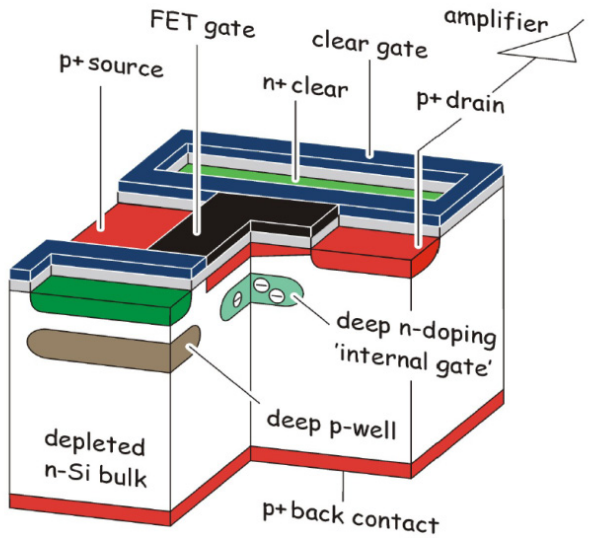
KEKB

- Aims to prove CP-violations in the B meson/anti-B meson decay (CP = charge-parity)
- Upgrade of KEKB to improve the rate of particle collisions by a factor of 40

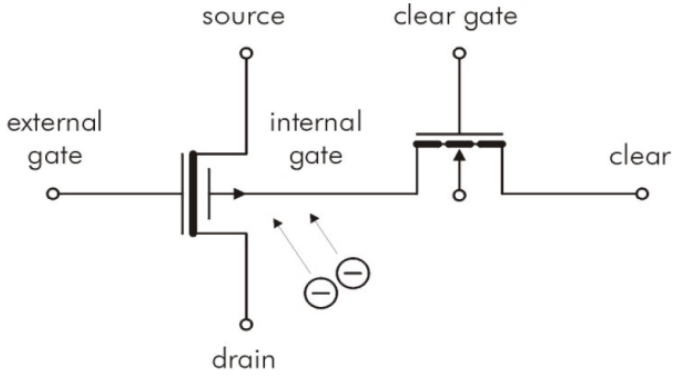
Belle Detector

- Detection of particles which result from the e+/e- collision
- SVD: 4 layers of double sided silicon strip sensors
- PIX: 2 layers of DEPFET pixel detectors

DEPFET Pixel and Operation Principle



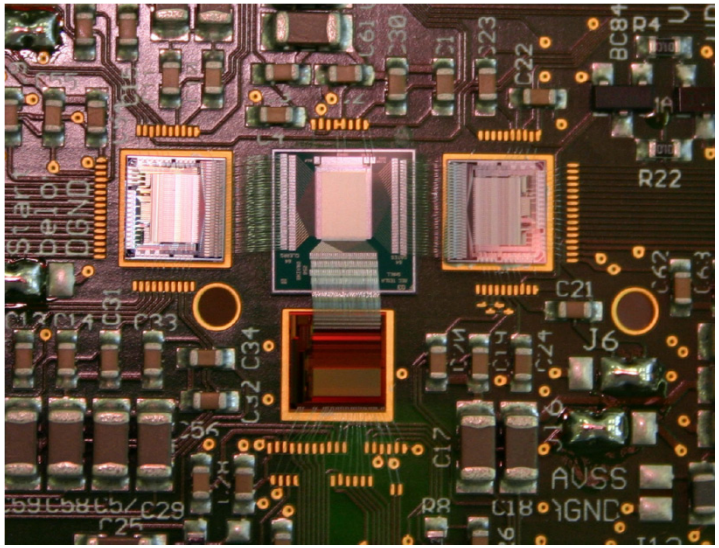
J. Kemmer & G. Lutz, 1987

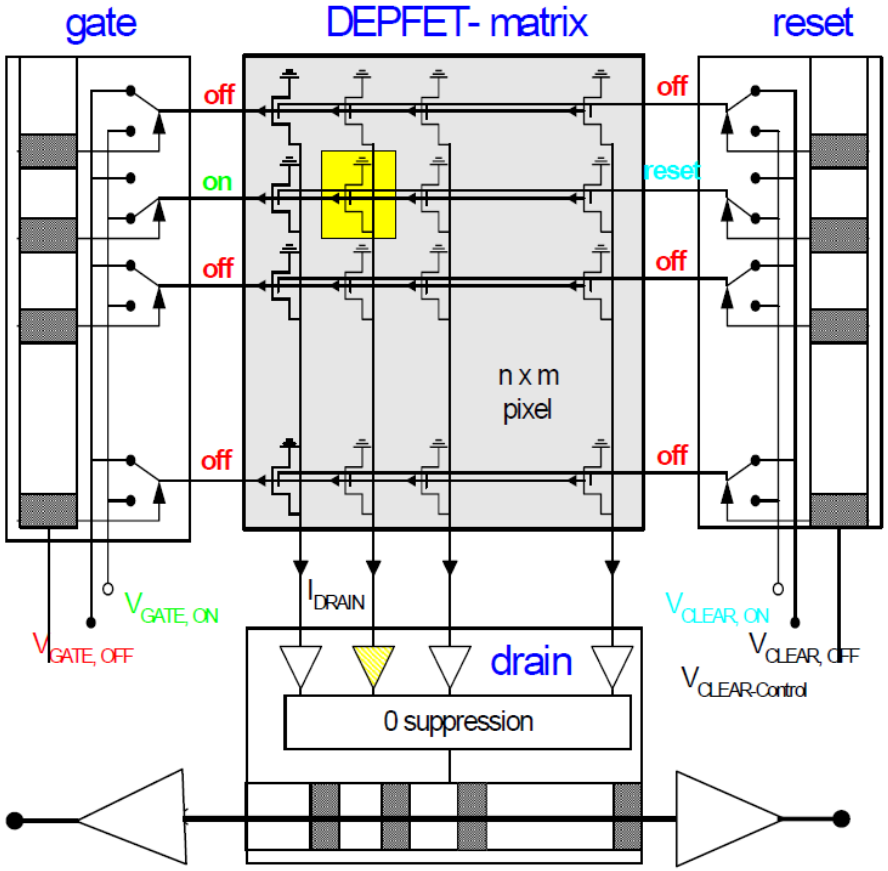


- DEPFET is an acronym for depleted p-channel field effect transistor
- Collection of electrons within the internal gate
- Modulation of the FET current by the charge in the internal gate
- Fully depleted sensitive volume
- Charge collection in the transistor "off" state, read out on demand
- Clear contact to empty the internal gate

DEPFET Pixel Matrix

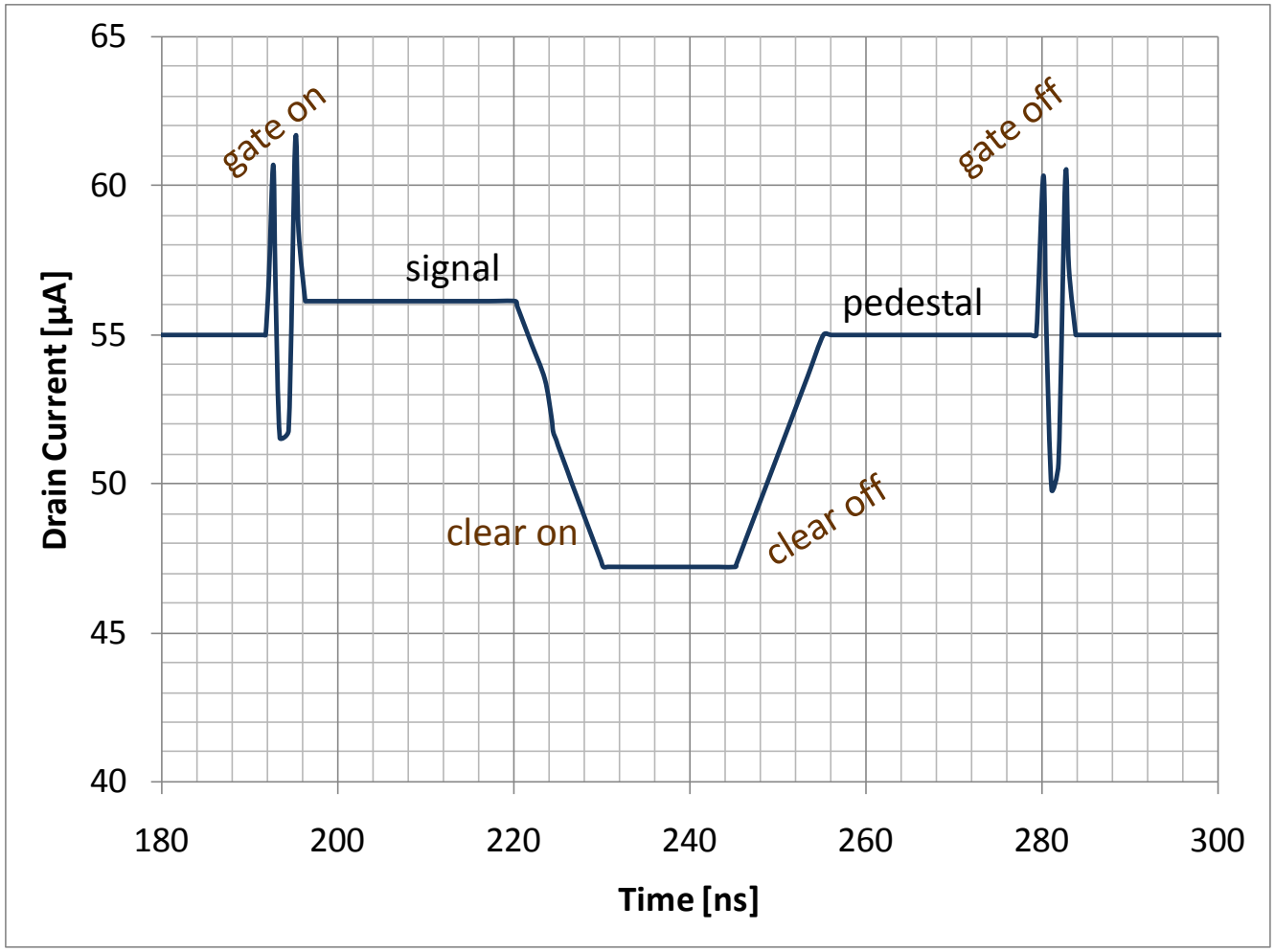
- Row wise read-out ("rolling shutter„)
- Correlated double sampling and single sampling possible
- auxiliary ASICs needed for row seleciton, clear and current read-out





Why Parasitic RC Parameter Extraction?

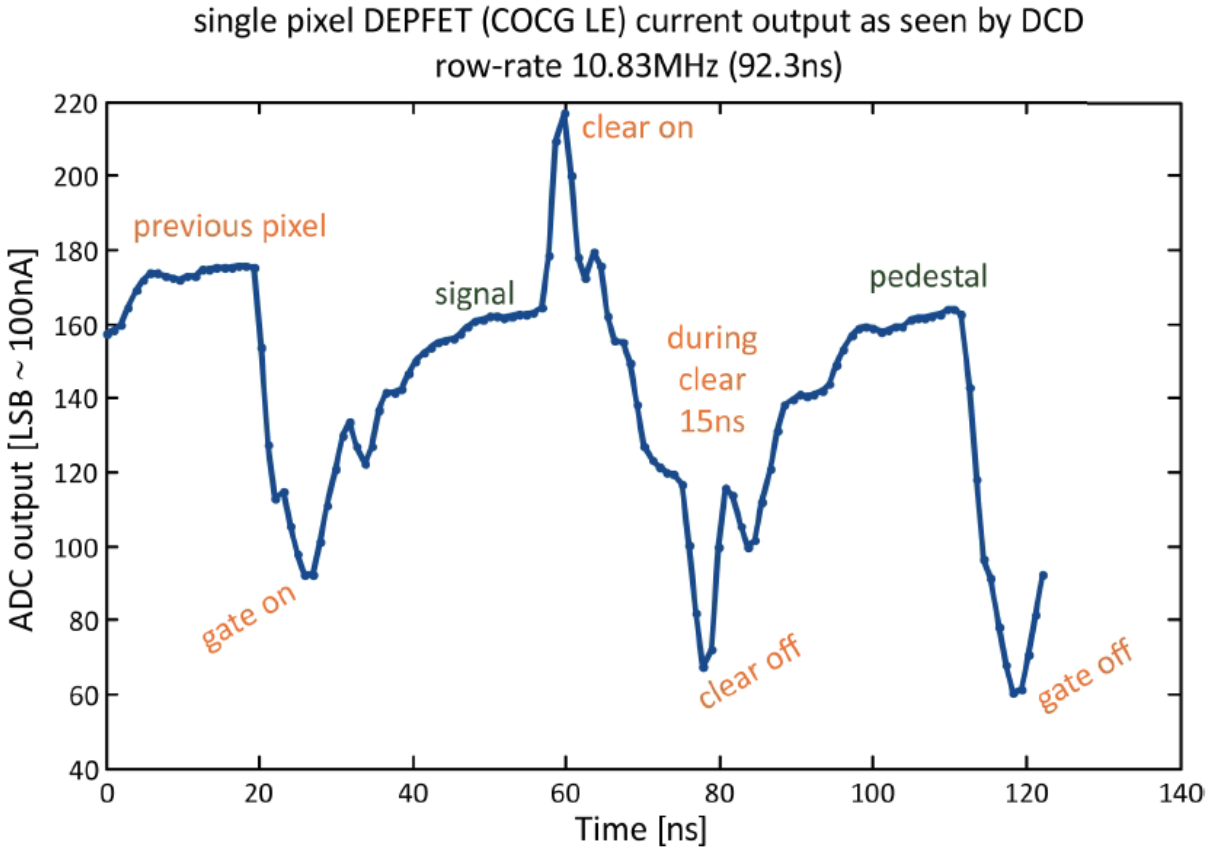
Simulation of the drain current of a DEPFET matrix without parasitic RCs.



Simulation tool: Cadence SpectreCMI, T Gate on = 90ns

Why Parasitic RC Parameter Extraction?

Time resolved DEPFET output current (maximum speed so far)



- no longer good settling behavior!
- sampling steps now 0.96ns

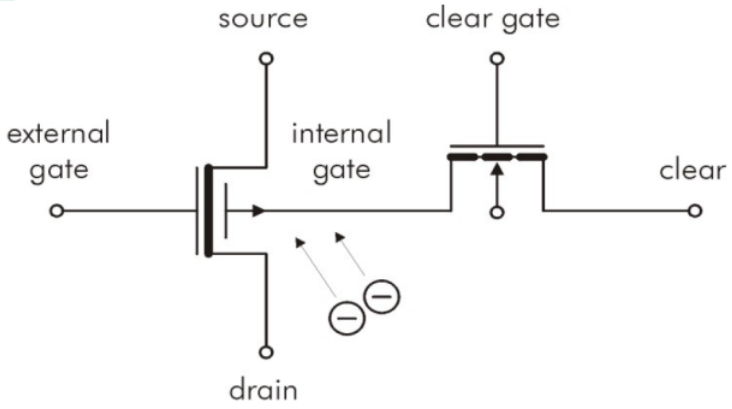
Measurement of a DEPFET matrix by Manuel Koch

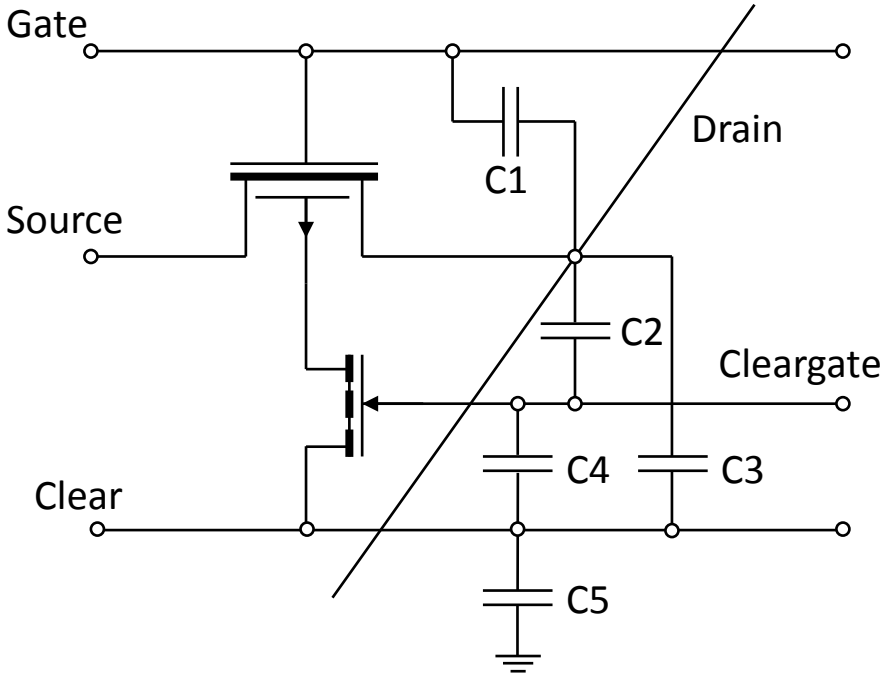
Why Parasitic RC Parameter Extraction?

→ Include coupling to neighboring drain, gate and clear lines

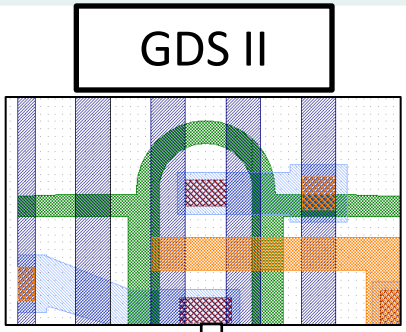
→ Belle-II DEPFET Pixel Matrix will have the dimensions of approx. 1 x 4 cm²

→ Simulation of the different designs options (Capacitive Coupled Cleargate)





Synopsys Raphael RCV + Sentaurus Structure Editor



Process Description

```
DEPOSITION THICKNESS=0.2 MATERIAL=Oxide TYPE=iso
ETCH THICKNESS=0.2 MATERIAL=Oxide TYPE=iso MASK=via1
                POLARITY=NEGATIVE
DEPOSITION THICKNESS=0.4 MATERIAL=Metal TYPE=patterned
                MASK=poly1 POLARITY=POSITIVE
```

APIS

SSE

MESH Generator

Linear Solver

Re-mesh Loop

Charge Calculation

Raphael RCV

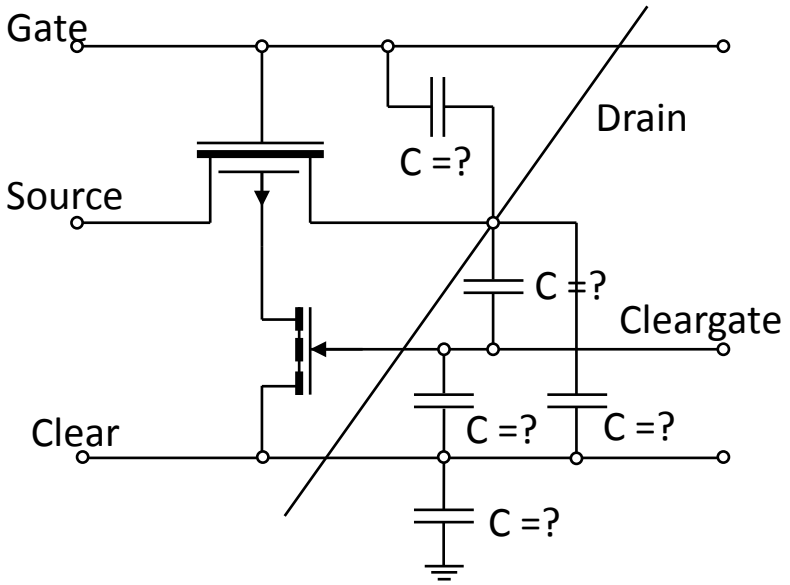
Capacitance Report

APIS= Advanced Parser of Interconnect Structures

SSE = Sentaurus Structure Editor

Capacitance Report

cap label	net1	net2	cap [fF]
C1_0	gate	drain1	31.9
C2_0	gate	drain2	60.3
C3_0	gate	drain3	67.4
C4_0	gate	drain4	63.0
C5_0	gate	drain5	51.6
C6_0	gate	drain6	67.4
C7_0	gate	drain7	60.3
C8_0	gate	drain8	31.9
C9_0	gate	source	28.4
C10_0	gate	clear	53.4
C11_0	gate	cleargate	24.6
C0_g	gate	GND	22.1



Technology Simulation using Sentaurus Structure Editor

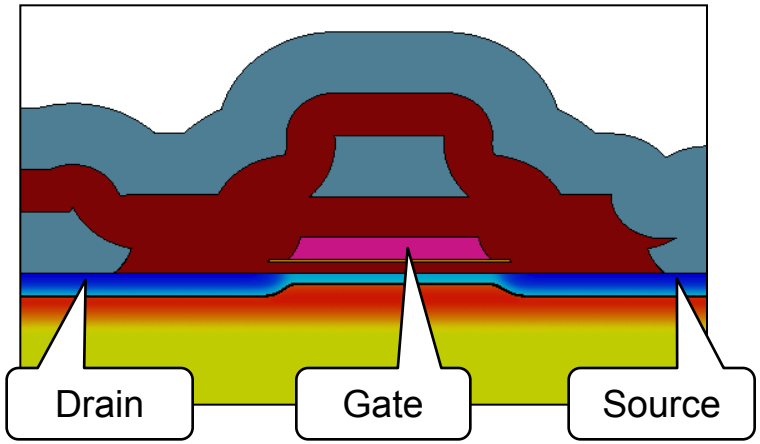
- Double poly/double aluminum process

Process Description

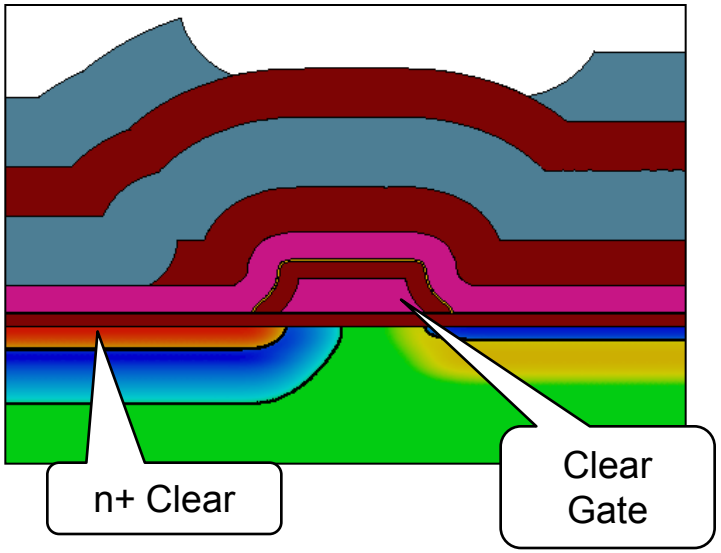
```
DEPOSITION THICKNESS=0.2 MATERIAL=Oxide
           TYPE=iso
DEPOSITION THICKNESS=0.4 MATERIAL=Metal
           TYPE=patterned MASK=poly1
           POLARITY=POSITIVE
DEPOSITION THICKNESS=0.2 MATERIAL=Oxide
           TYPE=iso
DEPOSITION THICKNESS=0.4 MATERIAL=Metal
           TYPE=patterned MASK=poly2
           POLARITY=POSITIVE
DEPOSITION THICKNESS=0.300 MATERIAL=Oxide
           TYPE=iso
ETCH THICKNESS=0.5 MATERIAL=Oxide TYPE=iso
           MASK=via1 POLARITY=NEGATIVE
DEPOSITION THICKNESS=0.4 MATERIAL=Metal
           TYPE=patterned MASK=metal3
           POLARITY=POSITIVE


CAPACITANCE gate drain8 drain7 drain6 drain5 drain4
           drain3 drain2 drain1 source cleargate clear
```

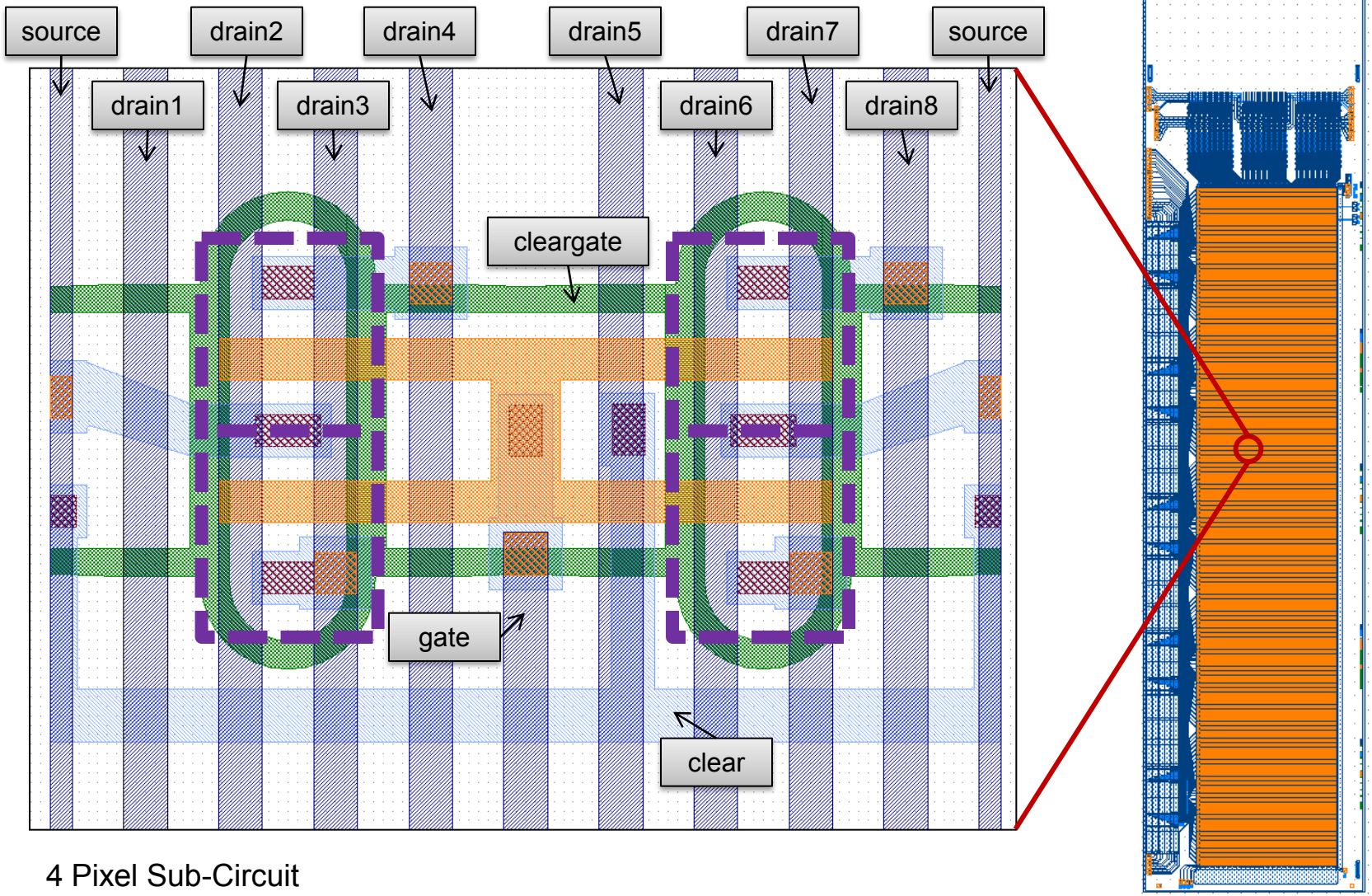
Along P-Channel



Perpendicular to Channel (with CLEAR)

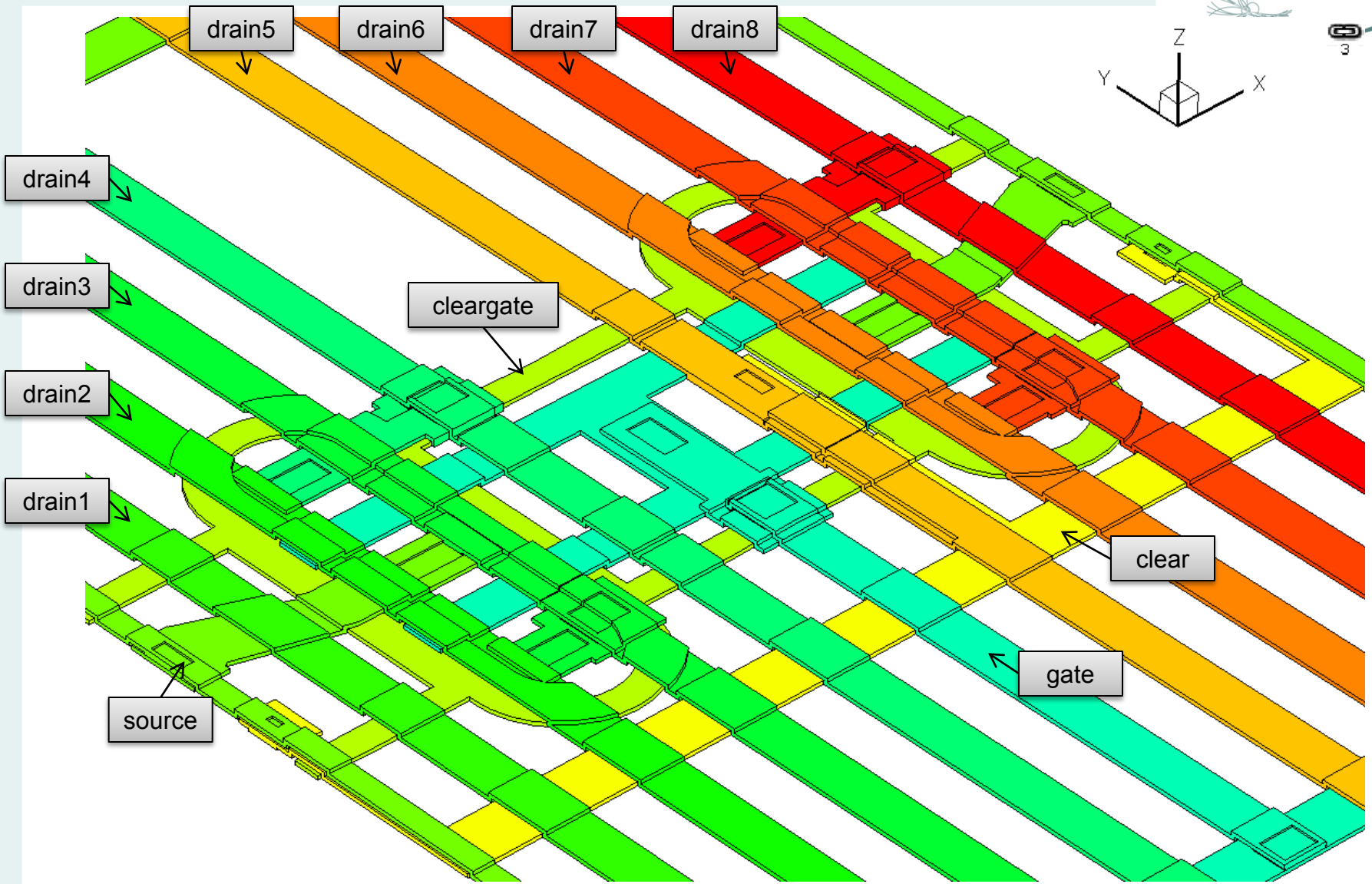


Detail of a DEPFET Layout

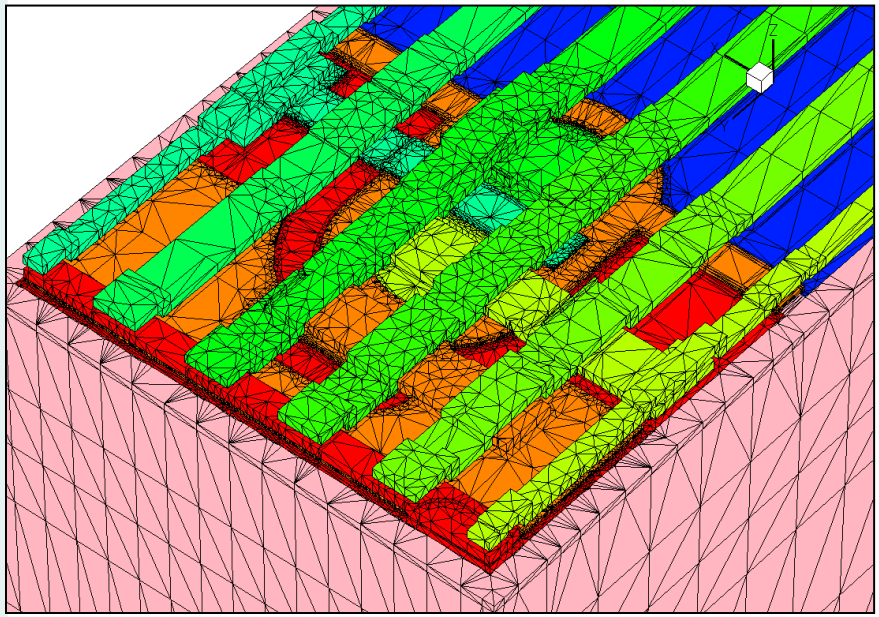


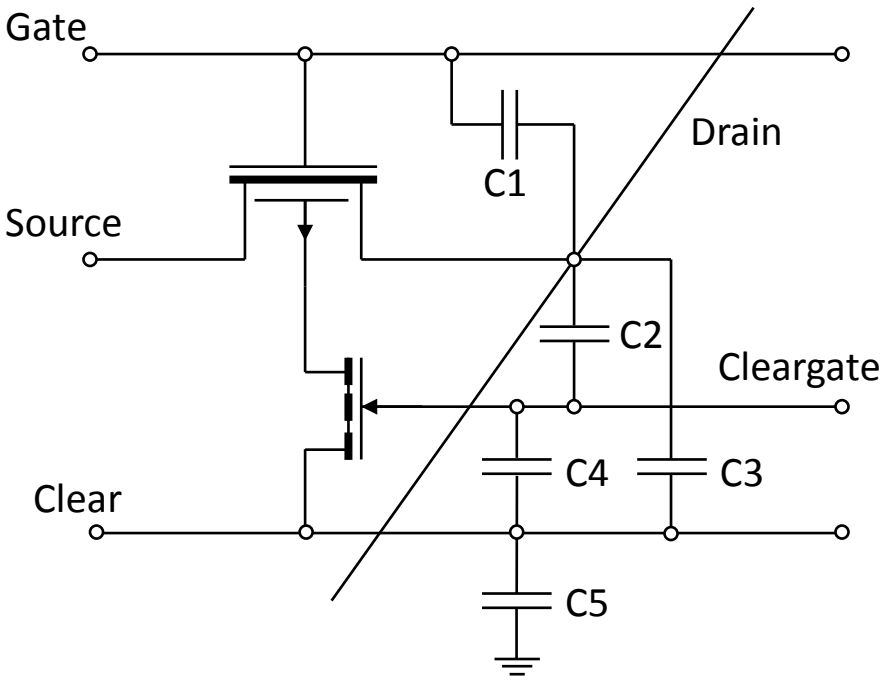
4 Pixel Sub-Circuit

3D Geometrical Model



Results for a Capacitive Coupled Clear Gate Pixel





cap label	net1	net2	cap [fF]
C1	Gate	Drain	8.7
C2	Cleargate	Drain	17
C3	Clear	Drain	4.5
C4	Clear	Cleargate	167
C5	Clear	All except cleargate	56

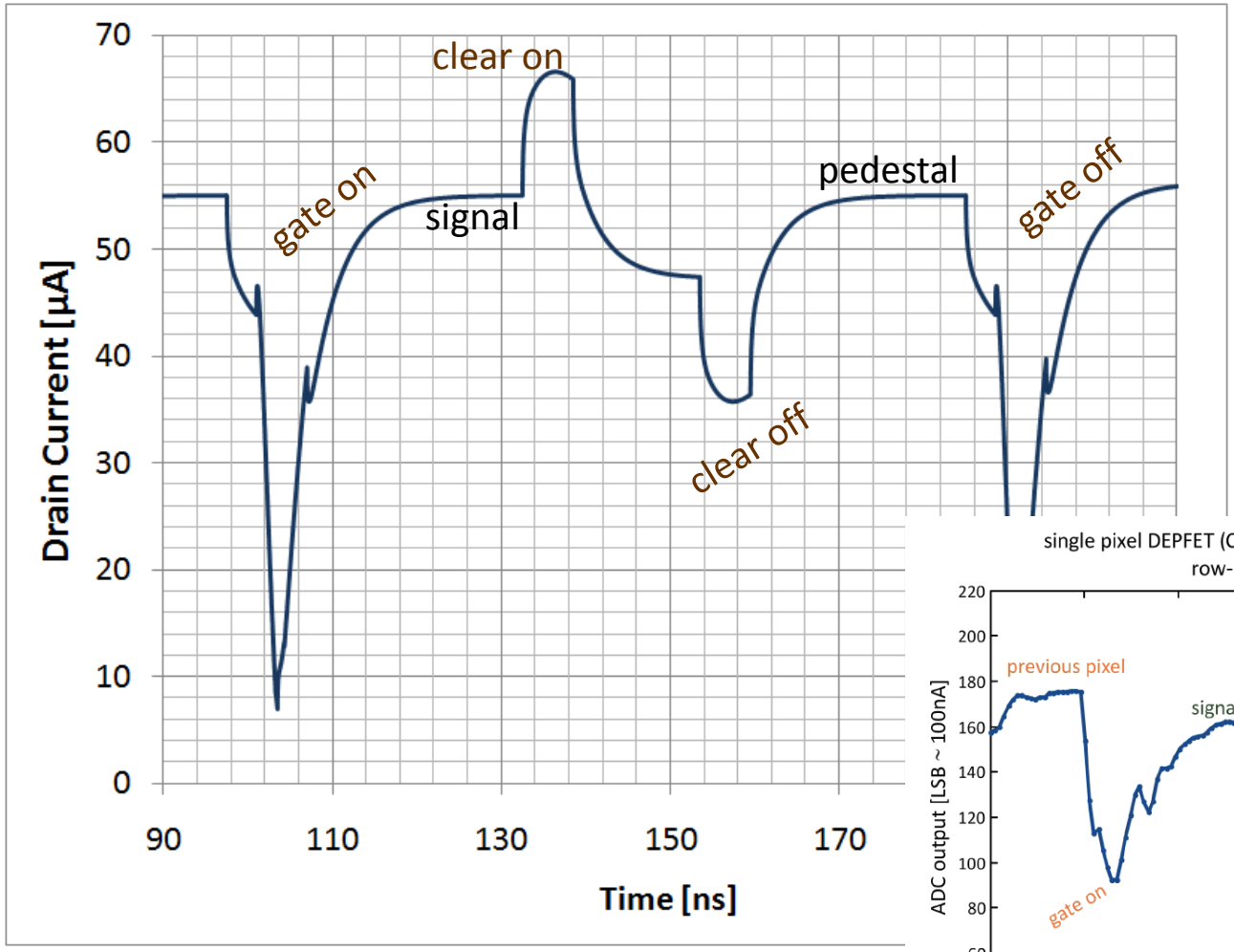
For a pixel array 768x160:

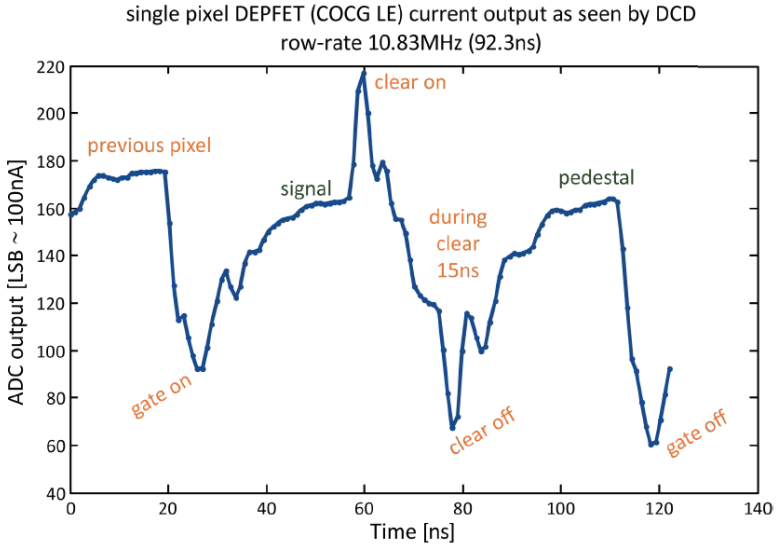
Cclear_array = 100 * 223fF = 22pF

Number of layout cells per row.

DEPFET Matrix Simulation including RC

PRELIMINARY





Summary and Outlook

- Work flow for the extraction of the parasitic RC parameters of DEPFET matrix designs has been established
  - based on layout files
  - including non-planar technology
- Extraction of the Clear-Cleargate capacitance of different design was performed for the current prototype production
- Improvement of the DEPFET model incl. different pixel cell designs and matrix designs is ongoing

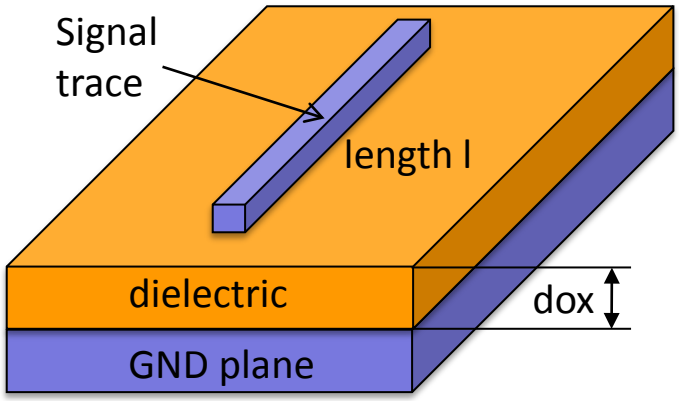
Thank you!

Model Validation

- Validation of the Raphael Simulator using a 2D field simulators shows errors in the 5% range
- Example: 100µm long trace over GND plane with different oxide thickness

$$C = \epsilon_0 \cdot \epsilon_r \cdot \left[1.15 \cdot \left(\frac{w}{dox}\right) + 2.28 \cdot \left(\frac{d}{dox}\right)^{0.222}\right] \cdot l$$

from CMOS Logic Circuit Design, John P. Uyemura.



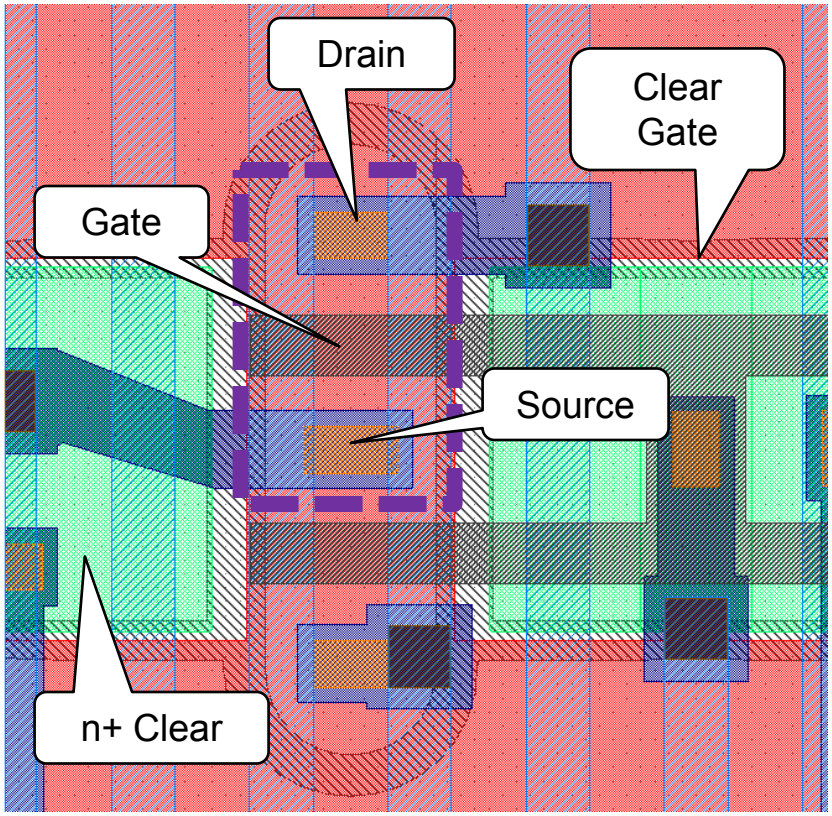
Simulation Result using

Raphael RCV + Sentaurus Structure Editor

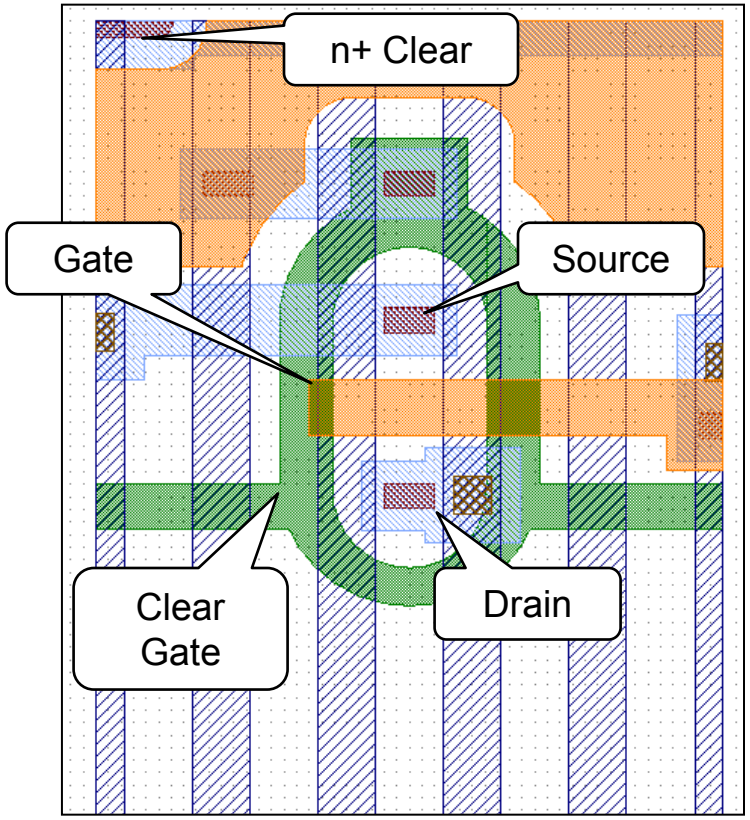
l [µm]	dox [nm]	C_calc [fF]	C_Raphael [fF]	error in %
100	100	52	55	7
100	200	30	33	11
100	400	18	21	12

Examples of DEPFET Pixel Cell Layouts

Common Cleargate DEPFET pixel



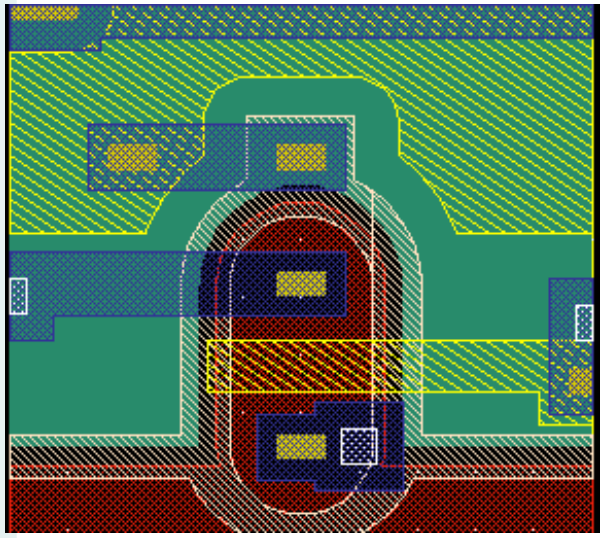
Capacitiv Coupled Cleargate DEPFET



- Small pixel size from 20 x 20µm² to 50 x 75µm²
- High spatial resolution

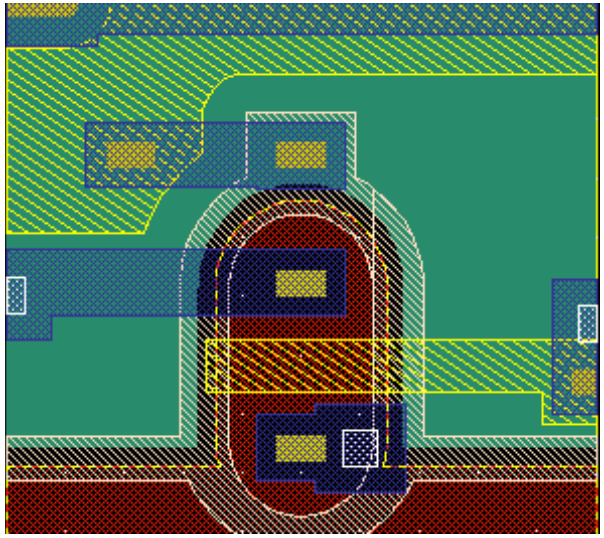
Capacitive Coupled Cleargate Designs

Different Poly2 Layouts for the Cleargate-Clear Capacitor



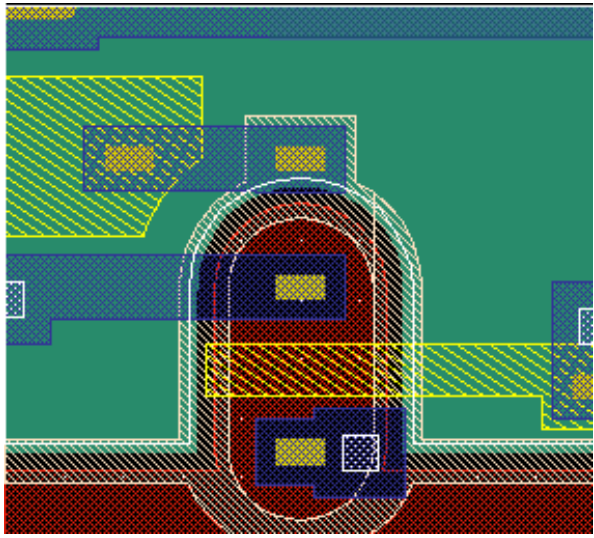
cap_simu_CC_CD_ED_SCG_Z100

Coupling Clear Cleargate: 68%



cap_simu_CC_CD_ED_SCG_Z100_A

Coupling Clear Cleargate: 64%



cap_simu_CC_CD_ED_SCG_Z100_B

Coupling Clear Cleargate: 51%

Spice Model

PRELIMINARY

cap label	net1	net2	cap [F]
C1_0	gate	drain1	3.19E-15
C2_0	gate	drain2	6.03E-15
C3_0	gate	drain3	6.74E-15
C4_0	gate	drain4	6.3E-15
C5_0	gate	drain5	5.16E-15
C6_0	gate	drain6	6.74E-15
C7_0	gate	drain7	6.03E-15
C8_0	gate	drain8	3.19E-15
C9_0	gate	source	2.84E-15
C10_0	gate	clear	5.34E-14
C11_0	gate	cleargate	2.46E-14
C0_g	gate	GND	2.21E-13

For a pixel array 768x160 ST_SD_SCG_Z075:

Cgate_array = 100 * 3.45E-13F = 35pF

DEPFET Pixel and Operation Principle

- based on the combination of the sidewards depletion principle and field effect transistor principle
- charge collection by drift
- detects particles which traverse the substrate of the detector