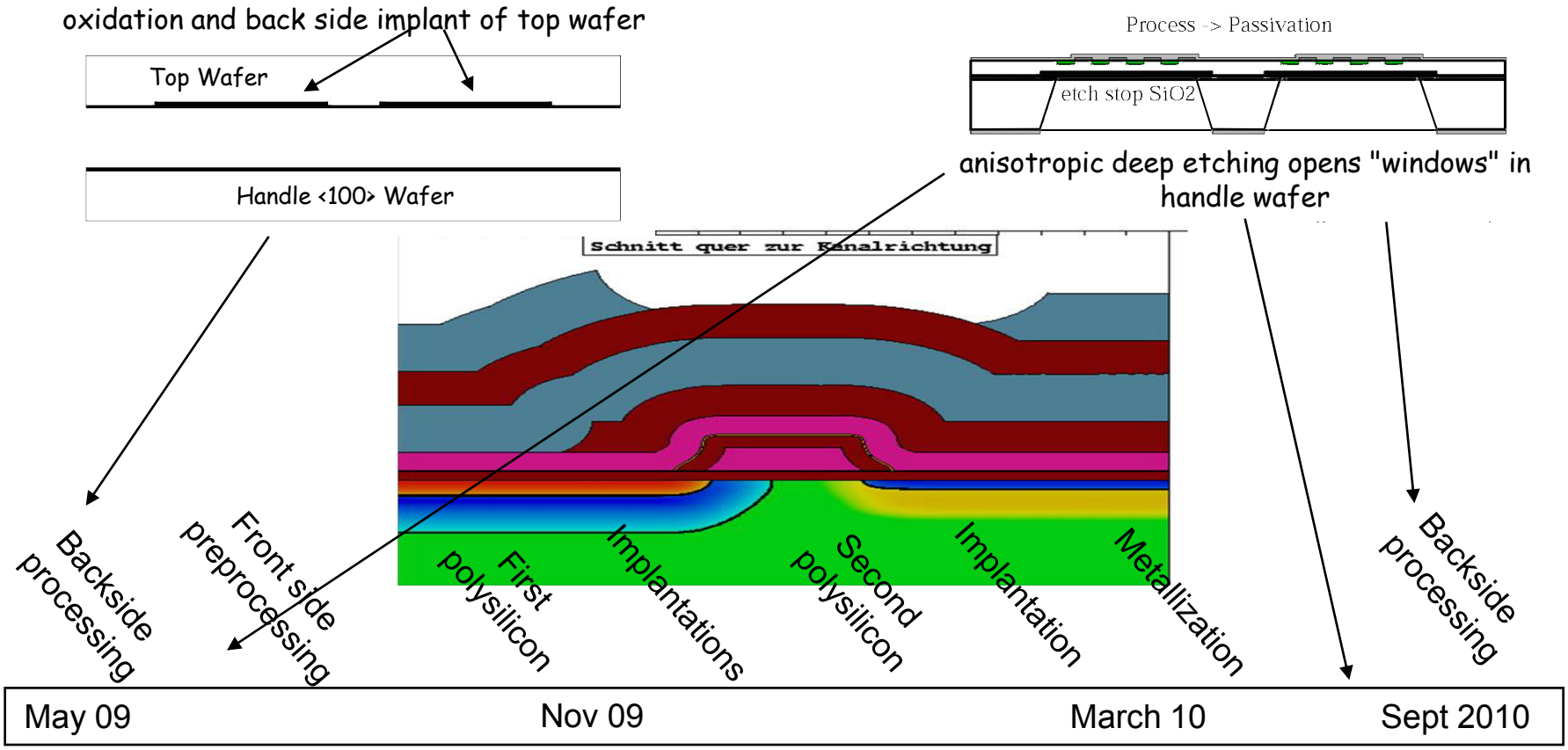
PXD6 Status and Hybrid Boards

Status: PXD6 production

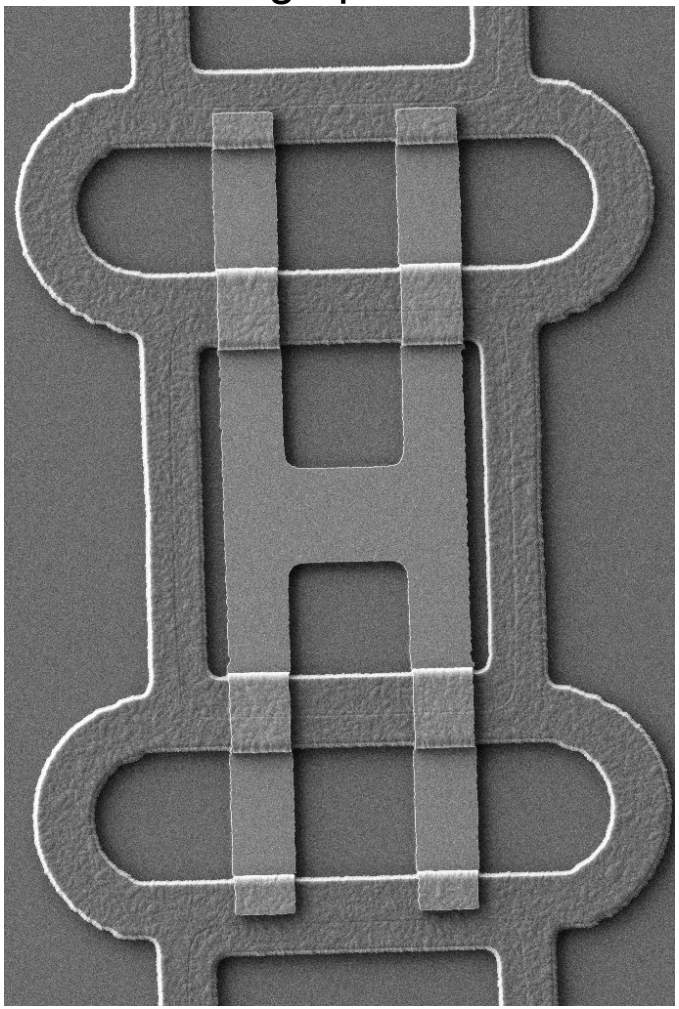
Hybrid Boards

PXD6 - Production status

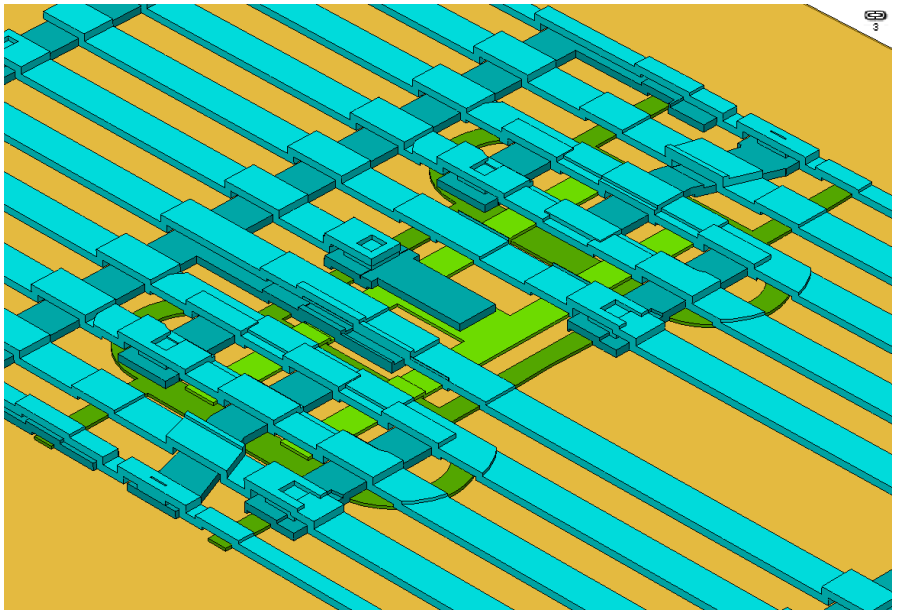


PXD6 status

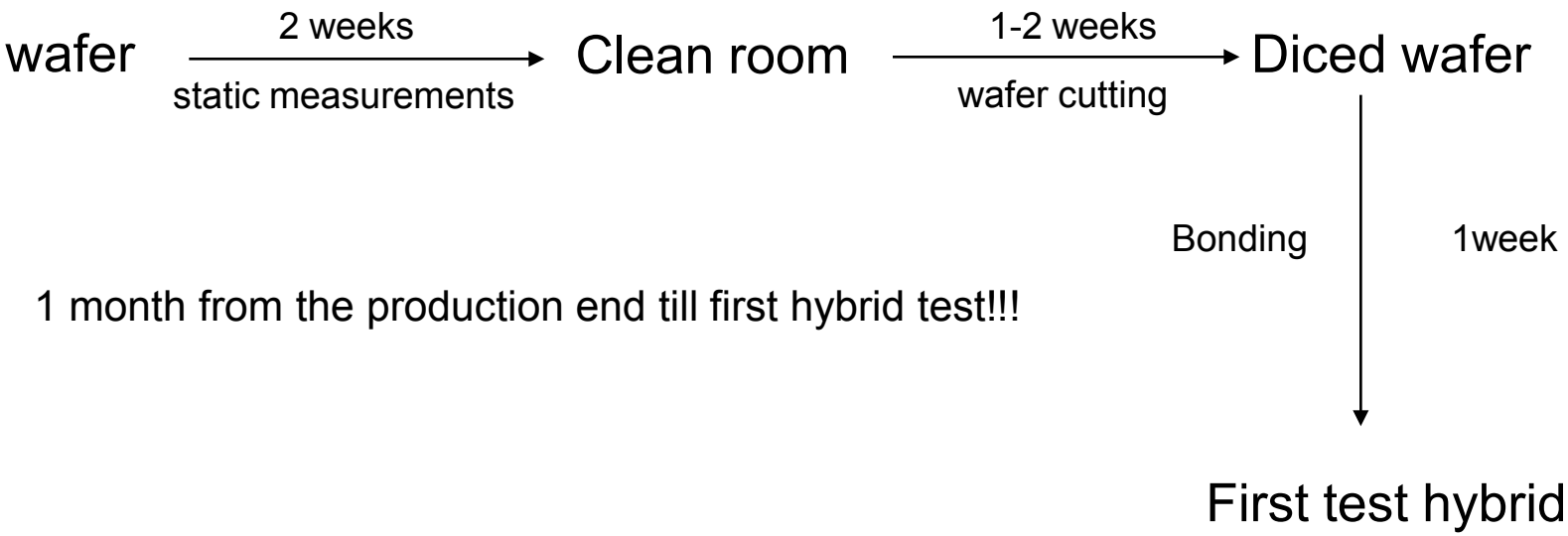
REM micrograph



3D model

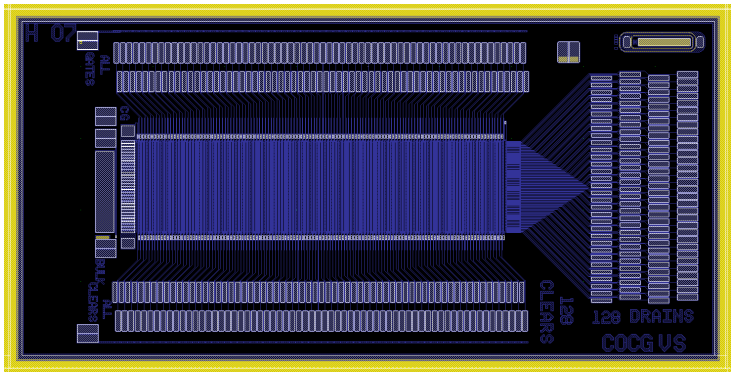


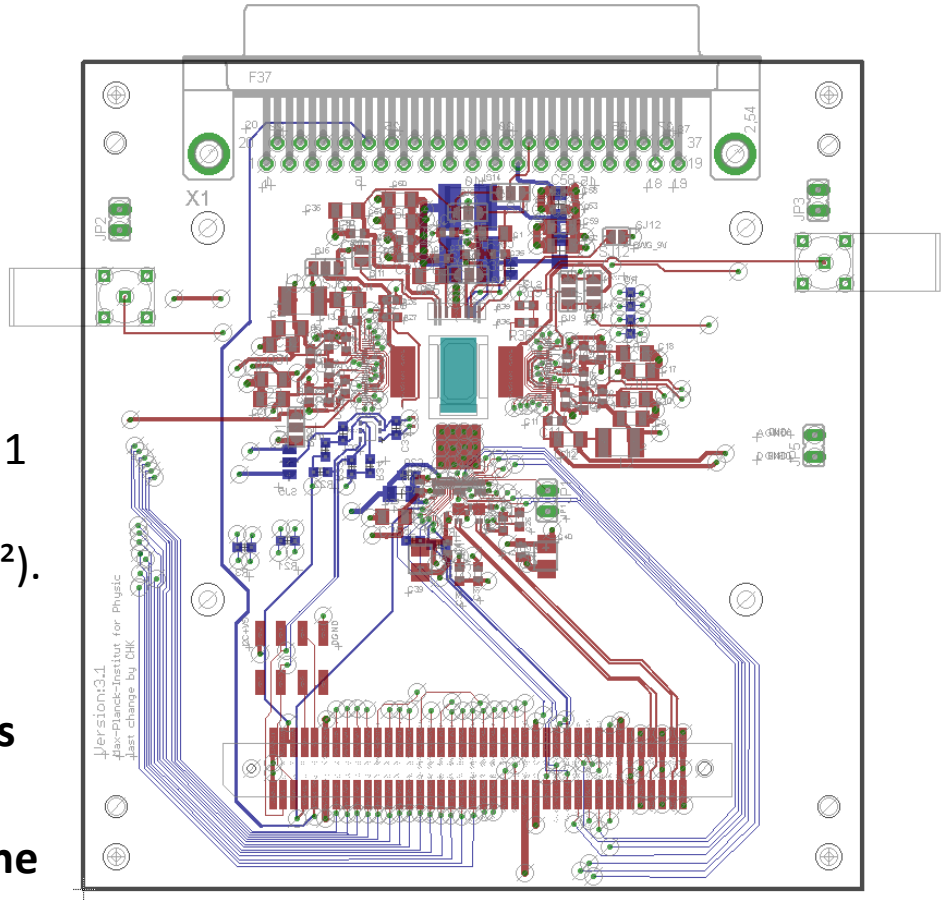
Time schedule



1 month from the production end till first hybrid test!!!

Version 1: PXD6 – ILC Type with Hybrid 3.1 - S3B system (CURO + SW3)





- PXD6 ILC Design can be used with Hybrid 3.1 (electrical identical with Hybrid 3.0 cut-out 4.3 x 9mm² instead of 5.3 x 10 mm²).
- **PXD6 Wafer:**
  - **3 x ILC type (24 x 24 µm² - type used as DUT in TB2009)**
  - **3 x ILC type VS (20 x 20 µm² - type as the best DUT TB2009)**

Version 1: PXD6 – ILC Type with Hybrid 3.1 - S3B system (CURO + SW3)

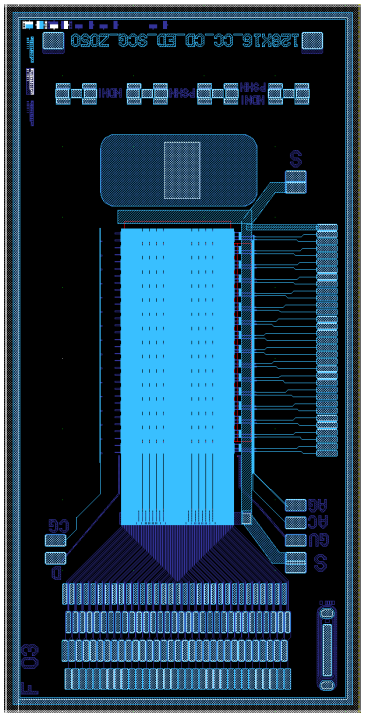
Pro:

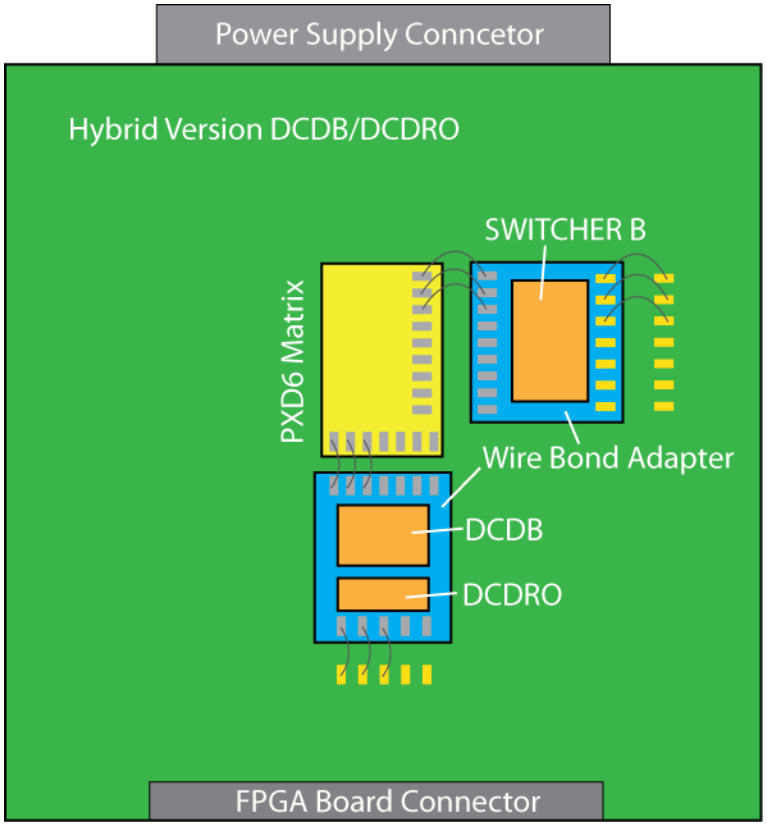
- start with a known matrix design: “ILC type”
- well known system (Hybrid + Power Supply + Readout DAQ)
- proof of principle of thin matrix designs

Contra:

- reduced sensor thickness (50µm) will reduce SNR
  - SNR will only be 1/9 of the PXD5 matrices

Version 2: PXD6 and Hybrid - DCD-B/DCDRO + SWB





- **Design is ongoing**
- DCDB and DCDRO converter chip on one adapter
- SWB on another adapter

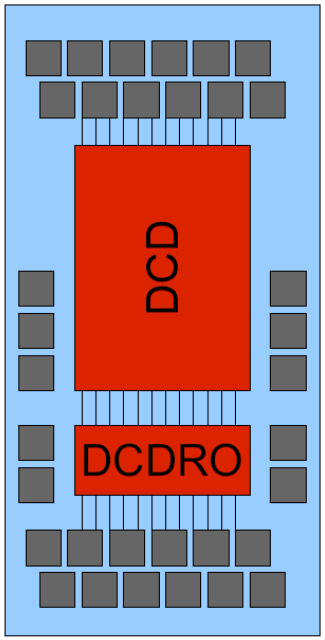
Version 2: PXD6 and Hybrid - DCD-B/DCDRO + SWB

Status:

- redesign of the wire bond adapter for DCD-B/DCDRO and SWITCHER-B

→ due to small pitch of the wire bond pads

→ this design is on-going; wafer for fabrication ready @ HLL (will be the same wafer as for DHP wire bond adapter)



- hybrid design will be finalized as soon as wire bond design is freezed (2 weeks design effort; 6 weeks PCB production)

- schematic is done; same pin assignment as DCD-B/DCDRO single test boards designed by Christian Kreidel

Version 2: PXD6 and Hybrid - DCD-B/DCDRO + SWB

Pro:

- designed for Belle-II matrices
- noise of DCD-B should be less then noise of CURO
- fast readout (300MHz) will be possible

Contra:

- new DAQ software necessary
- Bonn power supplies have to be modified (for use of one DUT bench power supplies can be used)

Version 3: PXD5 and Hybrid – DCD2/SW3

Pro: - boards are available

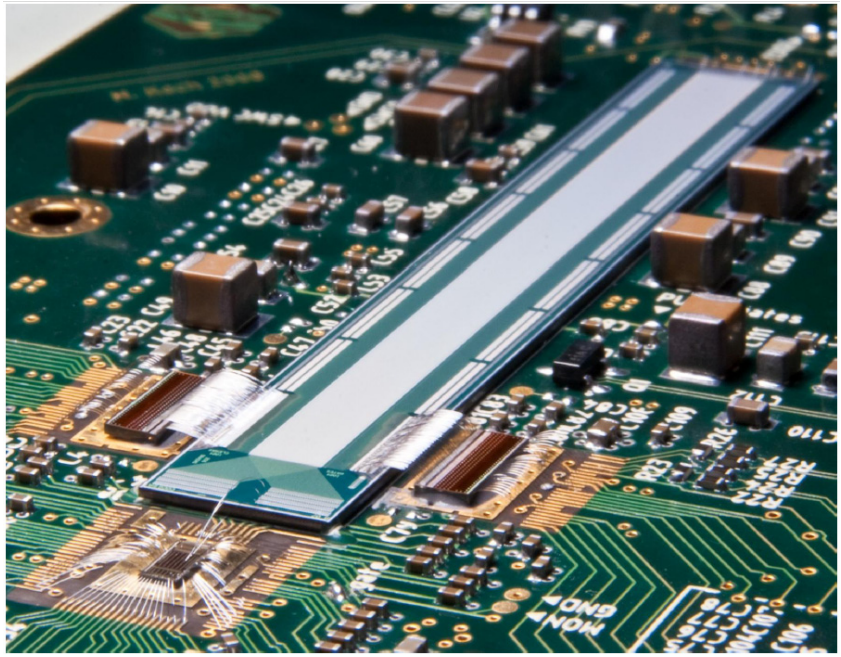
- first long matrix in a test beam

Contra: - only the lower rows can be connected (one SW3)

- only 6 columns are connected

- DAQ is necessary (same as for Version 2)

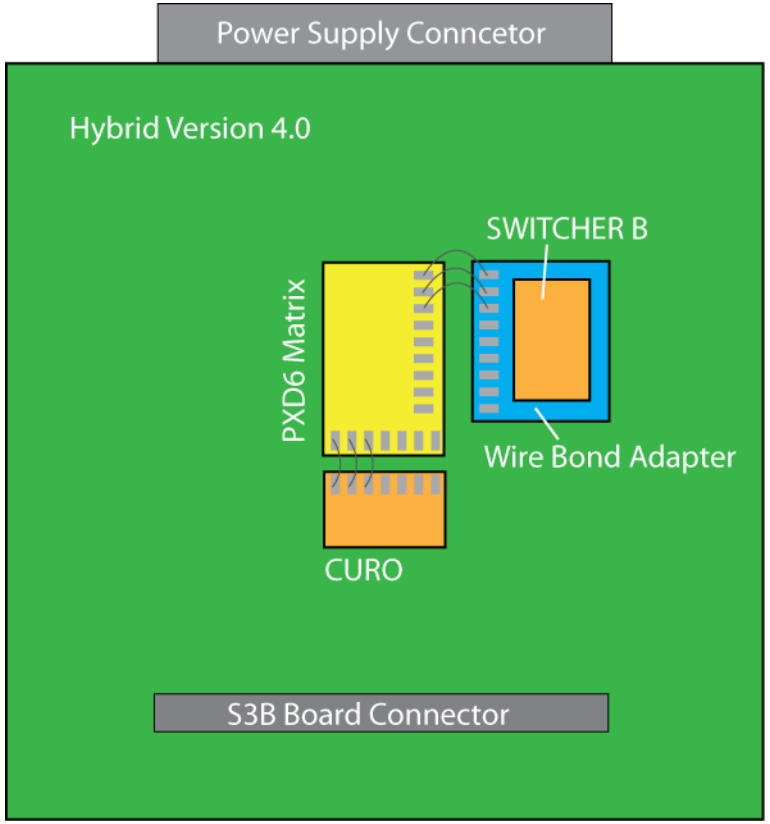
- at the moment bench power supplies are used



Version 4: PXD6 and Hybrid 4.0 for S3B System (CURO & SWB)

- Hybrid 4.0 is a re-design of Hybrid 3.0 with new SWB and CURO

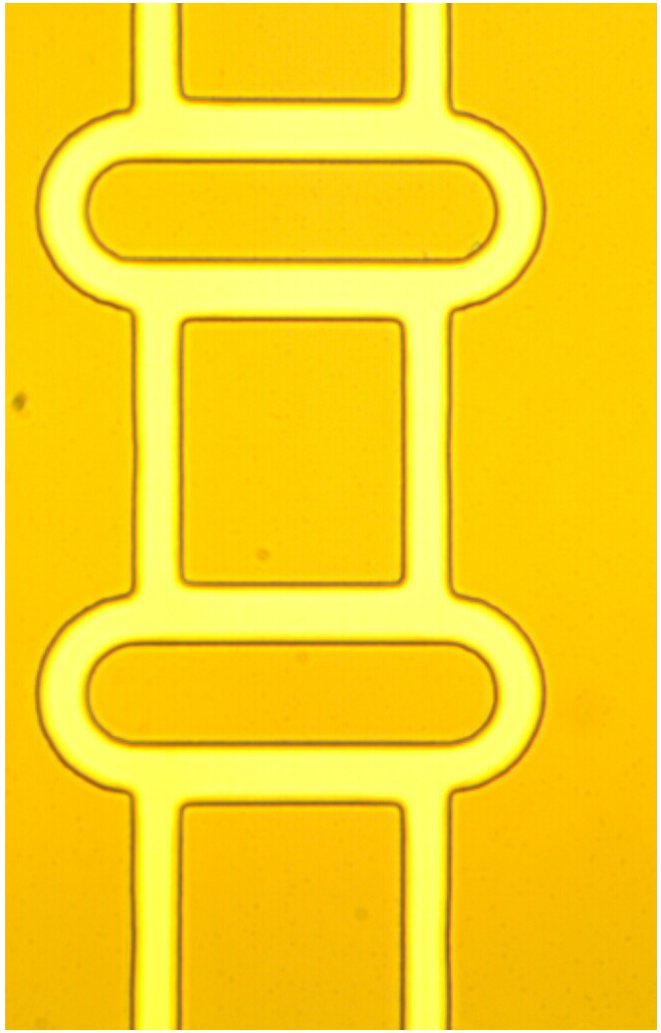
- Minor changes of the current power Supply and DAQ system
  - Power Supply of the SWB (single channel for Clear High/Gate Low – no staggered use of three power supply channels)
  - JTAG Protocol for Slow Control
  - Clear and Gate Sequence (new FPGA firmware)

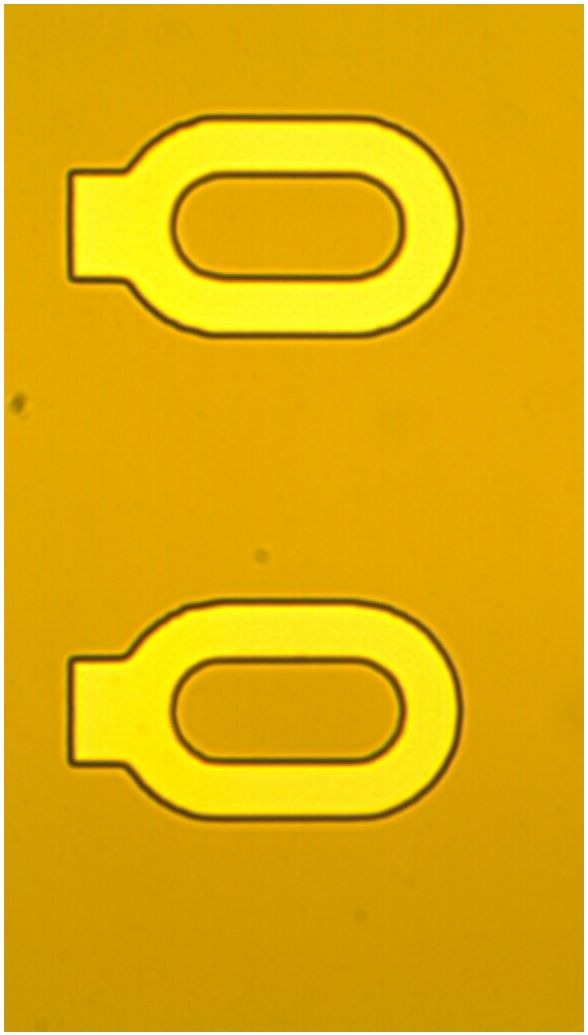


→Only back-up option in case there are problems with DCD-B/DCDRO
No priority at the moment.

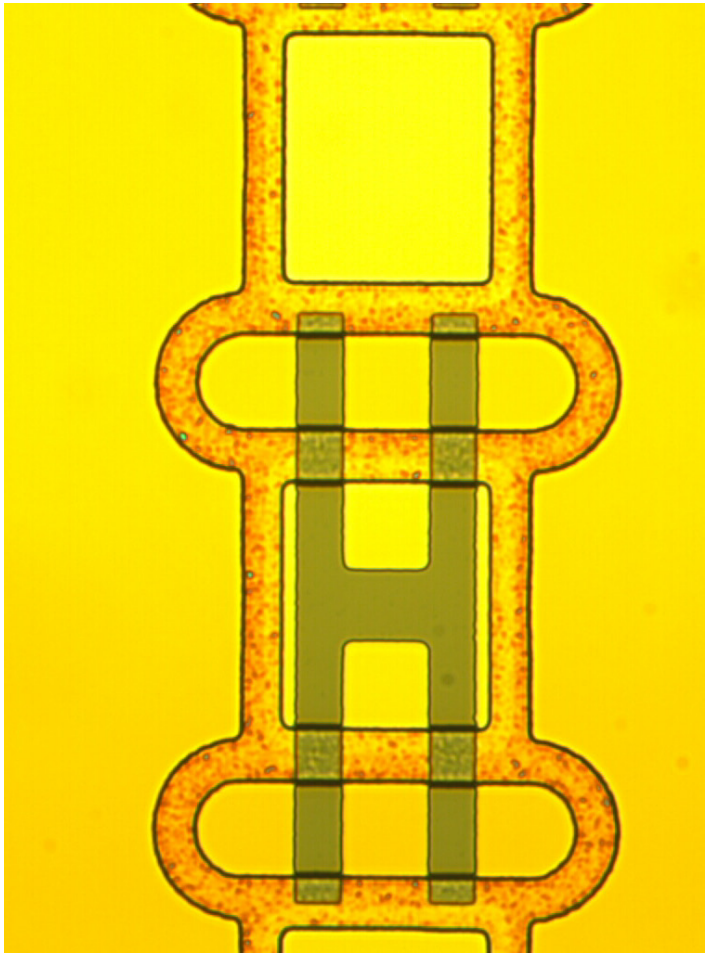
Thank you!

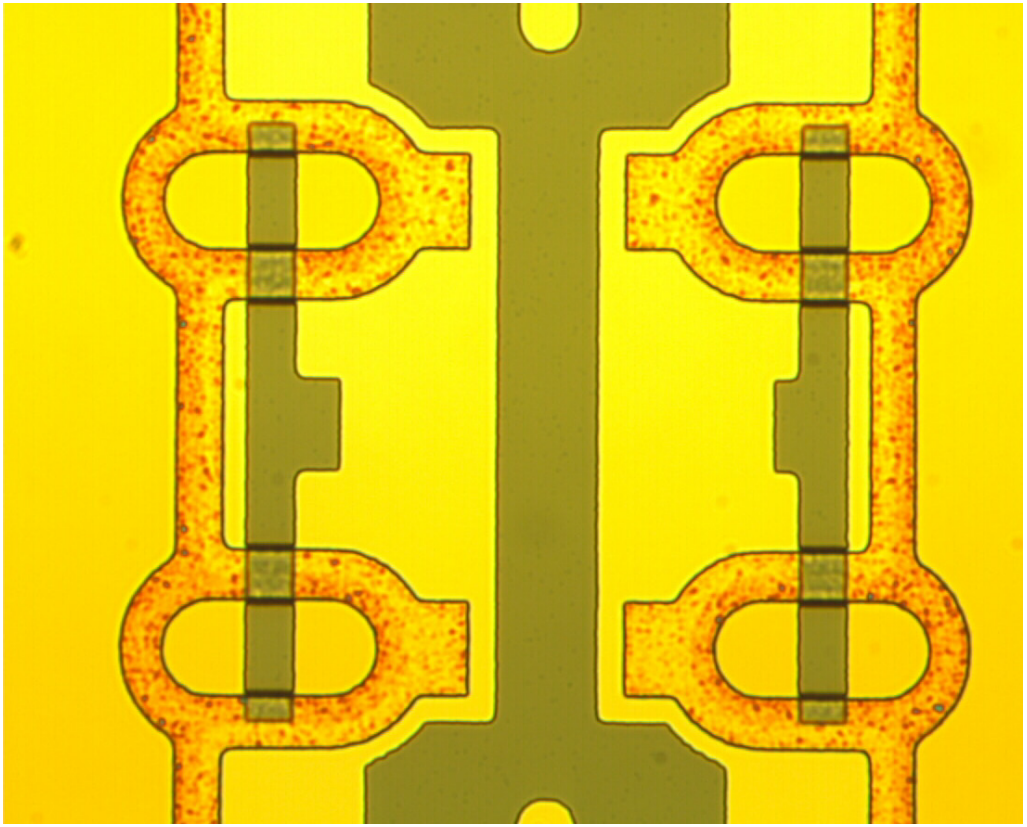
First polysilicon processing for PXD6 (Nov 2009)





Second polysilicon processing for PXD6 before oxidation





Second polysilicon processing for PXD6 after oxidation