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Module Link

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Overview

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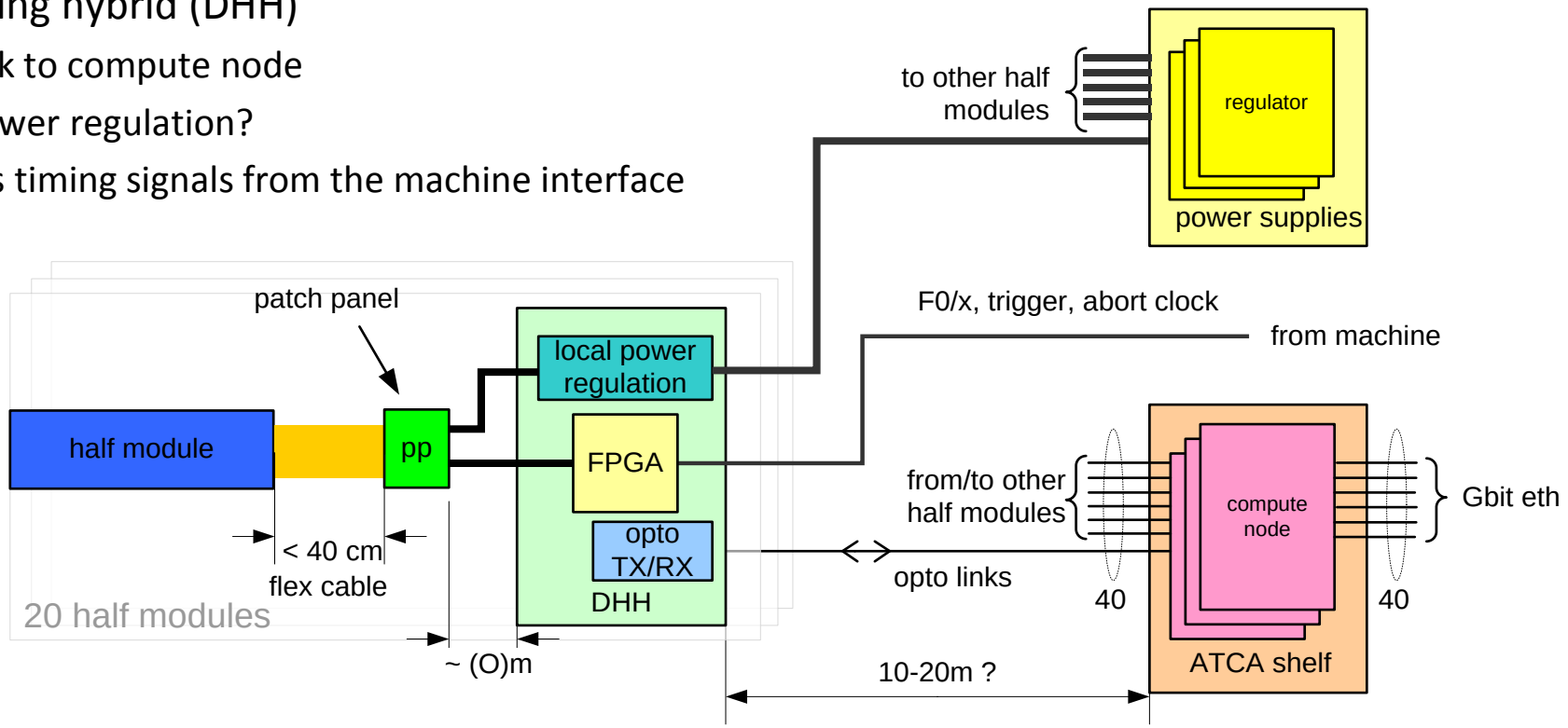
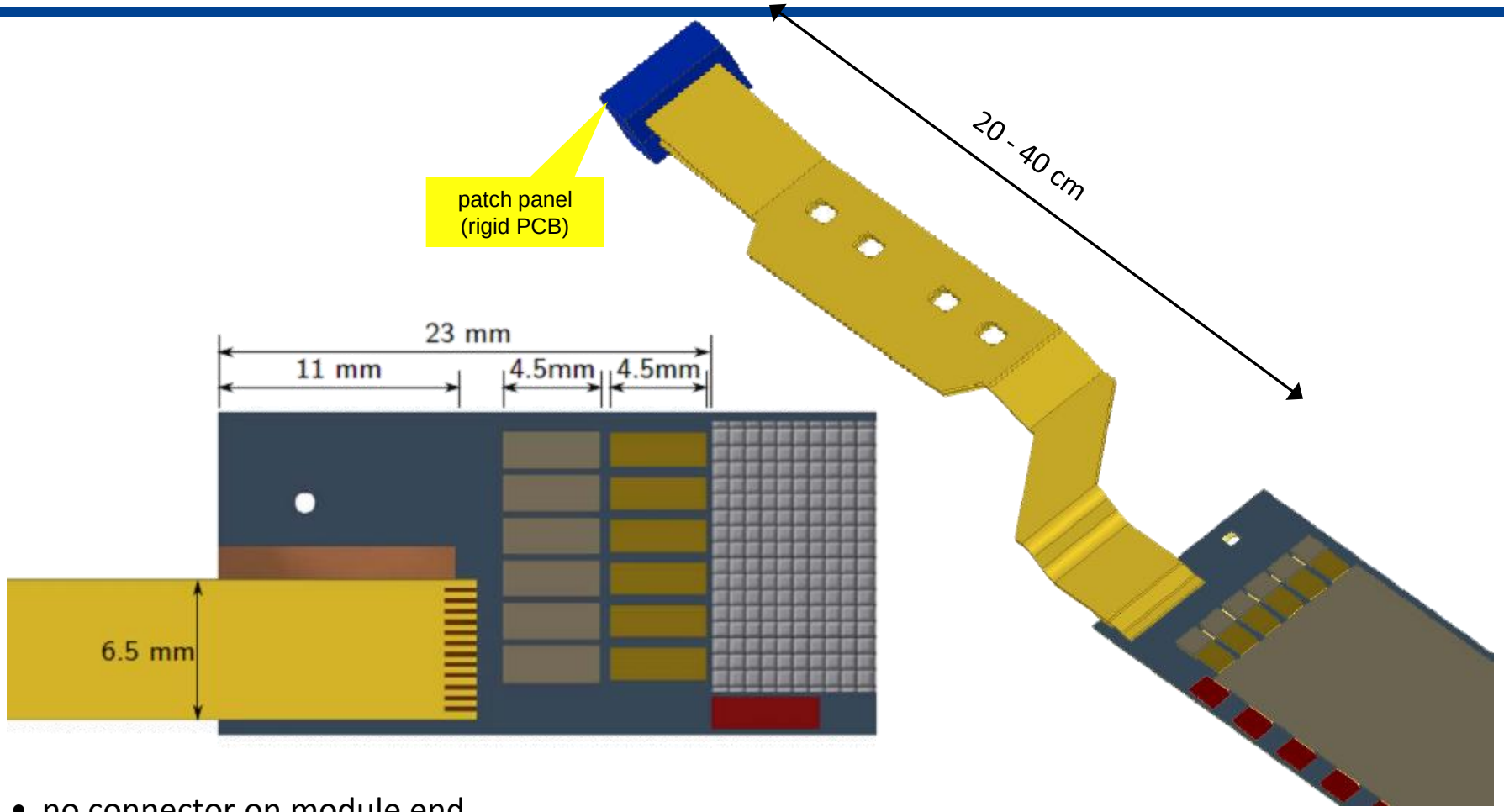
- Requirements & Constraints
  - mechanical, electrical
- Flex kapton design
  - layer stackup
  - TML design
- Signal integrity
  - schematic simulation
- Prototype layouts

DEPFET PXD – Backend Electronic

- flex cable connect modules (power, data, timing)
- patch panel at end of kapton flex
  - data links→ twisted pair cables
  - power lines → larger cross section cables
  - CML repeater/equalizer for Gbit links ?
- data handling hybrid (DHH)
  - opto link to compute node
  - local power regulation?
  - receives timing signals from the machine interface



Mechanical constraints



- no connector on module end
- max flex width: 6.5 mm
- quite complex outer shape

Signal & Power lines

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- Digital signals between DHH and DEPFET module (DHP)

Signal name	Type	Description	Comment
GCK	LVDS in	system clock = 1/8 rowClk (~100 MHz)	generated from RF clock F0 adjusted by additional factor on the DHH
FCK	LVDS in	99.2 kHz frame clock	synchronous to the beam gap
TRG	LVDS in	trigger	10-30 kHz
TMS	LVDS in	JTAG mode select	
TCK	LVDS in	JTAG clock	
TDI	LVDS in	JTAG data in	
TDO	LVDS out	JTAG data out	
RST	LVDS in	reset	for all chips? polarity?!
DO[3:0]	CML out	DHP data out	one per chip

1.25 Gbps

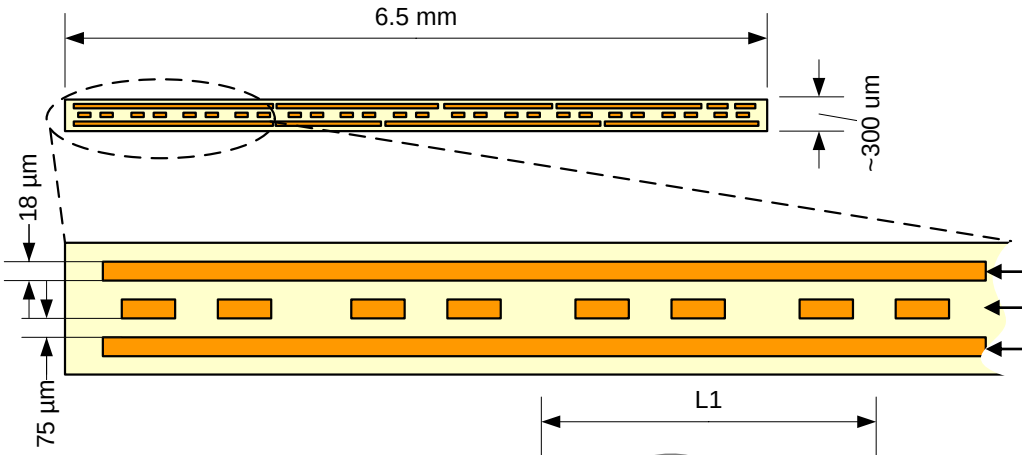
- Power lines
  - DCD (3x analog + digital)
  - DHP (digital IO + core)
  - Switcher (4x analog + digital)
  - DEPFET bias (5x)

Power / bias lines

	name	type	voltage [V]	current [mA]	comment	diff.	thin	thick	width [mm]	voltage drop [V]
power supplies	VDDA	DCD analog	1,8	2300	sense line		1	6	3,48	0,35
DCD	VDDD	DCD digital	1,8	800	sense line				1,21	0,35
	REFIN	DCD analog ref	1,1	100	sense line		1	2	0,15	0,35
	DGND	common digital ground	0	800	common					
	AGND	analog ground	0	2300	sense line		1	6	3,48	0,35
	AMPLOW		0,35	1500	sense line		1	4	2,27	0,35
DHP	VDDIO	DHP IO rail	1,8	100	sense line		1	2	0,15	0,35
	VDDC	DHP core	1,2	500	sense line		1	5	0,76	0,35
	DGND	digital ground	0	600	common					
SWITCHER	VDDS	digital supply	3,3	4				1	0,01	0,35
	DGND	digital ground	0	4	common					
	VJTAG	JTAG IO rail	1,8	4	common					
common	VDDIO	common IO rail + DCD digital	1,8	904	sense line		1	4	1,37	0,35
	DGND	digital ground	0	1404	sense line		1	6	2,12	0,35
bias voltages	Vclear_on	clear on	~17	30			1			
	Vclear_off	clear off	~8	30			1			
	Vgate_on	gate on	~4	30			1			
	Vgate_off	gate off	~13	30			1			
	Vsource	source	7	100			1	1		
	Vccg	common clear gate	~7	0			1			
	Vbulk	bulk	~17	0			1			
	Vguard	gurad ring (edge)	?	0			1			
	Vbias	backplane	-20	0			1			
					signal pins:	24	17	37		
		power current		4956	**total sum:**			78	15,00	

- min. copper width (17µm copper) for ΔU < 0.4 V (10A, 50 cm length): 15 mm
- total flex width (including digital, bias and sense lines): ~24 mm ➔ 3 layer flex, 6 mm wide
- still some safety factor if 35µm instead of 18µm copper for power layers would be used

Proposed layer stackup



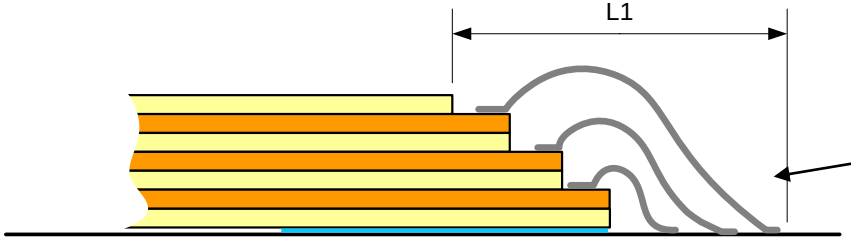
perpendicular cross section a)

cross section zoom in (not to scale) b)

(split) power plane

differential strip lines

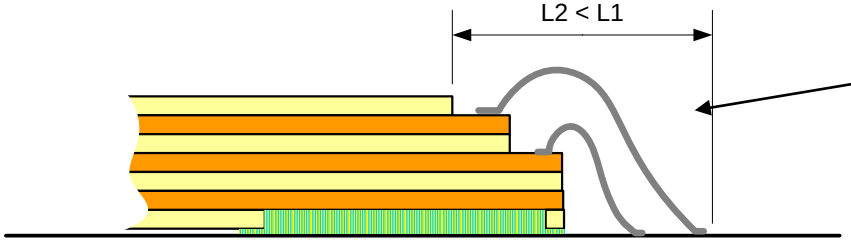
(split) ground plane



c)

three wire bond rows, flex glued to substrate (electr. passive)

longitudinal cross section at module end



d)

alternative option:

two wire bond rows for signal layer and top layer and z-axis glue (or solder or silver epoxy) for bottom layer

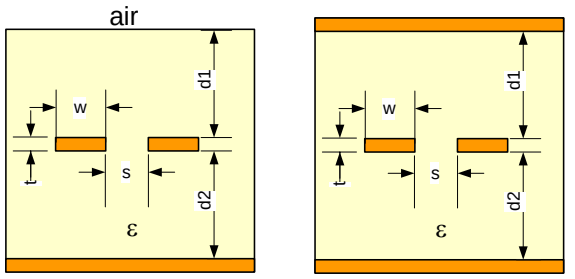
Transmission line calculations

- differential TML variants
  - **d = d1 = d2 = [25, 50, 75] µm**
  - ε = 3.5
  - **s = 100 µm**, **w = [60, 80 100] µm**, t = 18 µm

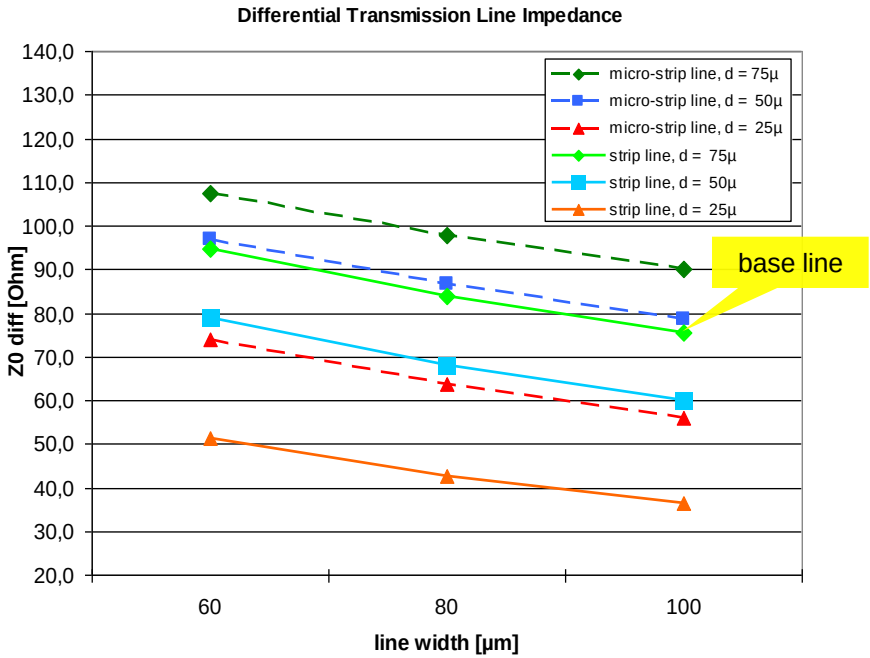
- target: diff. impedance Z_0 = 100 Ω
  - industry standard termination for differential signalling
  - also DHP output driver has 50 Ω single-ended output impedance (could be adjusted to smaller values in future chip versions)

- how to achieve this
  - thick dielectric → overall thickness and cable flexibility
  - thin wires → yield issues, resistive loss
  - micro-strip line gives higher Z_0, but becomes strip line when touching metal parts → impedance discontinuities

- need 50 µm lines strip lines (d = 75 µm) for Z_0 = 100 Ω
  - but min. width = 100 µm, smaller width possible but not recommended (yield, accuracy, resistive loss)



differential micro-strip line differential strip line



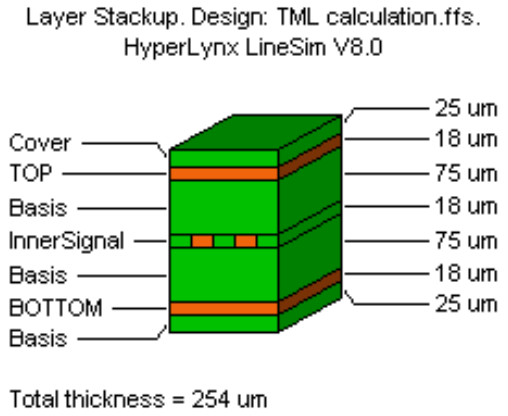
➔ base line: 100 µm width strip line with 75 µm dielectric (Z_0 = 74.5 Ω)

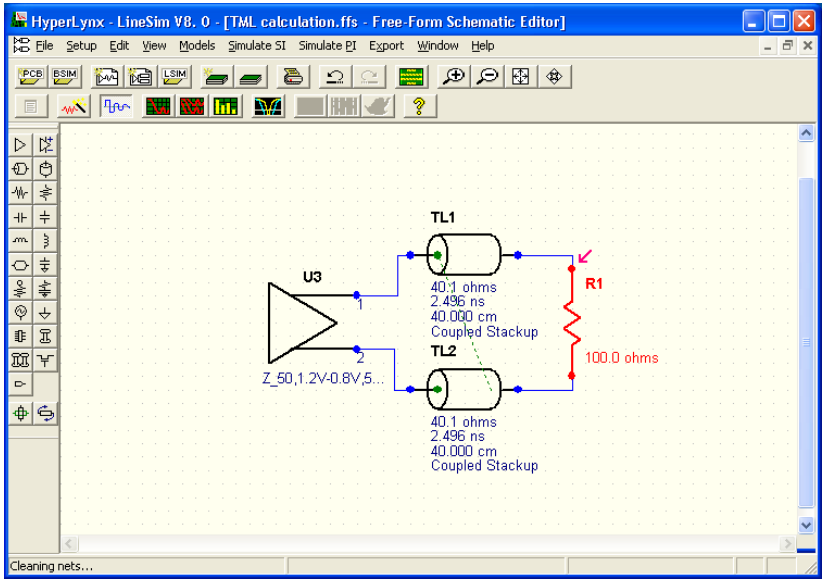
Signal integrity simulation basics

- Simulation tool (HyperLynx, Mentor Graphics)
  - schematic based: TML model from layer stackup
  - layout based: TML model from imported PCB layout

- TML implementation
  - dielectric layer thickness d1 = d2 = 75 µm
  - dielectric constant ε = 3.5
  - spacing 100 µm, line width 100 µm
  - signal layer thickness 18 µm
  - ➔ Z_0 s.e. = 40.1 Ω, Z_0 diff = 75.4 Ω

- simplified driver model
  - single ended output impedance: 50 Ω
    + 1 pF parallel and 2 nH series parasitics
  - rise time: 50 ps (ideal ramp)
  - output levels: 0.8 – 1.2 V



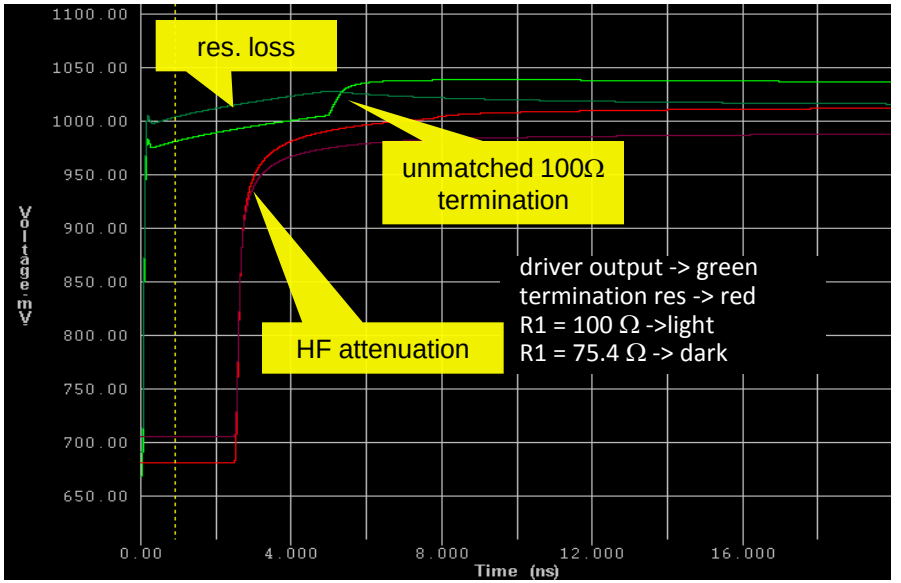


Signal integrity simulation basics (contd.)

time-domain reflectometry (TDR)

- input: ideal voltage step
- output: reflected signal measured at the driver
- resolves spatial resolution of line impedance

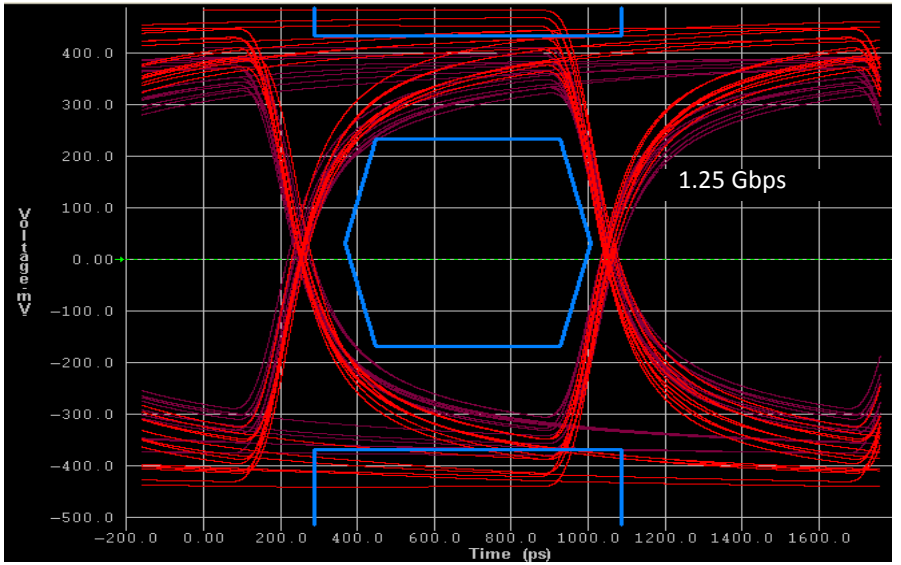
➔ optimize layout: find & resolve impedance discontinuities (vias, connectors…)



eye diagram

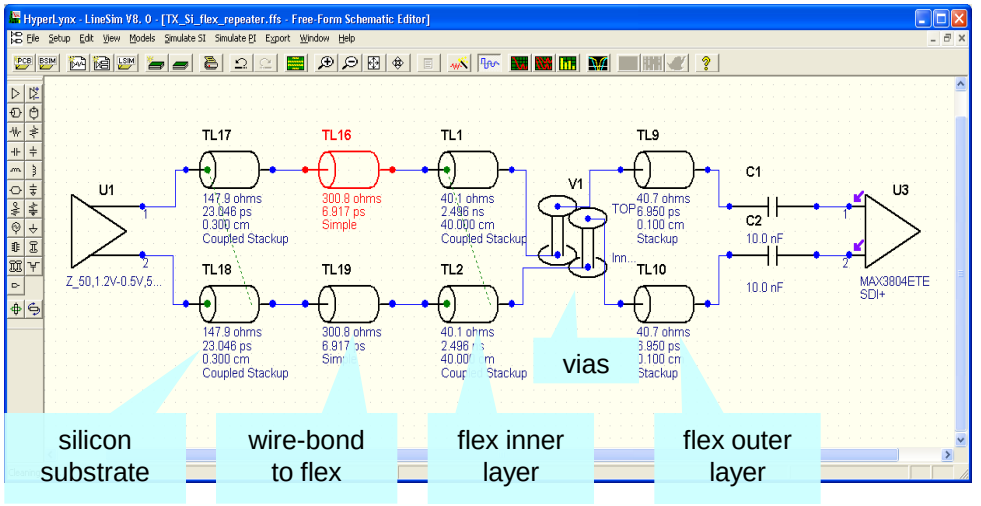
- input: pseudo random bit sequence (PRBS) or 8b/10b patterns
- output: overlay of waveforms at the receiver triggered with the bit clock
- measure eye opening
  - vertical: minimum differential receiver input voltage
  - horizontal: maximum timing jitter (deterministic + random)

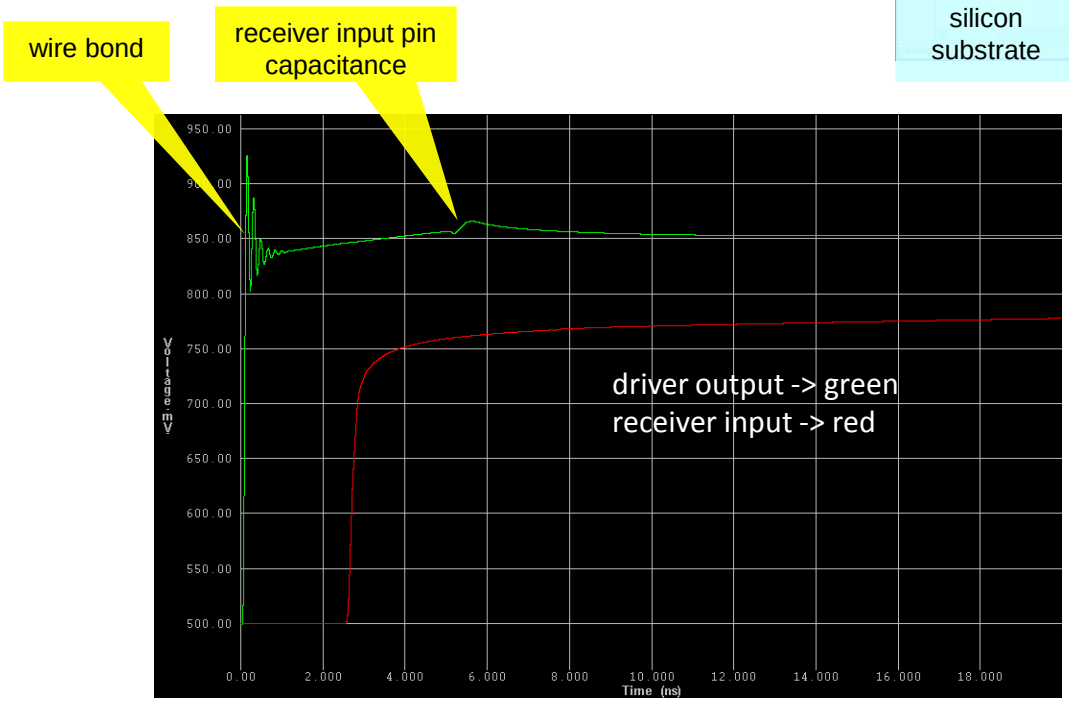
➔ estimate bit error rate

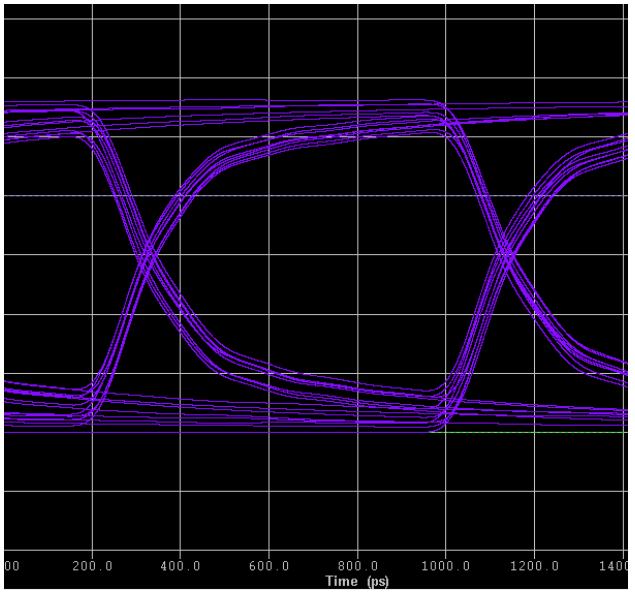


Signal integrity simulation – advanced design

- real design more complicated
  - DHP driver (ESD, pad, bump bond → generate IBIS model, tbd.)
  - silicon substrate
  - wire bond to flex
  - flex (✓)
  - via (✓)
  - receiver ICs (✓, IBIS models from vendor)



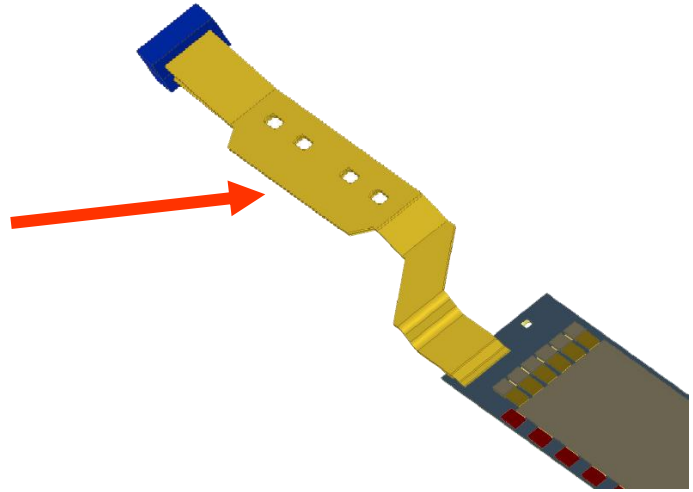




Signal integrity simulation - outlook

work in progress:

- define simulation model for DHP CML driver
- layer stackup for routing on silicon substrate (2 or 3 metal layers)
- simulate different receiver components
  - repeater ICs
  - TWP or coax cables (for passive patch panel option)
- board level simulation
  - import flex design and re-simulate
  - will be important for designs with complex flex outline



Flex link prototype design

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- simulations are good – but measurements are better…

- what do we want to test & measure?
  1. line impedance (process tolerance), attenuation
  2. repeater performance (max. cable length, radiation tolerance)
  3. flex attachment to the substrate (wire bonding & gluing)
  4. data transmission with DHP 0.1

- flex designs variants (20 – 30 cm)
  - A) differential line pairs with variations line width & spacing, both sides with WB balcony
  - B) flex with rigid PCB on one side (patch panel) comprising supporting different commercial board equalizer chips (repeater) and different connectors (SMA, RJ-45…)
  - C) same as B) but with one repeater only plus external connectors for support of all DHP 0.1 signals + power → DHP 0.1 test system

Prototype flex designs variants

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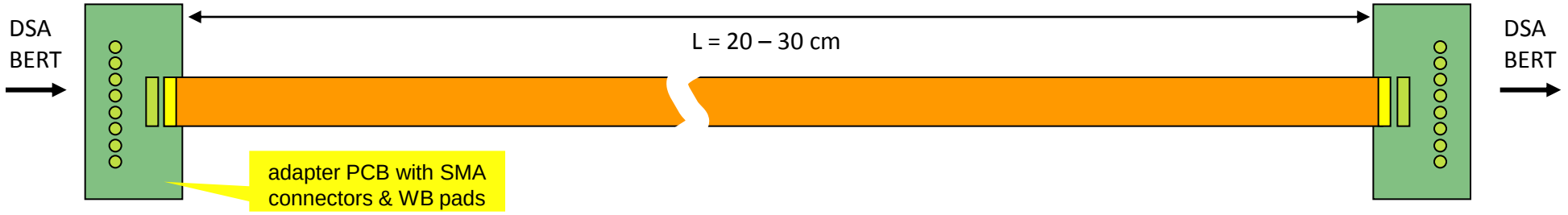
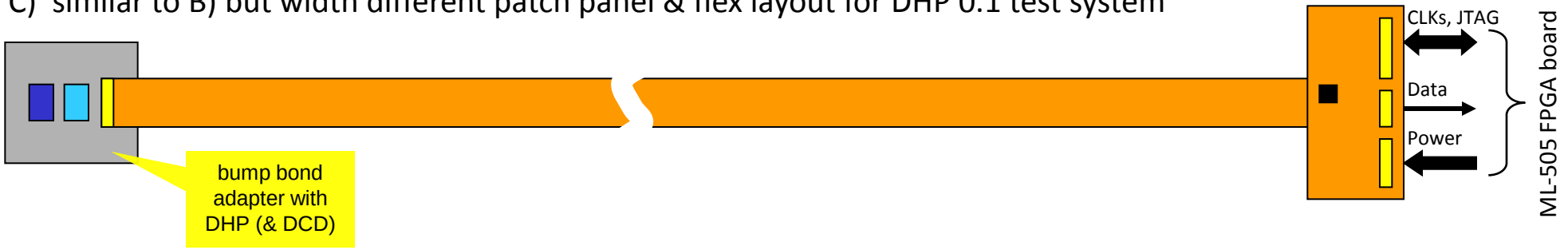
A) diff. TML pairs with line width / spacing variations, WB balcony on both ends

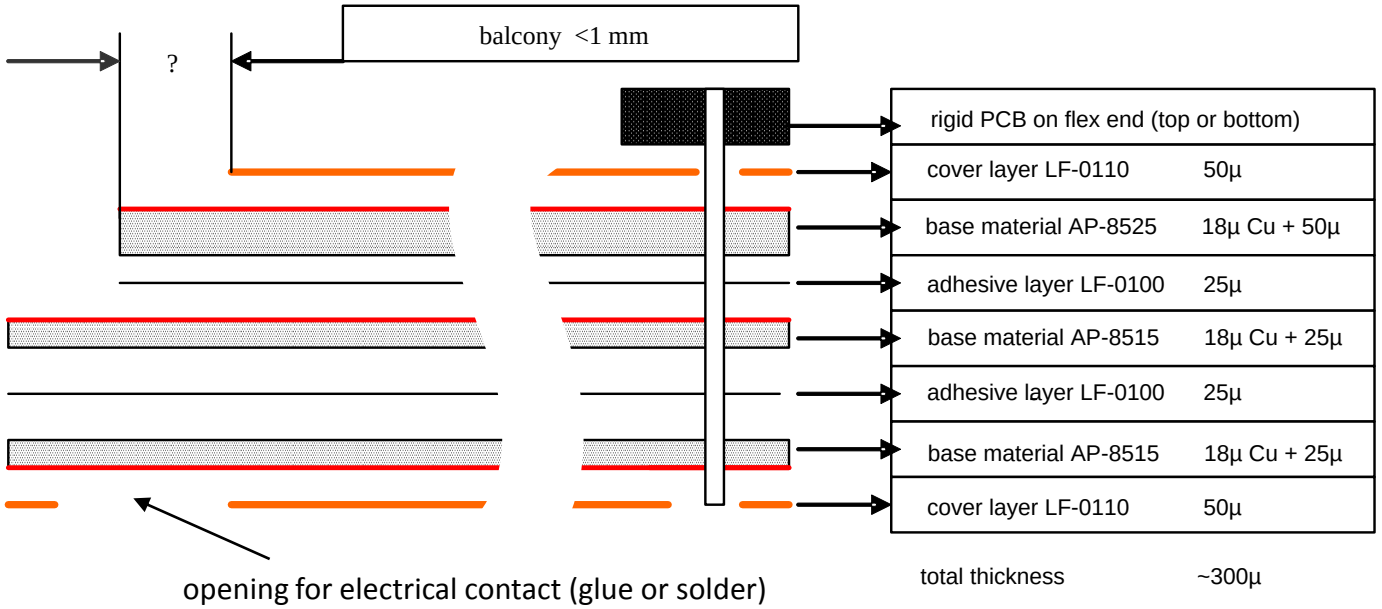


B) diff. TML pairs, patch panel on one side with different board equalizer ICs (repeaters) + connectors

C) similar to B) but width different patch panel & flex layout for DHP 0.1 test system



Layer stackup for test flex



- design rules (for 18µm copper):
  - 100µm line width & spacing (80µ line width?)
  - 200µm/400µm via hole/outer ring diameter
  - dielectric constant: 3.4 – 3.6 for all isolation layers
- 75µm dielectric above and below the (inner) signal layer
- bottom layer “upside-down” for glue attach area

Summary

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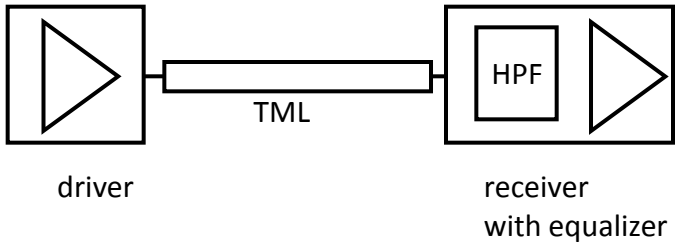
- (initial) definition of flex design parameters
  - power & signal requirements
  - layer stackup
  - TML parameter
- started signal integrity analysis
- design of prototype flex structures ongoing (production planned for end of March)
  - high speed link test bench: DSA, BERT
- did not touch:
  - power issues
  - connection from patch panel to DHH
- other groups (URL, TUM…) are welcome to join in for the final design

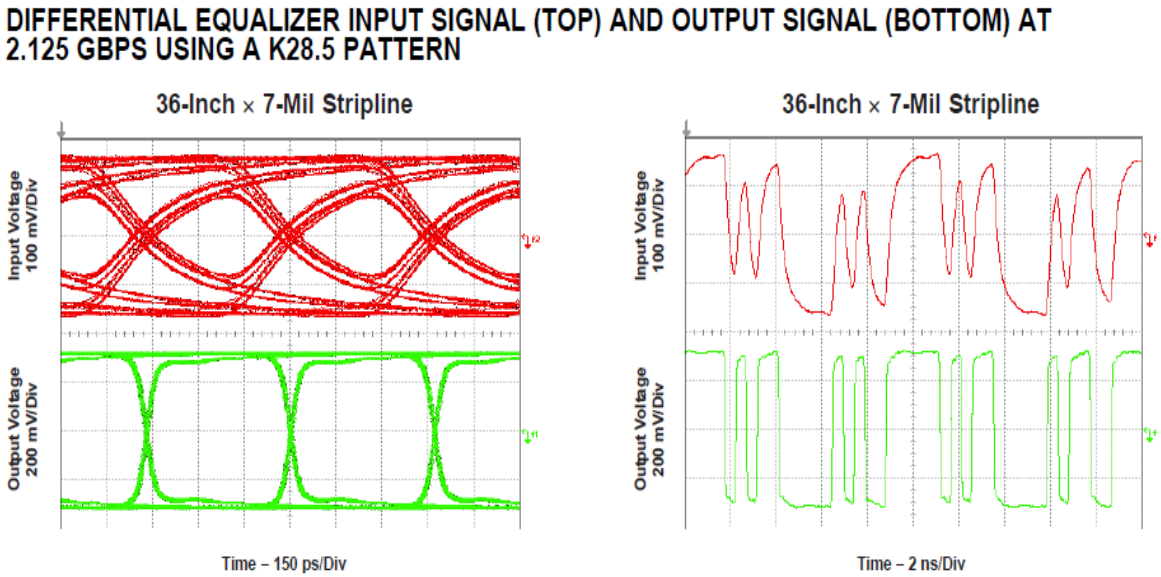
backup

Board equalizer

- basic operation principle: compensate low pass characteristic of TML with matched high pass filter at input of the receiver (active filter)
  - fixed high frequency boost or programmable or adaptive → compare input frequency spectrum with ideal (white) spectrum and adjust filter coefficients accordingly
  - alternative: add HF boost at driver output (pre-emphasis)



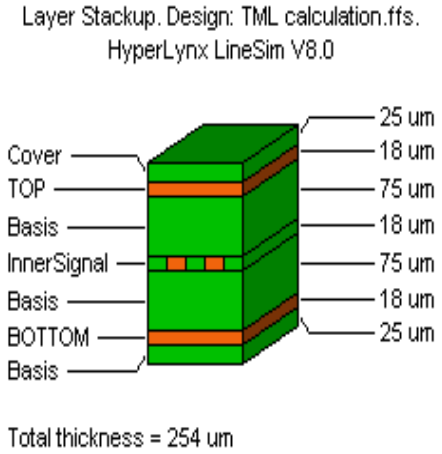
block diagram



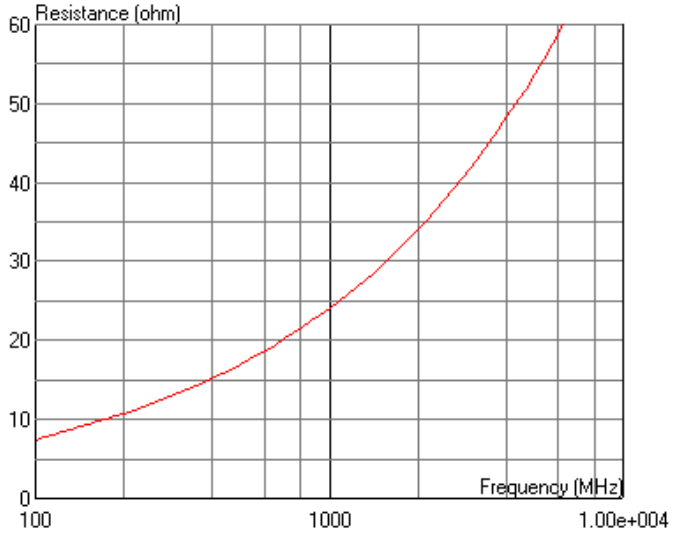
TLK6201EA Board Equalizer (Texas Instruments)

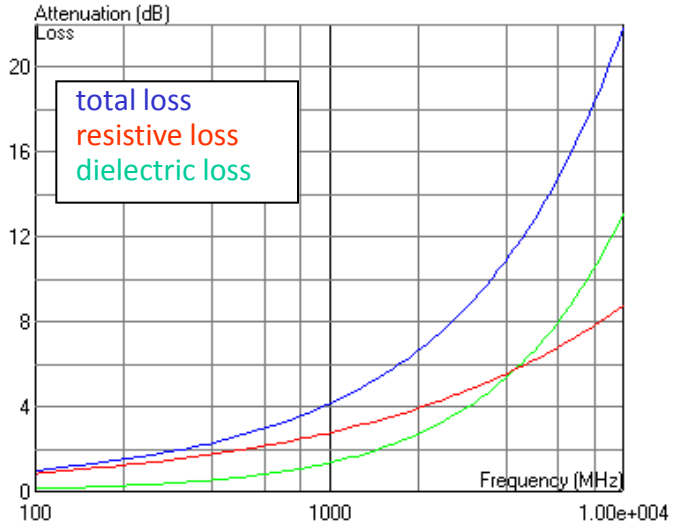
Lossy TML

- differential strip line
  - dielectric thickness : 75 µm
  - dielectric constant: 3.5
  - spacing: 100 µm, width: 100 µm
  - metal thickness: 18 µm
  - length: 40 cm



- impedance and loss
  - Z_0 = 40.2 Ω
  - DC resistance R_{DC} = 3.8 Ω
  - effective resistance @ 1 GHz R_{eff} = 24 Ω
  - attenuation 20 log (Z_0/(Z_0+R_{eff})) = 4dB





TML impedances: flex kapton and Si substrate

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micro-strip line (no top metal layer), 18 µm copper				
line width	spacing	dielectric	Z0 se.	Z0 diff
60	100	25	39,2	74,0
80	100	25	33,6	63,7
100	100	25	29,5	56,0
60	100	50	56,0	96,9
80	100	50	49,6	86,6
100	100	50	44,7	78,6
60	100	75	67,0	107,4
80	100	75	60,4	97,7
100	100	75	55,1	90,1

strip line, 18 µm copper				
line width	spacing	dielectric	Z0 se.	Z0 diff
60	100	25	25,7	51,2
80	100	25	21,3	42,6
100	100	25	18,3	36,4
60	100	50	40,7	78,9
80	100	50	35,0	68,2
100	100	50	30,7	60,0
60	100	75	51,1	94,6
80	100	75	44,9	83,8
100	100	75	40,1	75,4

micro-strip line on *silicon substrate, 1 metal layer, 1µm Al*					
line width	spacing	dielectric	Z0 se.	Z0 diff	
5	5	0,2	477	92,5	
3	5	0,2	495	107	
micro-strip line on *silicon substrate, 2 metal layers, no passivation on top*					
line width	spacing	dielectric	Z0 se.	Z0 diff	
5	5	0,2	6,9	13,8	no passivation
5	5	1	26,1	50,5	no passivation
5	5	1	23,9	45,8	1 µ passivation

bulk resistivity [Ohm/m]

Cu $1.724\ 10^{-8}$

Al $2.863\ 10^{-8}$

Ag $1.63\ 10^{-8}$

Au $2.72\ 10^{-8}$

Zn $11.5\ 10^{-8}$

High speed signalling test equipment

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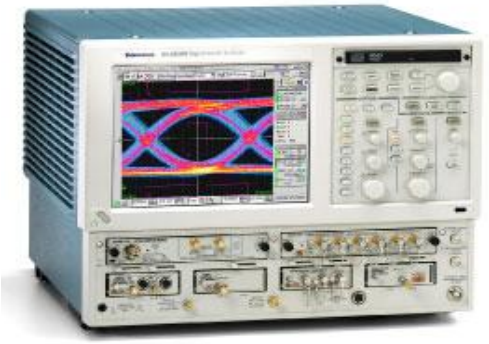
- 20 GHz Sampling Oscilloscope (DSA 8200)
  - high speed data links characterization
  - time domain reflectometry (TDR)
  - eye diagram analysis



- 3.35 GHz Pattern Generator (Agilent 81134A)
  - real time signal measurements

- FPGA based bit error rate tester
  - ML-505 board (Virtex5LX110T)