



DCE8 Status

A. Wassatsch

- Introduction
- Clustering principle
- Implementation
- Test environment
- Time-plan



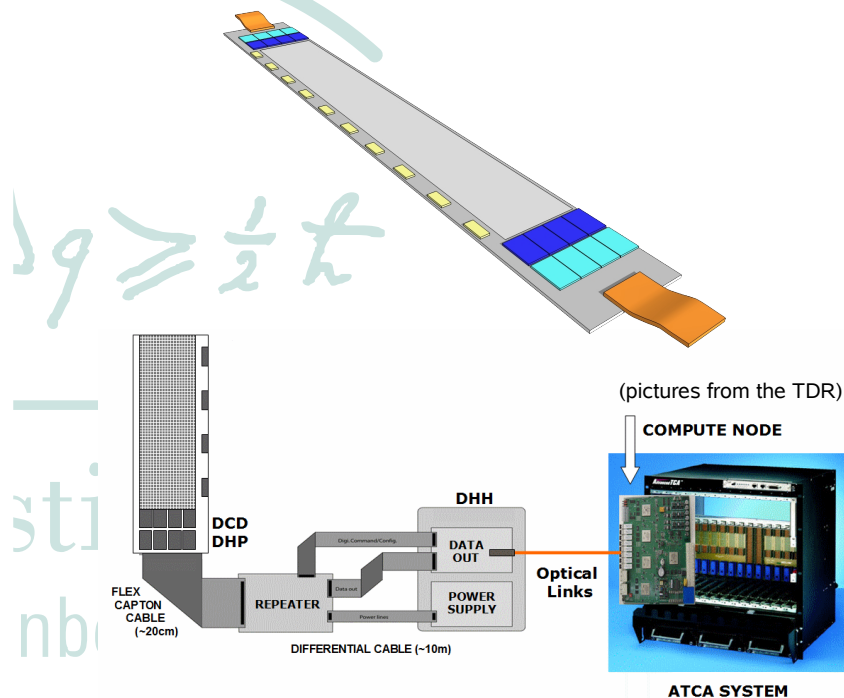
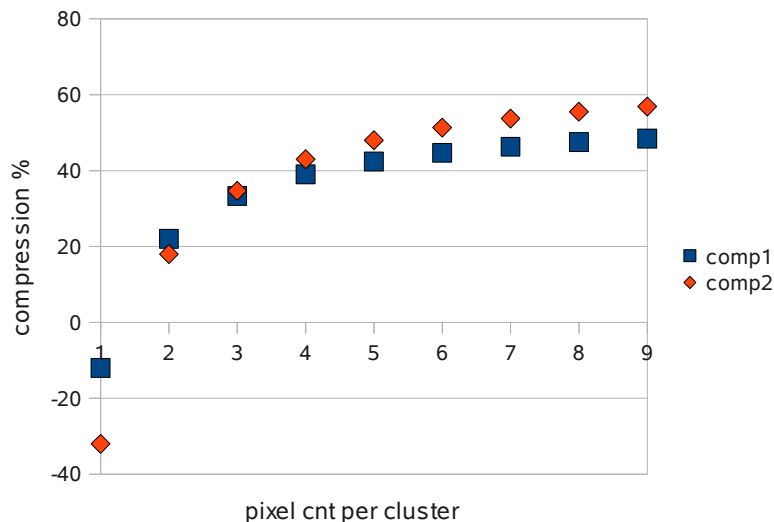
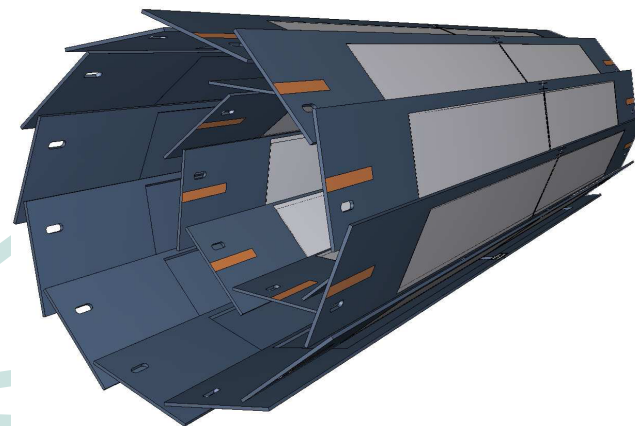
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Clustering for the Belle II PXD

- Readout of 240x1000 pixels per half ladder @ 50MHz row frequency
 - 8bit adc value + 18bit address
 - 1-2% fill factor
 - mean value of 3-4 pixel per cluster, commonly no more than 3 pixel per cluster in both directions
 - up to 6Gb raw data rate per half module → 4Gb after clustering





Clustering principle

	1	2	3	4	5	6	7	8
8	0	0	0	0	0	0	0	0
7	0	72	0	74	0	76	0	0
6	0	0	63	0	65	0	0	0
5	0	0	53	0	55	0	0	0
4	0	0	0	0	0	0	0	0
3	0	32	0	0	0	0	0	0
2	0	0	0	24	25	26	27	0
1	0	0	0	0	0	0	0	0

- Process data after zero suppression
- Pixel wise readout: 24 2 4; 25 2 5; 26 ...; 76 7 6
- $12 \times (8+8+10)b = 312b$

- With clustering:

CE CY CX ML ME...
 25 2 5 18h 24 26;
 27 2 7 0h;
 32 3 2 0h;
 63 6 3 a2h 53 72 74;
 65 6 5 82h 55 76;

50b
 34b
 34b
 58b
50b
 226b

- One row per clock cycle in parallel

$$\Delta p \cdot \Delta q \geq \frac{1}{2} \hbar$$

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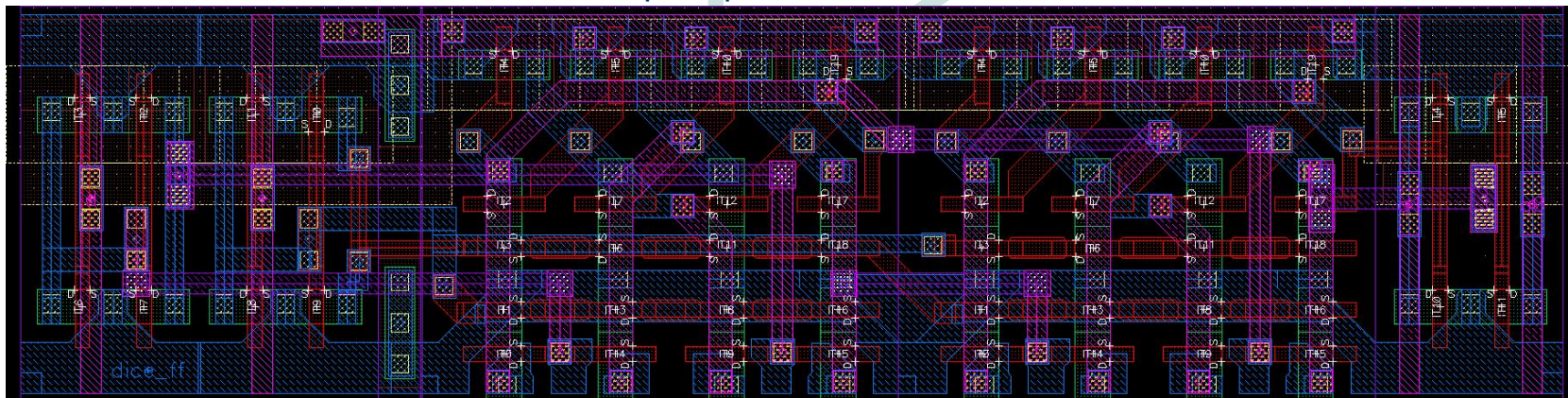
5	6	7
3		4
0	1	2

Local address scheme

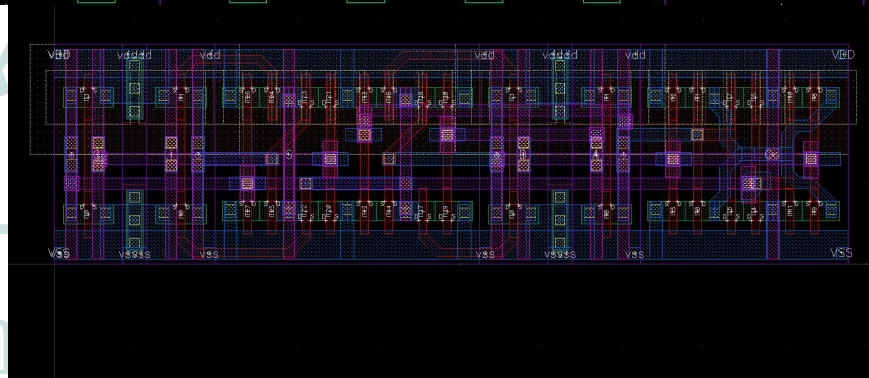


Implementation details: the cell library

- 90nm IBM process
- Self made library
 - Need of SEU tolerant Flip-Flop cell → dice cell



- Minimum sized logic cells



- compatible with the ARM standard cell lib (backup solution)

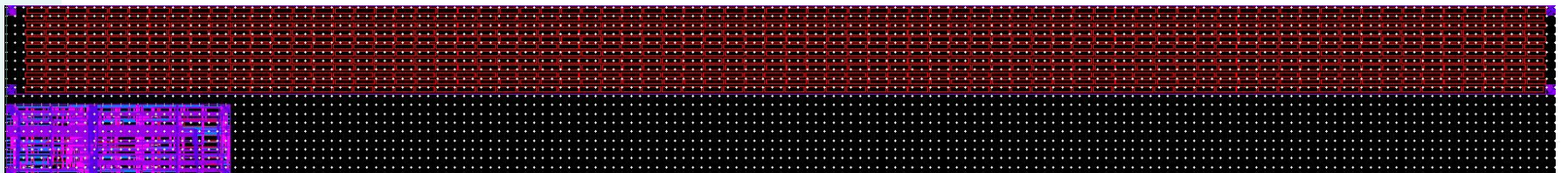
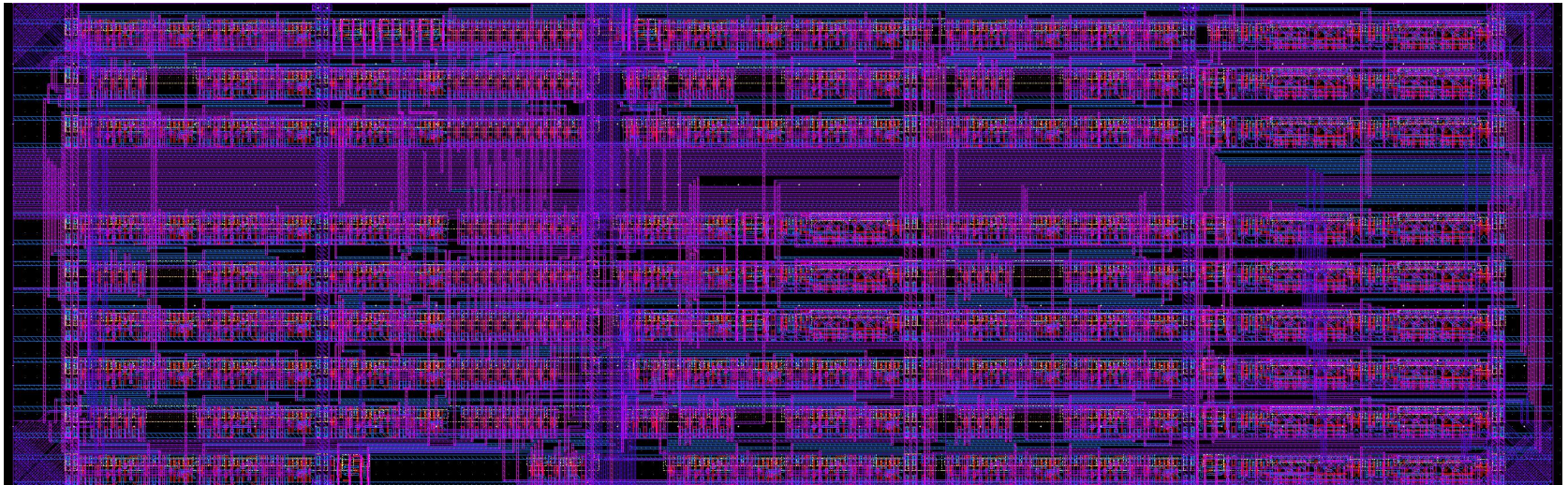
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Implementation details: the clustering node

- Basic building block of the clustering algorithm
- 4 side plug-gable
- implements a simplified clustering algorithm → area reduction by factor 8
- $127 \times 40 \mu\text{m}^2$ (old: $850 \times 50 \mu\text{m}^2$)



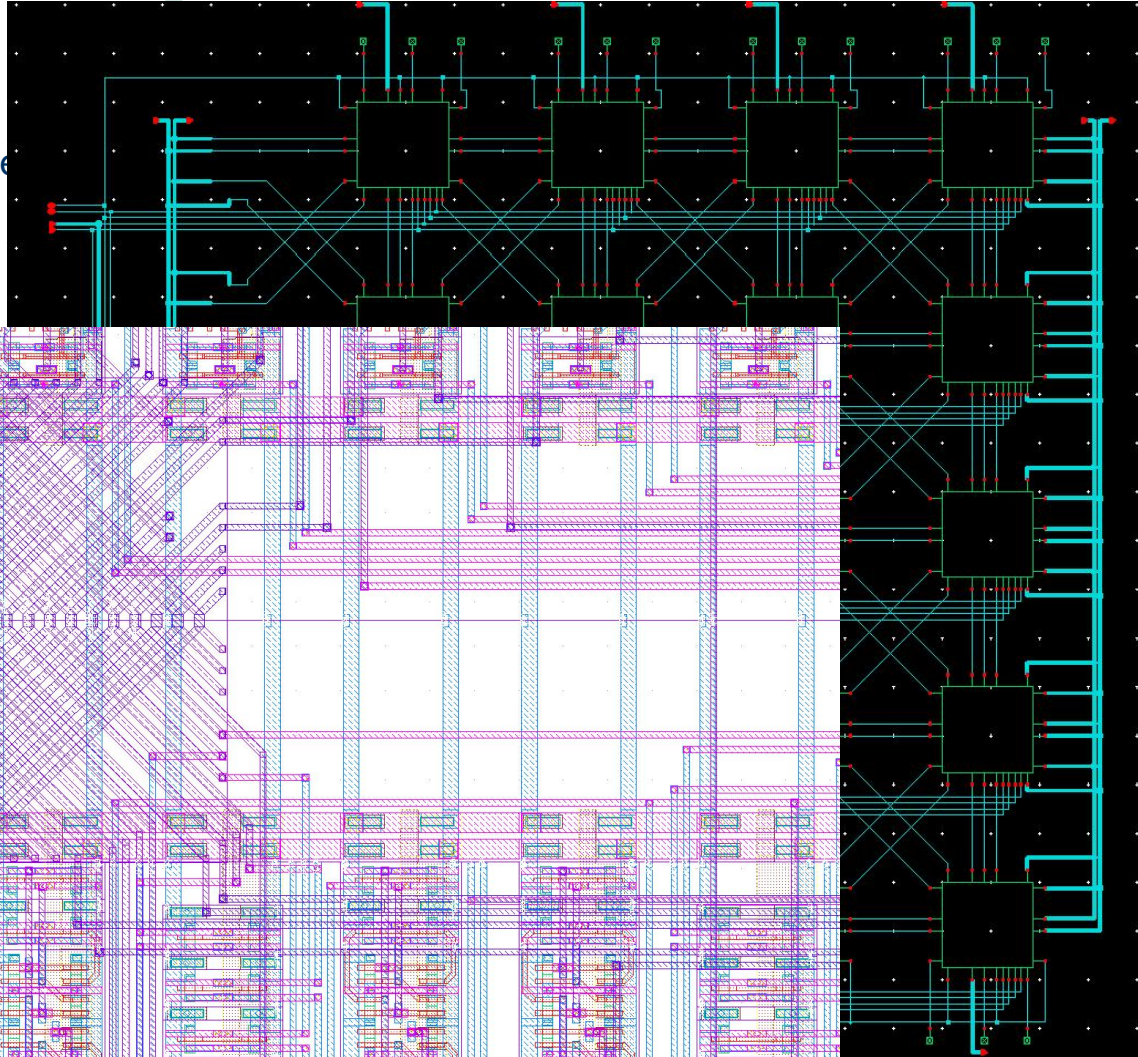


Implementation details: the clustering array

- Implements the clustering algorithm

Pipe-lined implementation:

- 5 stages
- 1 row per clock
- “unlimited” channel count possible



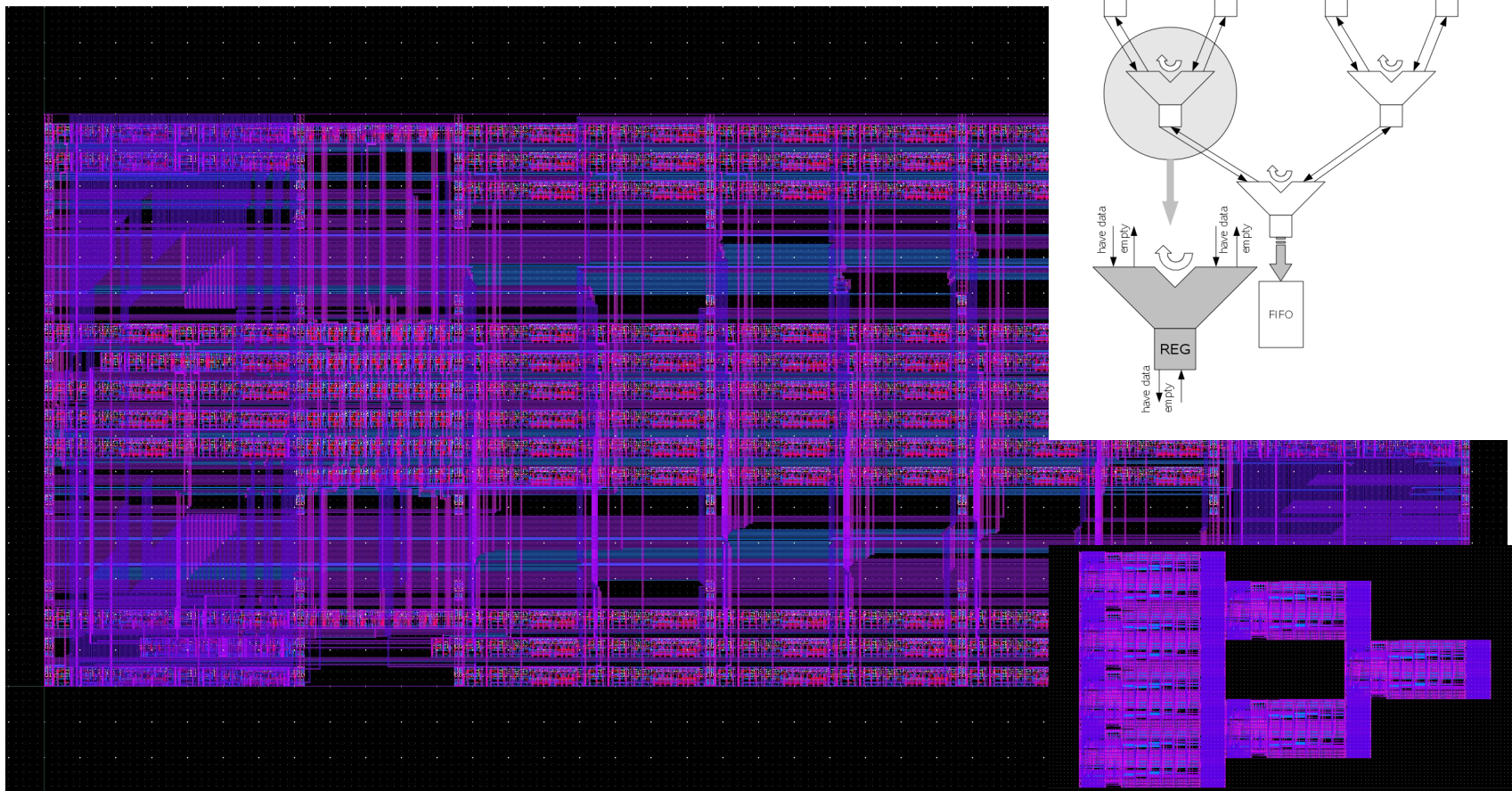


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- The image displays a digital logic design project in a software environment. The top portion shows a schematic diagram of a circuit. It features two comparators, each with a 7-bit input and a 7-bit output. The first comparator's output is connected to a multiplexer (MUX) that selects between two inputs based on a control signal. The second comparator's output is connected to a multiplexer that selects between two inputs based on a control signal. The circuit is designed to detect a new edge in a digital signal.
- The bottom portion shows a timing diagram with multiple signal traces. The traces are color-coded: red for clock signals, blue for data signals, and green for control signals. The diagram shows the timing relationships between various signals, including a clock signal (buf_clk), a data signal (data), and control signals (new_edge, clus_out, clus_in). The timing diagram is used to verify the functionality of the circuit by checking the timing of the signals.



Implementation details: the tree node

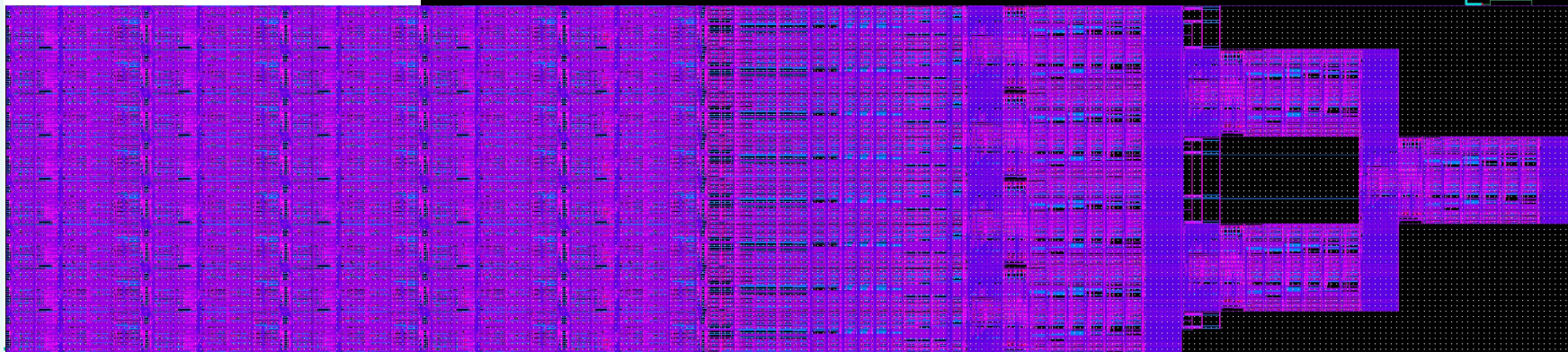
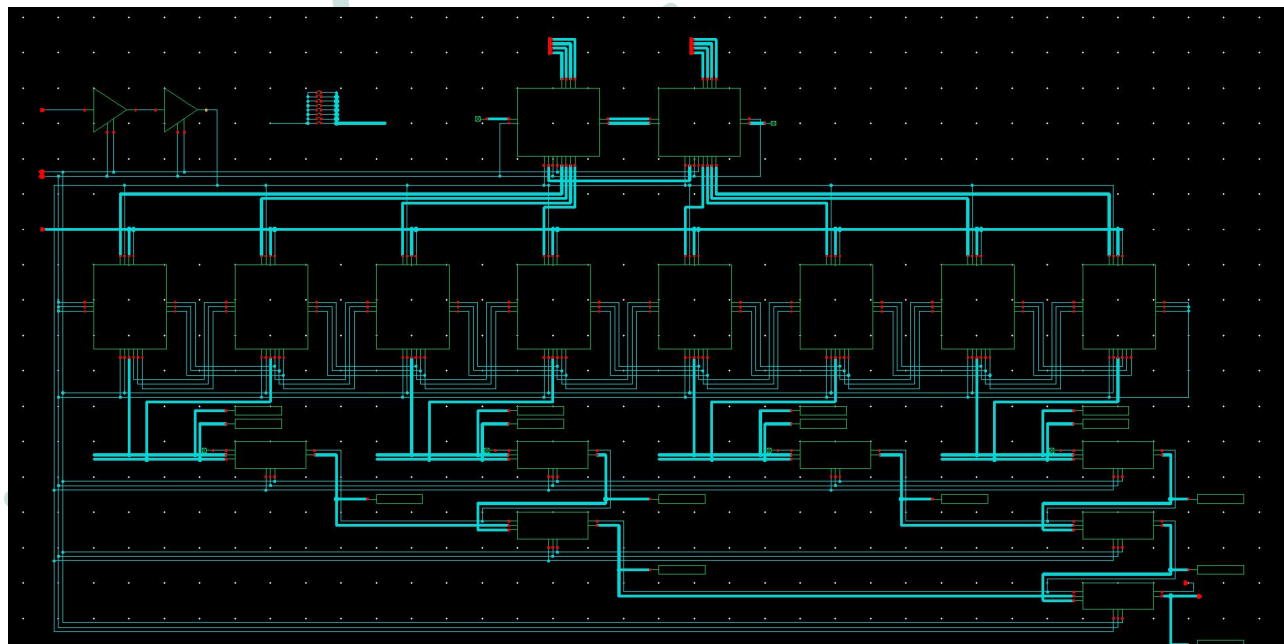
- Collects the cluster packages out from the different columns
- Through-put optimized version
- $200 \times 80 \mu\text{m}^2$





Implementation details: the dec8 core

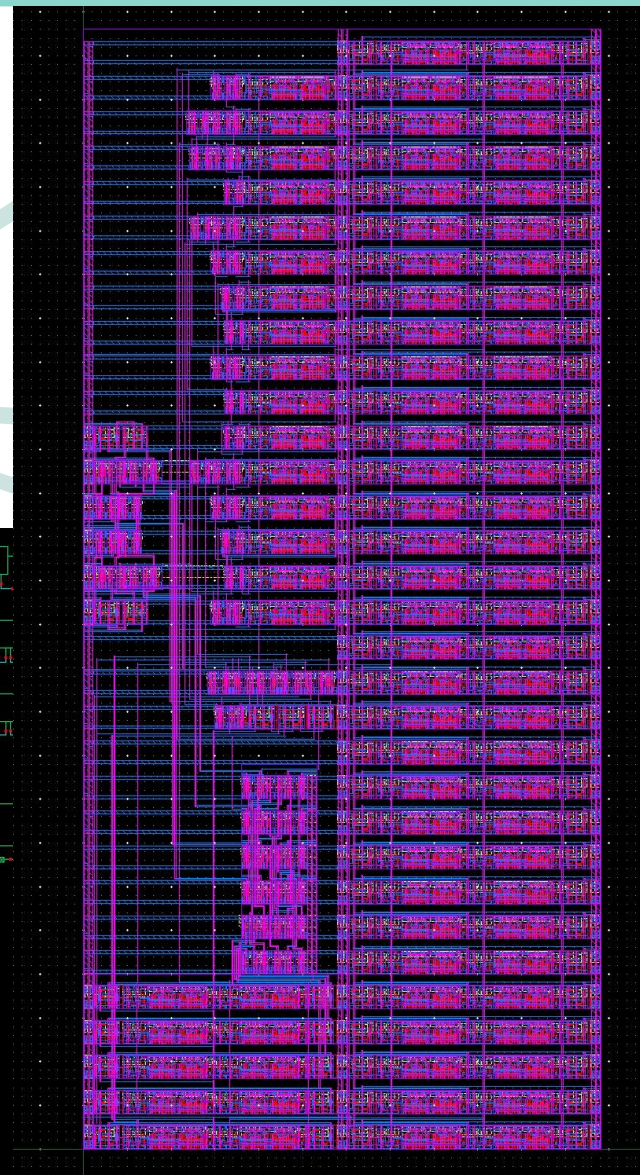
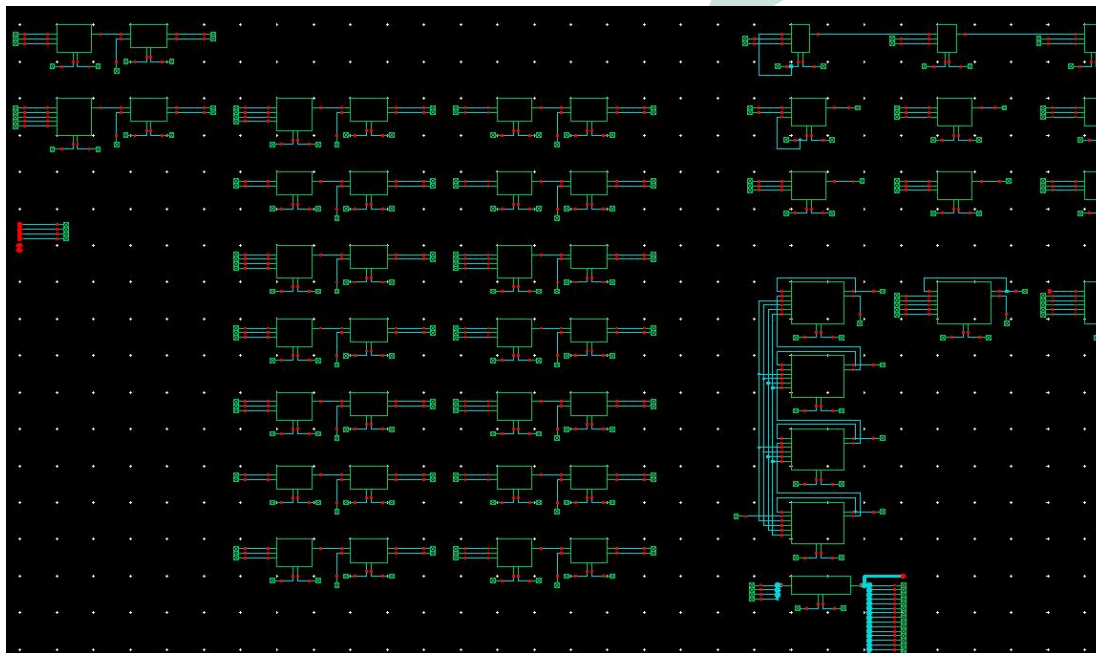
- 8 channel version of the clustering pipeline, designed for 100MHz operation frequency
- Over all 5+2+3 pipeline stages
- 0.45mW/ch@100MHz
- 1.4x0.32mm²





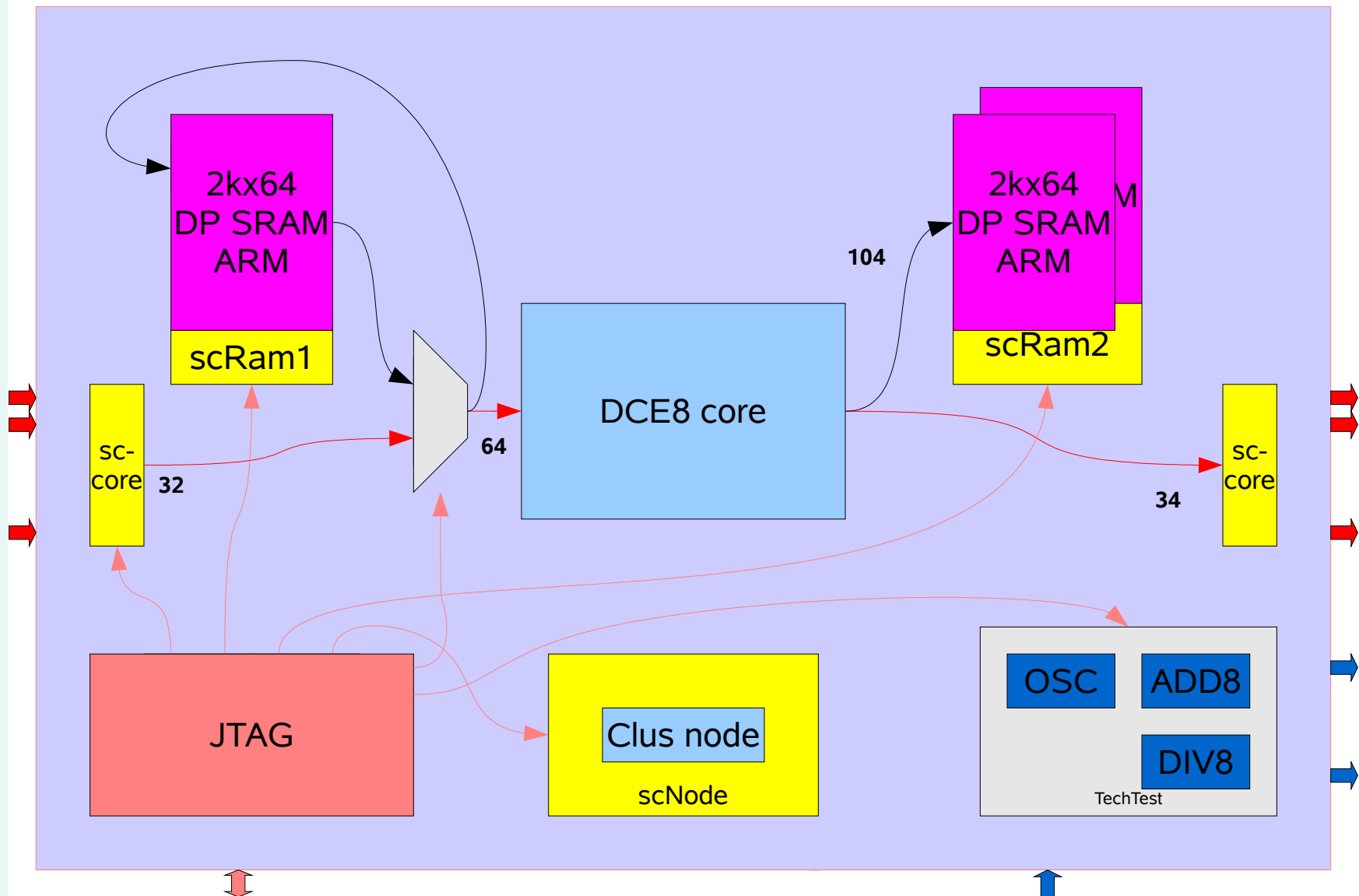
Implementation details: JTAG interface

- Standard for the slow control in the Belle II PXD
 - 32 bit user register
 - 14 free scan chains



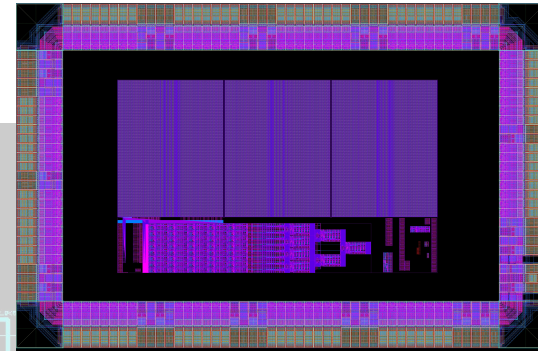


The DCE8 asic





Implementation: status



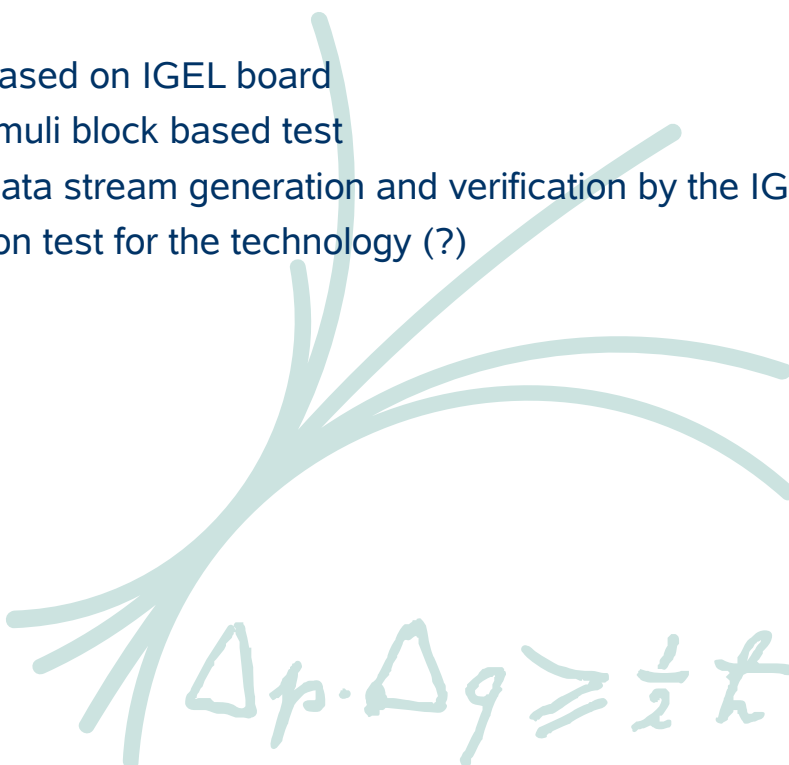
- VHDL description: **ready**
 - for ARM lib based synthesis and verification
 - for equivalence checking against cadence schematics
- Small standard cell mpi lib: **ready**
 - To become familiarly with the technology
 - ARM 90nm standard cell library still available, used for the pad ring
- macro cells (clus,coll,tree) as a custom layout (based on the small mpi lib): **ready**
- JTAG ctrl unit (32bit user chain and 14 additional instruction decode outputs): **ready**
- Dual-port memory out from the ARM/Artisan compiler: **ready**
- Spy/Stimuli unit: **ready**
- Output scheduler: **ready**
- DCE8 core: **ready**
- DCE8 asic (pad connections, technology test circuits): work in progress
 - 3.5x2.3 mm
 - 3M transistor design → challenging verification → mixed mode simulations
- Nice to have features, but currently not implemented:
 - Fast link components for interface to DHP (1. gen) and readout board (De-/Serializer)
 - On-Chip pll for local clock generation
 - Further optimization of the tree layout

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Test plan and environment

- Standalone test based on IGEL board
 - Spy/Stimuli block based test
 - Serial data stream generation and verification by the IGEL fpga
 - Radiation test for the technology (?)

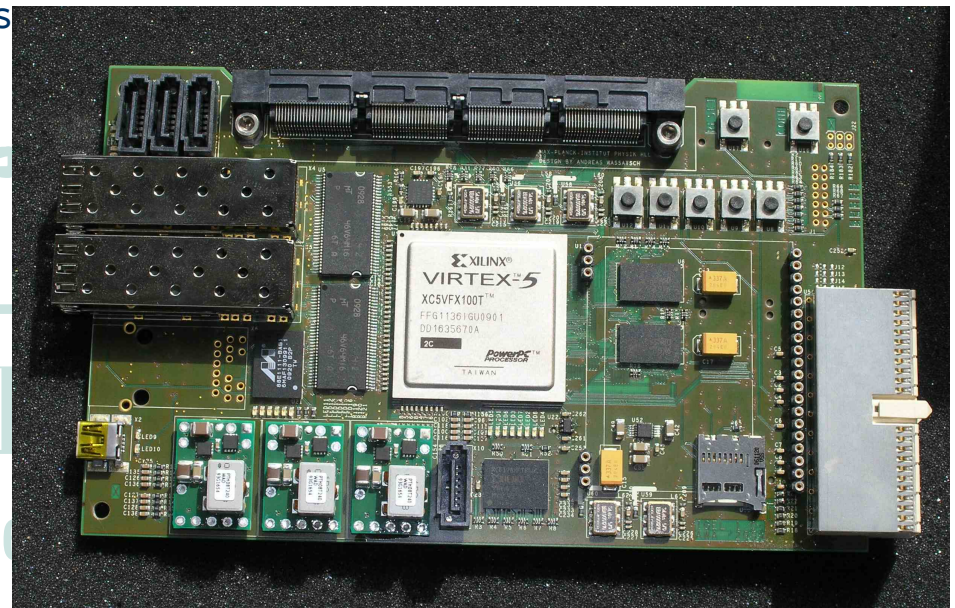

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Time-plan and Next steps

- DCE 8 column testchip
 - Finalization of the design: May. 2010
 - Submission: second 2010 mosis run (24.05.2010)
 - CERN will not organize a MPW contribution → full MOSIS costs (95k\$)
 - Update: 20.04.2010 the May mosis run will most likely not take place (CERN,MOSIS), next date 09.09.2010
- IGEL board:
 - two prototype boards arrived from the WHI workshop (FX70/100T)
 - First board tests in progress
 - Production of the remaining 8 boards of the first batch (Sep. 2010)



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