DCE8 Status

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- Introduction
- Clustering principle
- Implementation
- Test environment
- Time-plan

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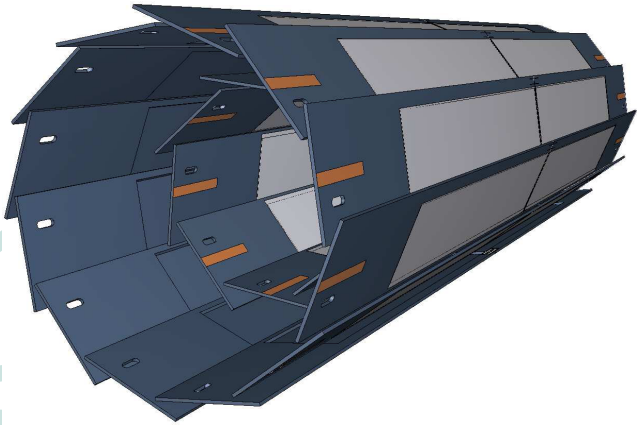
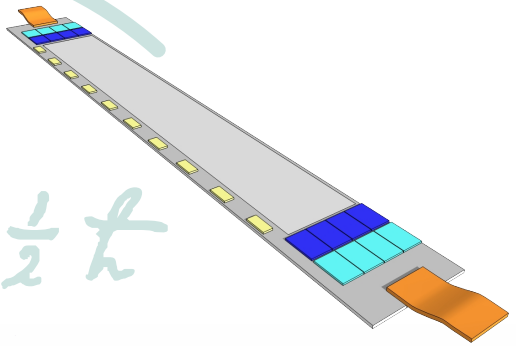
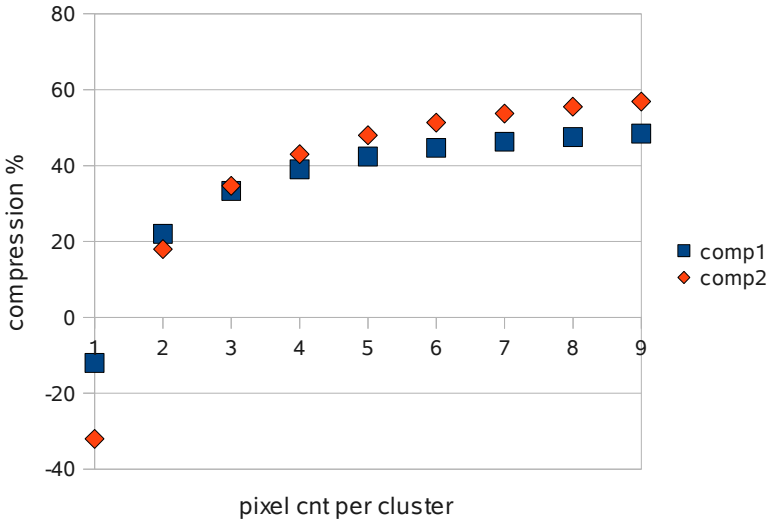
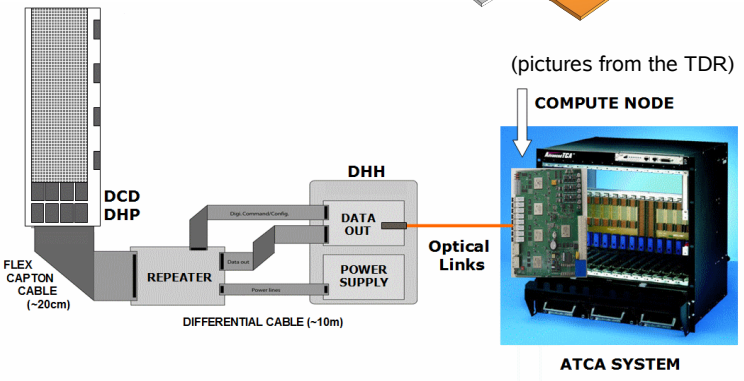
Clustering for the Belle II PXD

- Readout of 240x1000 pixels per half ladder @ 50MHz row frequency
  - 8bit adc value + 18bit address
  - 1-2% fill factor
  - mean value of 3-4 pixel per cluster, commonly no more than 3 pixel per cluster in both directions
  - up to 6Gb raw data rate per half module → 4Gb after clustering

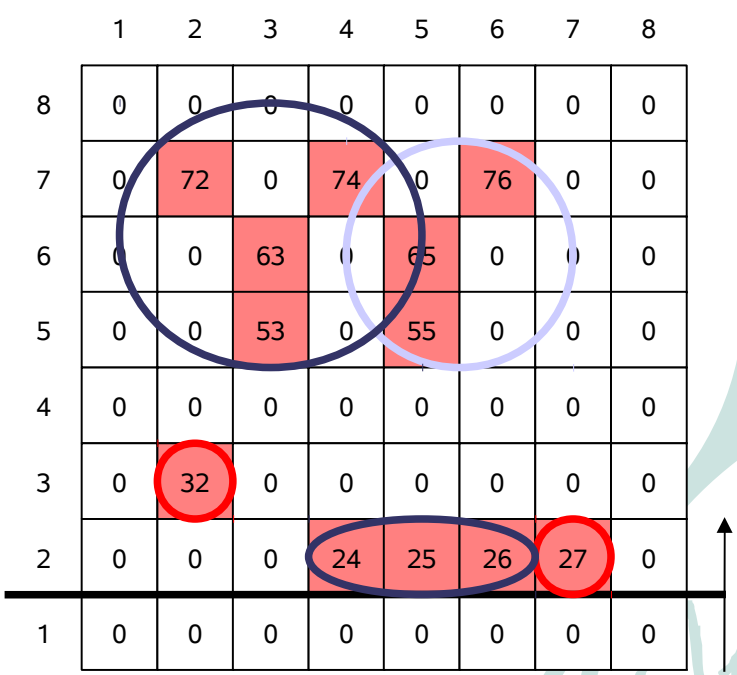








Clustering principle



- Process data after zero suppression
- Pixel wise readout: 24 2 4; 25 2 5; 26 …; 76 7 6
  - 12x(8+8+10)b = 312b
- With clustering:

CE	CY	CX	ML	ME...	
25	2	5	18h	24 26;	50b
27	2	7	0h;		34b
32	3	2	0h;		34b
63	6	3	a2h	53 72 74;	58b
65	6	5	82h	55 76;	50b
					226b

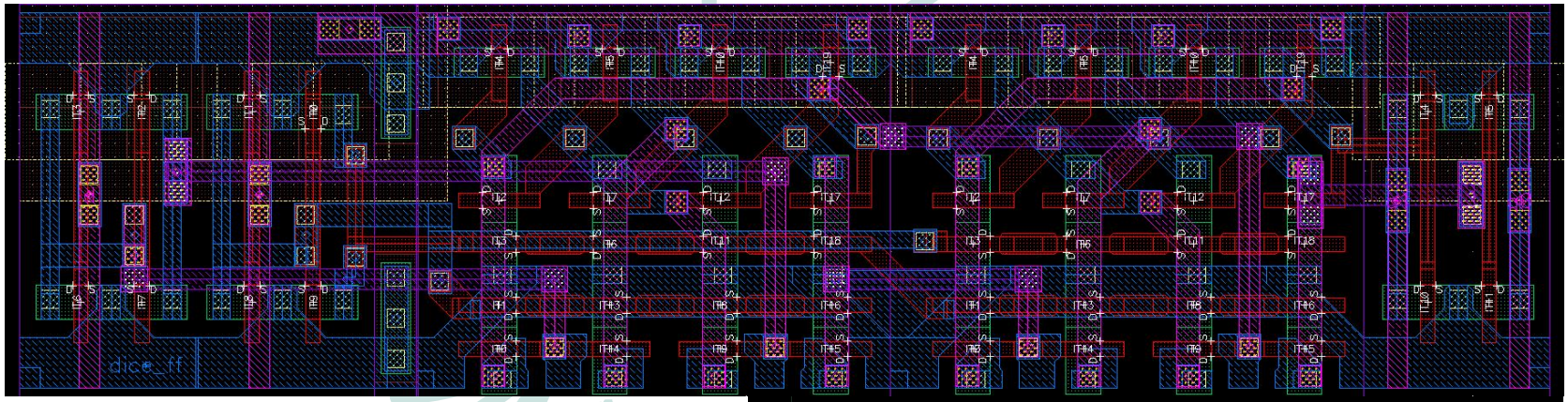
- One row per clock cycle in parallel

5	6	7
3		4
0	1	2

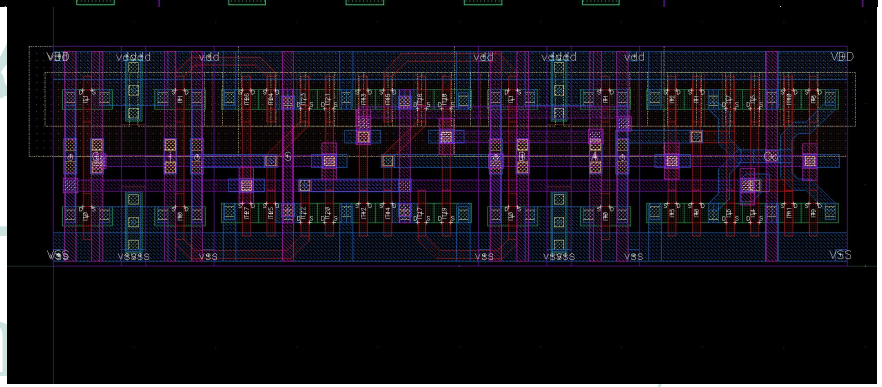
Local address scheme

Implementation details: the cell library

- 90nm IBM process
- Self made library
  - Need of SEU tolerant Flip-Flop cell → dice cell



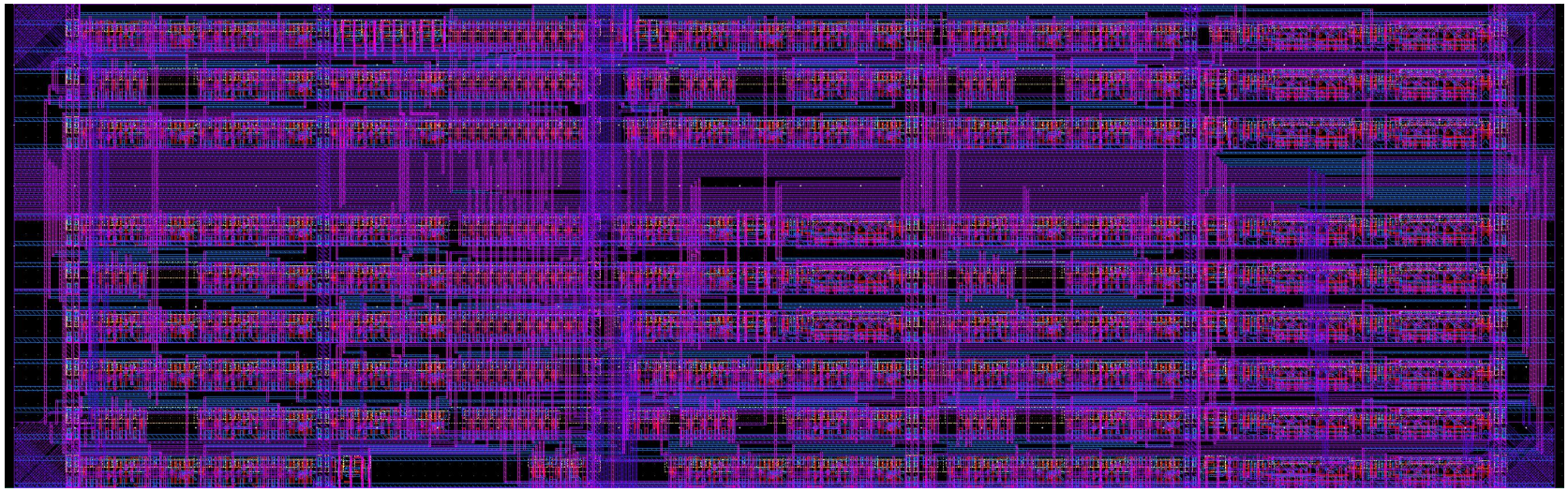
  - Minimum sized logic cells

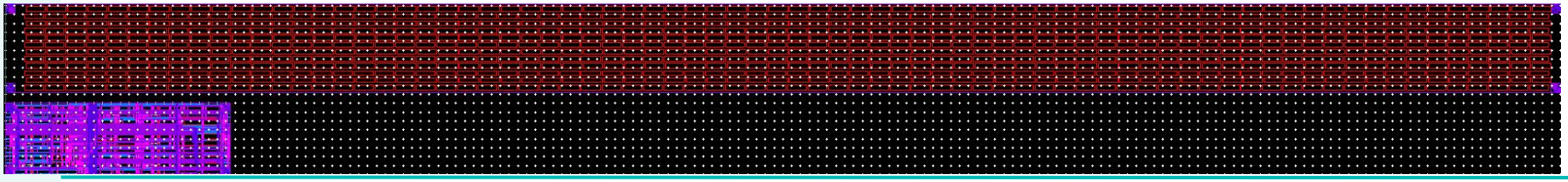


  - compatible with the ARM standard cell lib (backup solution)

Implementation details: the clustering node

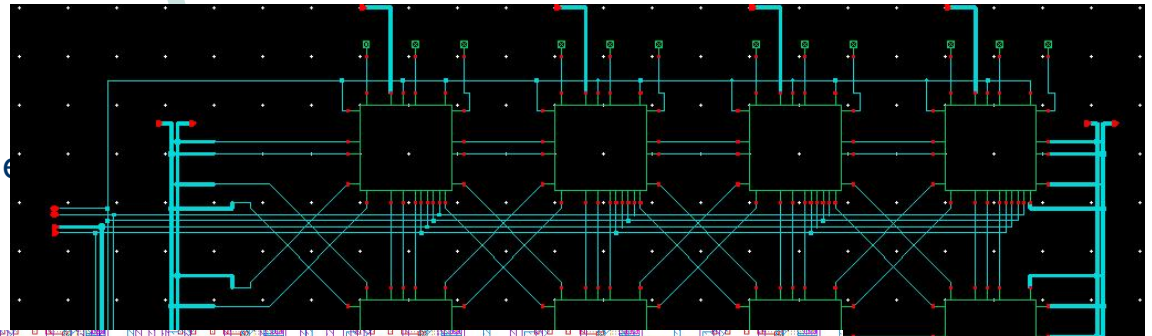
- Basic building block of the clustering algorithm
- 4 side plug-gable
- implements a simplified clustering algorithm → area reduction by factor 8
- 127x40µm^2 (old: 850x50µm^2)

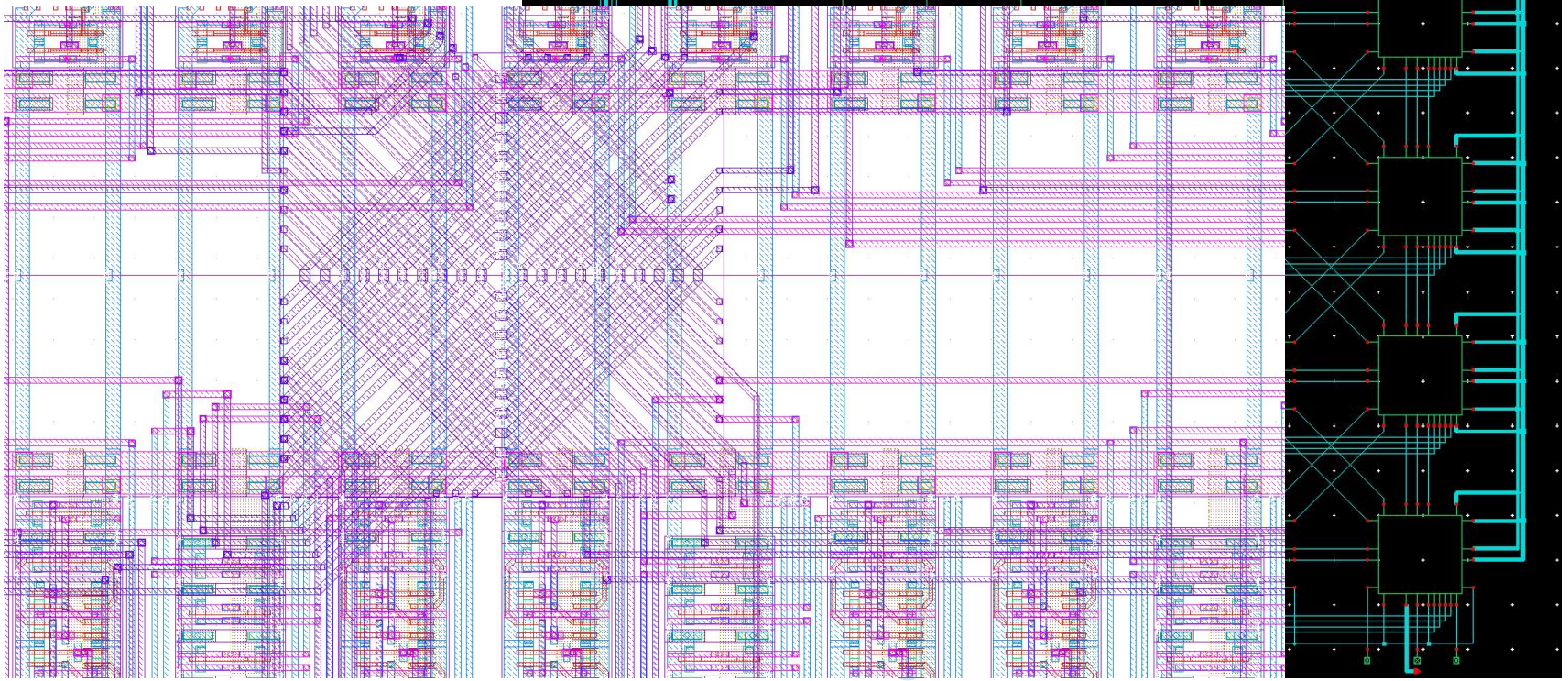




Implementation details: the clustering array

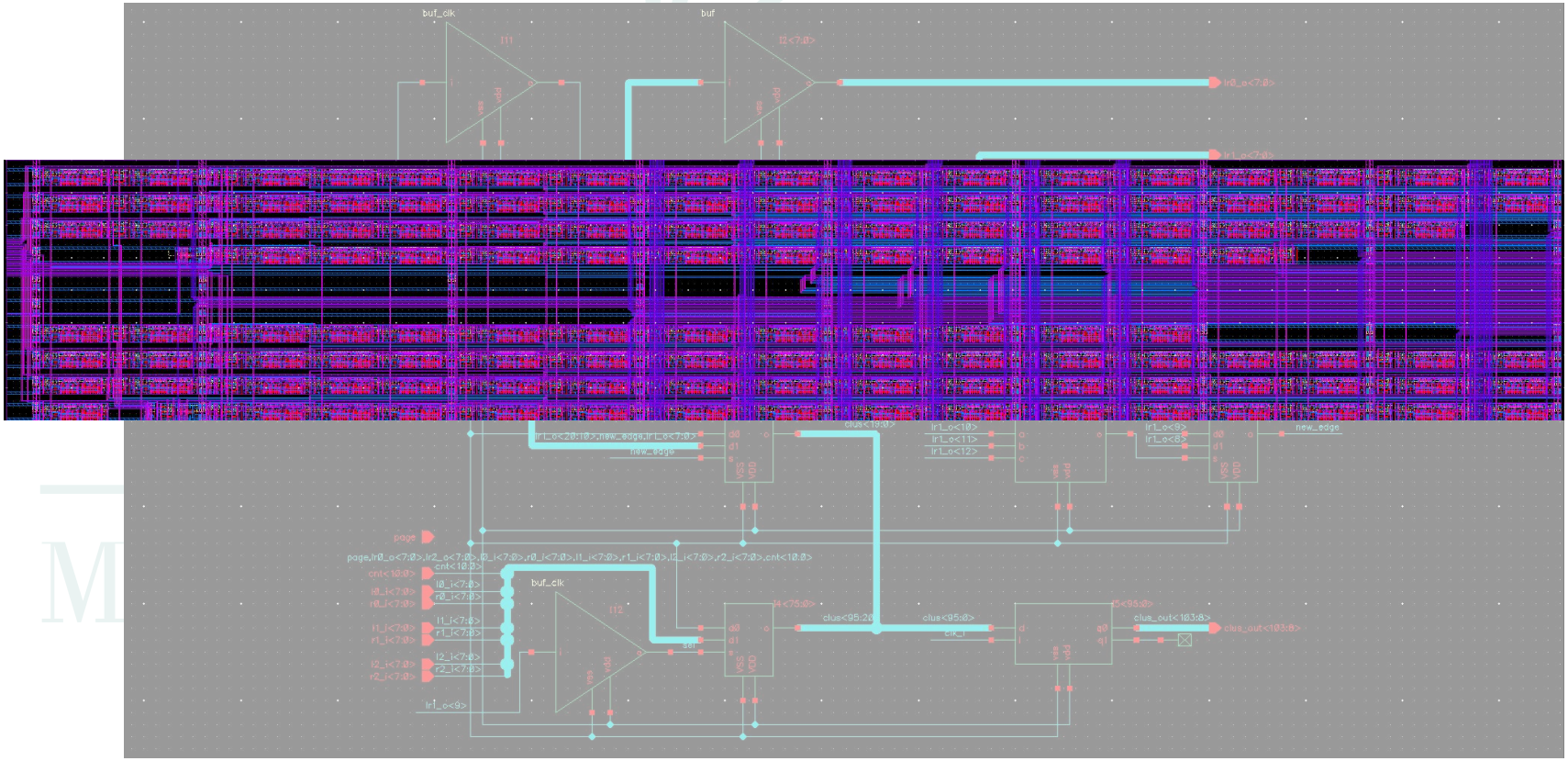
- Implements the clustering algorithm
- Pipe-lined implementation:
  - 5 stages
  - 1 row per clock
  - “unlimited” channe count possible





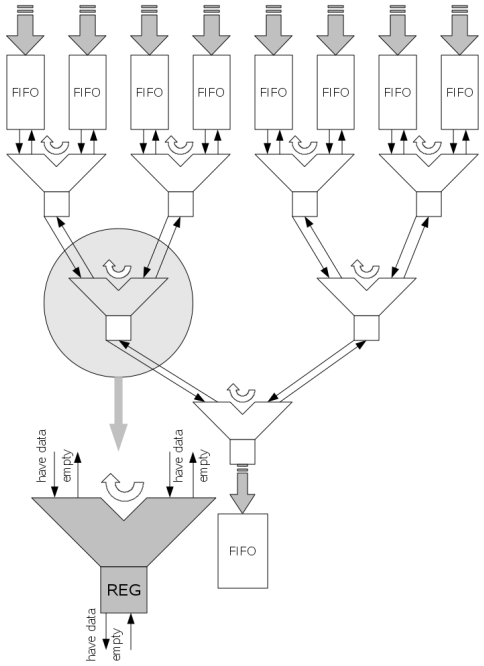
Implementation details: the collect node

- Collect the data for the cluster packages
  - 240x40 µm²
- Reduce the area of the clustering nodes
  - 21 Flip-Flops in clustering node → 104 FF (5x50 +240 < 5x200)



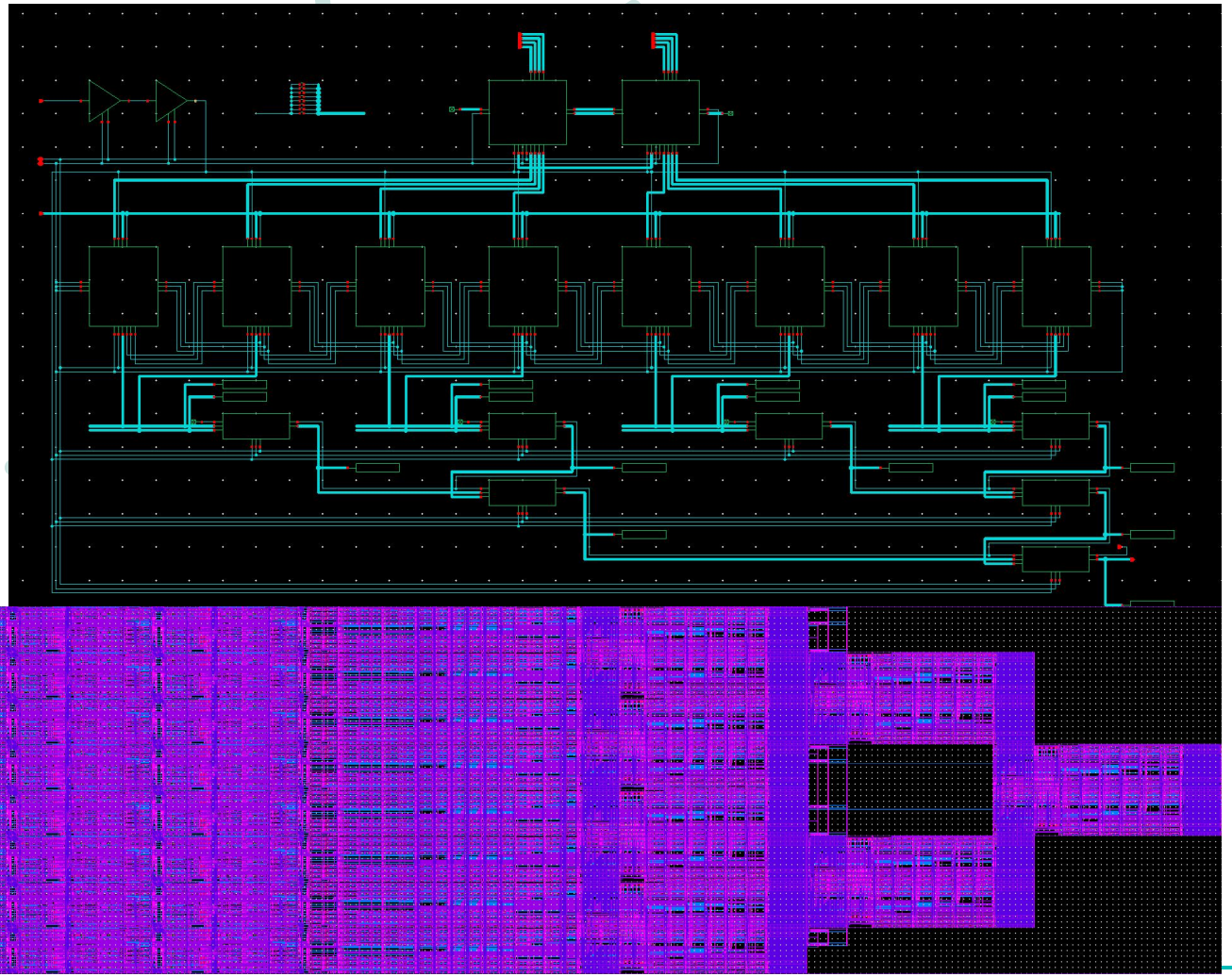
Implementation details: the tree node

- Collects the cluster packages out from the different columns
- Through-put optimized version
- 200x80 μm^2



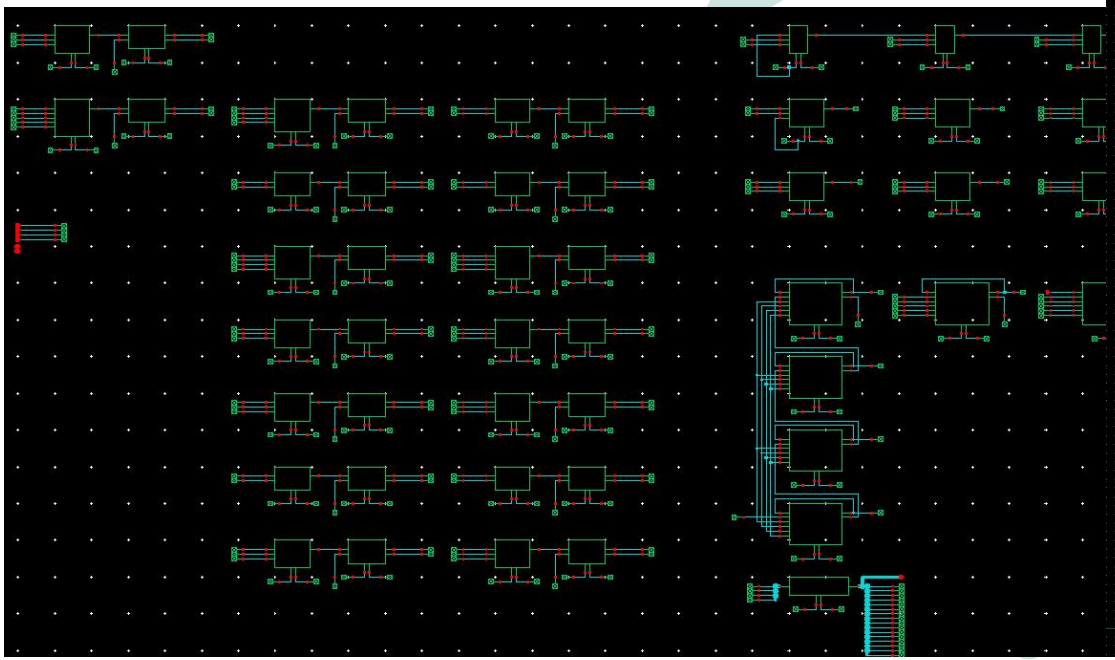
Implementation details: the dec8 core

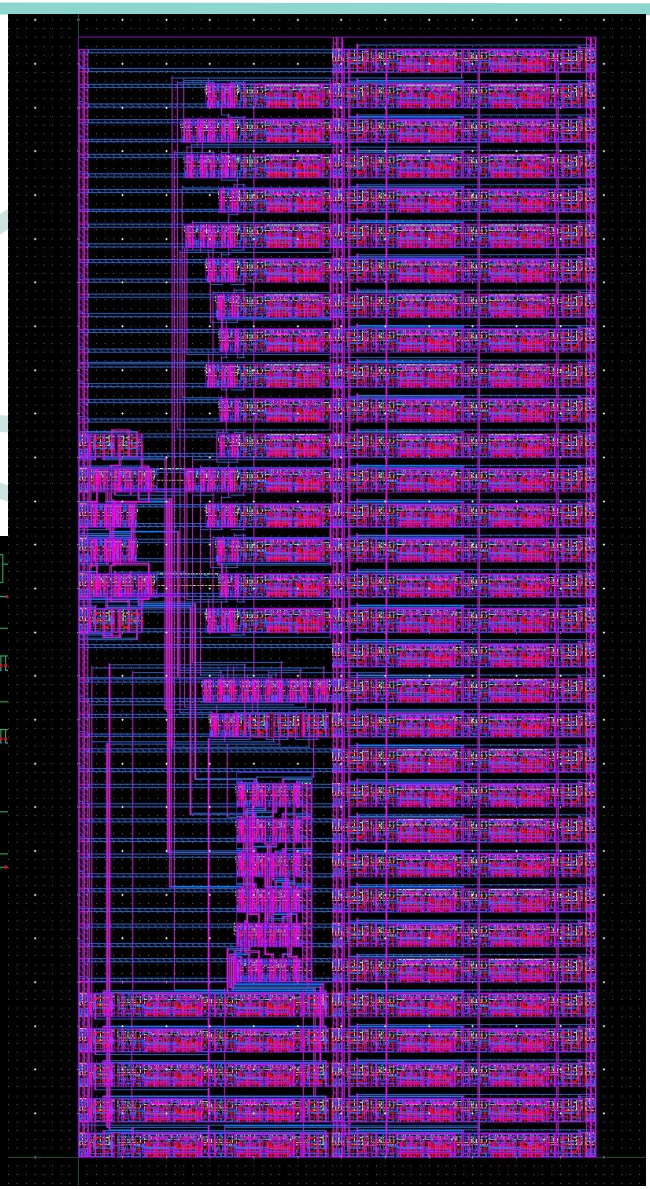
- 8 channel version of the clustering pipeline, designed for 100MHz operation frequency
- Over all 5+2+3 pipeline stages
- 0.45mW/ch@100MHz
- 1.4x0.32mm^2



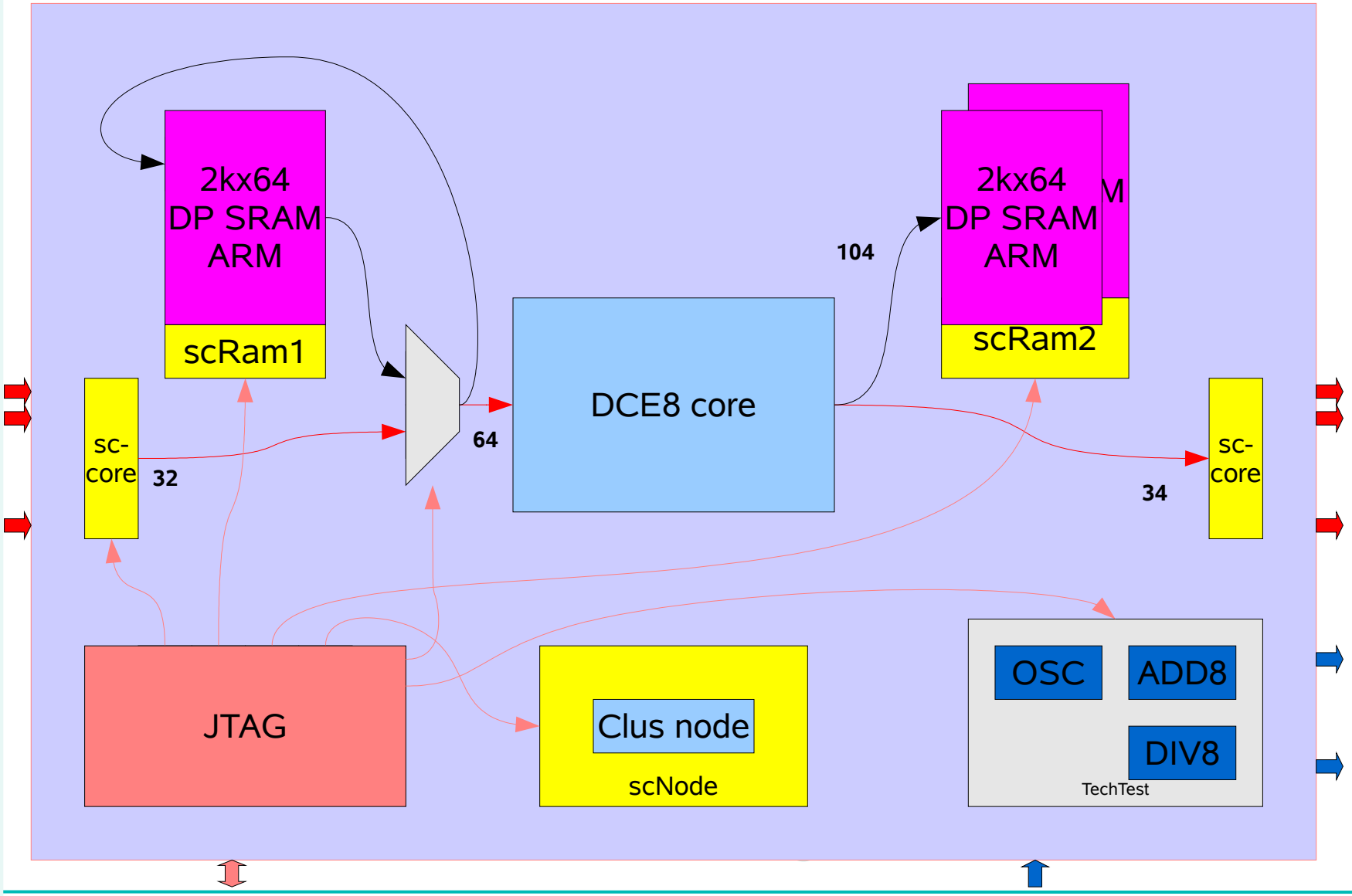
Implementation details: JTAG interface

- Standard for the slow control in the Belle II PXD
  - 32 bit user register
  - 14 free scan chains

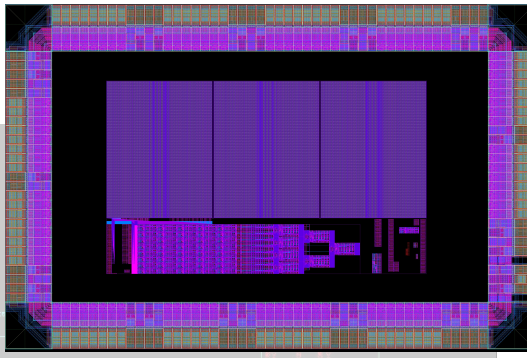




The DCE8 asic



Implementation: status



- VHDL description: ***ready***
  - for ARM lib based synthesis and verification
  - for equivalence checking against cadence schematics
- Small standard cell mpi lib: ***ready***
  - To become familiarly with the technology
  - ARM 90nm standard cell library still available, used for the pad ring
- macro cells (clus,coll,tree) as a custom layout (based on the small mpi lib): ***ready***
- JTAG ctrl unit (32bit user chain and 14 additional instruction decode outputs): ***ready***
- Dual-port memory out from the ARM/Artisan compiler: ***ready***
- Spy/Stimuli unit: ***ready***
- Output scheduler: ***ready***
- DCE8 core: ***ready***
- DCE8 asic (pad connections, technology test circuits): work in progress
  - 3.5x2.3 mm
  - 3M transistor design → challenging verification → mixed mode simulations
- Nice to have features, but currently not implemented:
  - Fast link components for interface to DHP (1. gen) and readout board (De-/Serializer)
  - On-Chip pll for local clock generation
  - Further optimization of the tree layout

Test plan and environment

- Standalone test based on IGEL board
  - Spy/Stimuli block based test
  - Serial data stream generation and verification by the IGEL fpga
  - Radiation test for the technology (?)

Time-plan and Next steps

- DCE 8 column testchip
  - Finalization of the design: May. 2010
  - Submission: second 2010 mosis run (24.05.2010)
    - CERN will not organize a MPW contribution → full MOSIS costs (95k$)
    - Update: 20.04.2010 the May mosis run will most likely not take place (CERN,MOSIS), next date 09.09.2010
- IGEL board:
  - two prototype boards arrived from the WHI workshop (FX70/100T)
  - First board tests in progres
  - Production of the remaining 8 boards of the first batch (Sep. 2010)