UNIVERSITÄT
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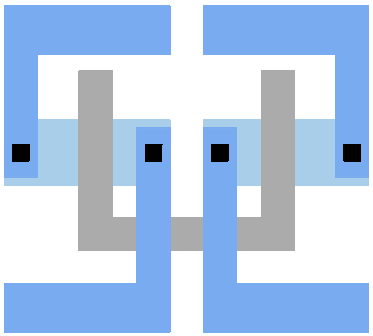
DCD-RO



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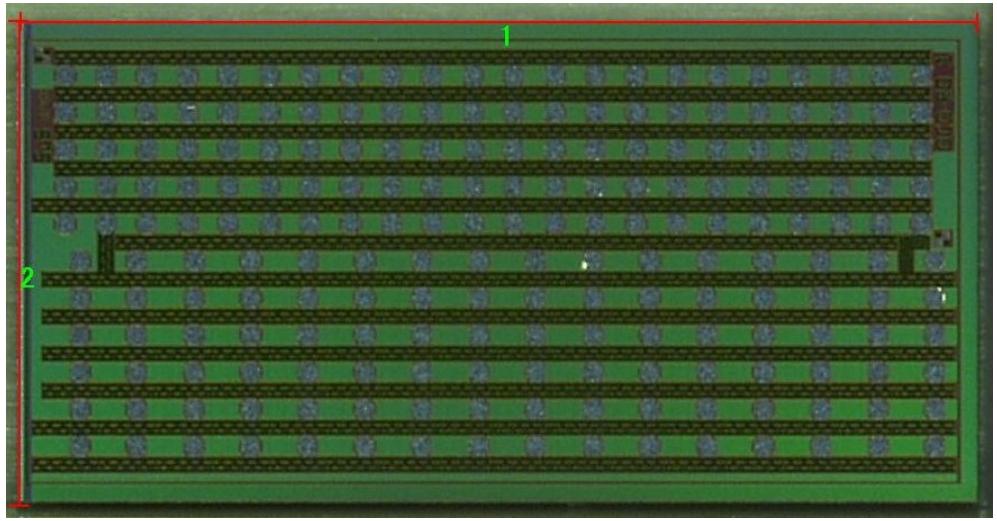
4th International Workshop on DEPFET detectors and applications

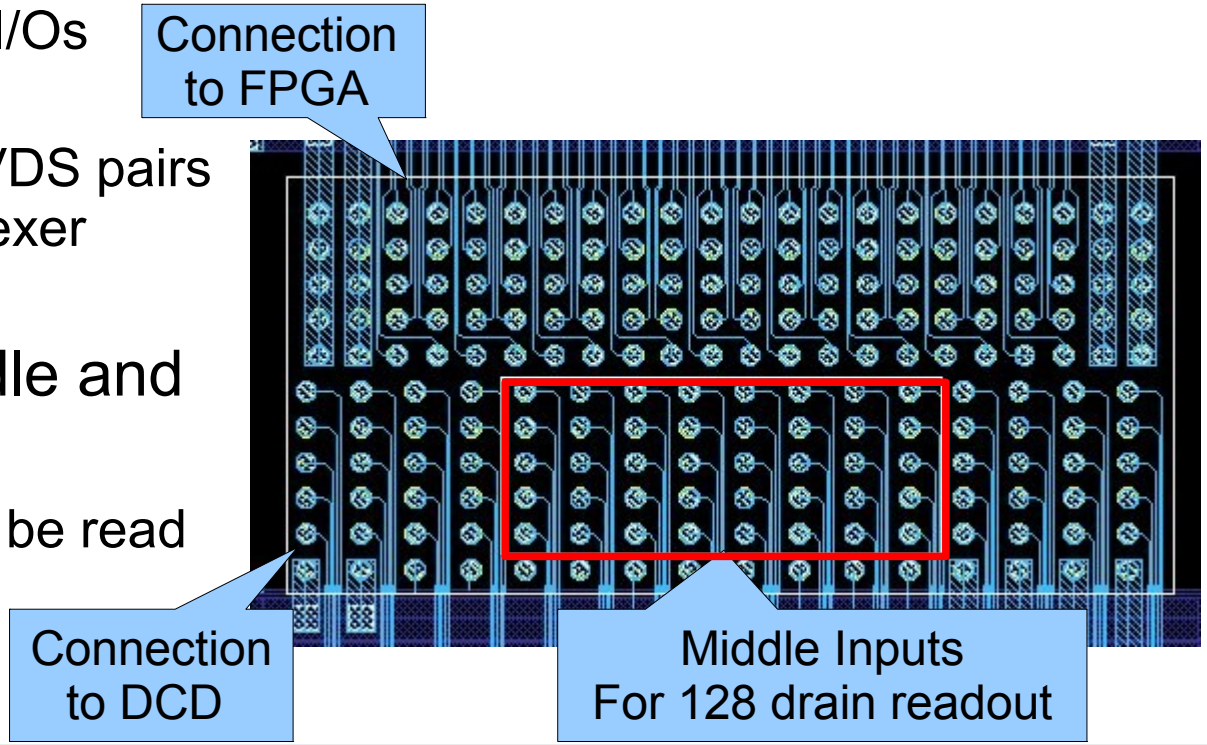
Ringberg Castle

03. - 05.05.2010

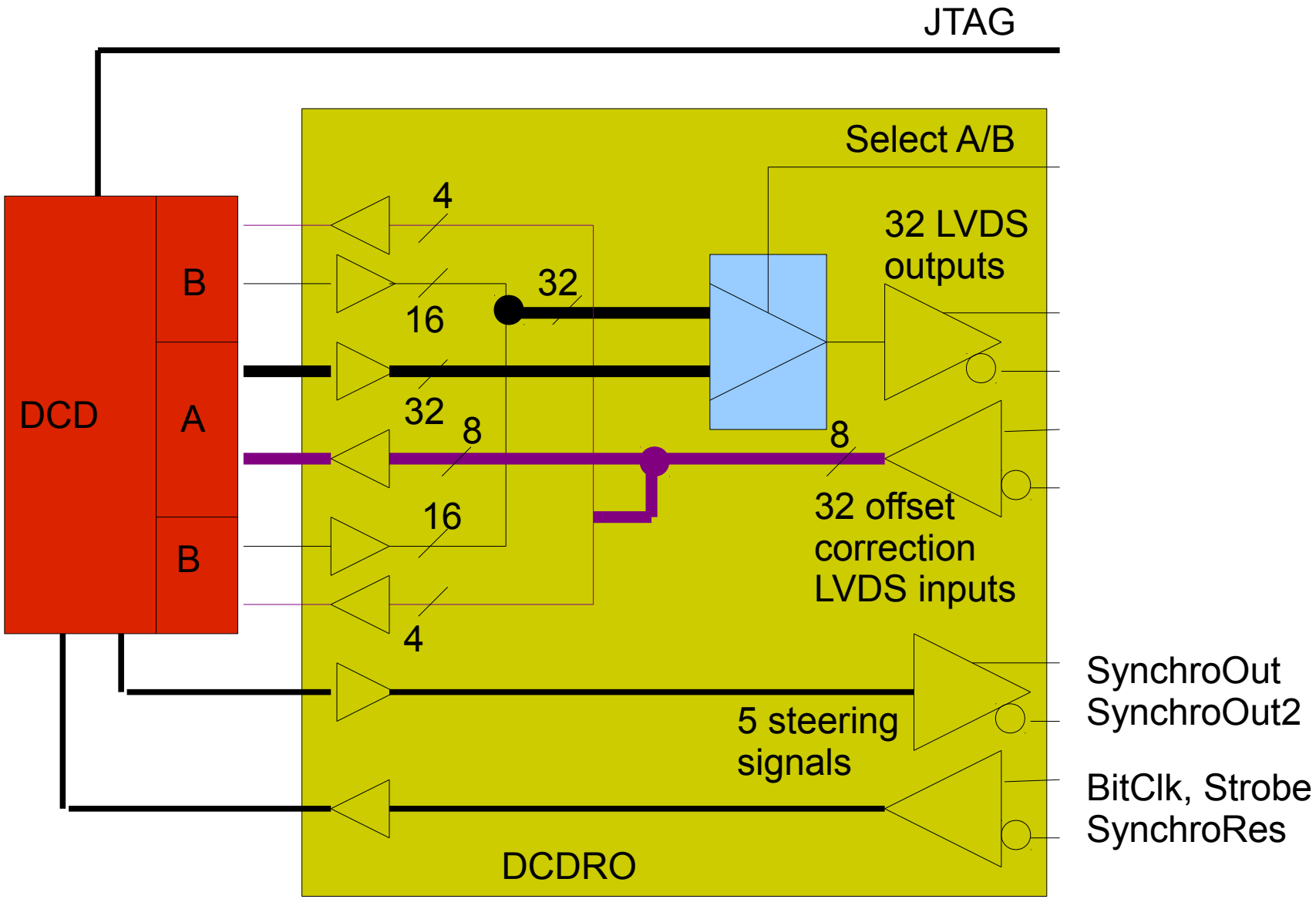
DCDRO Converter Chip

- DCD Outputs are intended to drive DHP inputs closely
  - cannot drive long lines
  - need converter chip if DCD operated without DHP
  - convert SE to LVDS
- 1x2 miniASIC (1525 x 3280µm²)
  - fits DCD width → all DCD I/Os connected
  - chipsize cannot contain LVDS pairs for all DCD I/Os → multiplexer needed
- multiplex between 4 middle and 4 outer DCD slices
  - matrix with 128 drains can be read out without switching



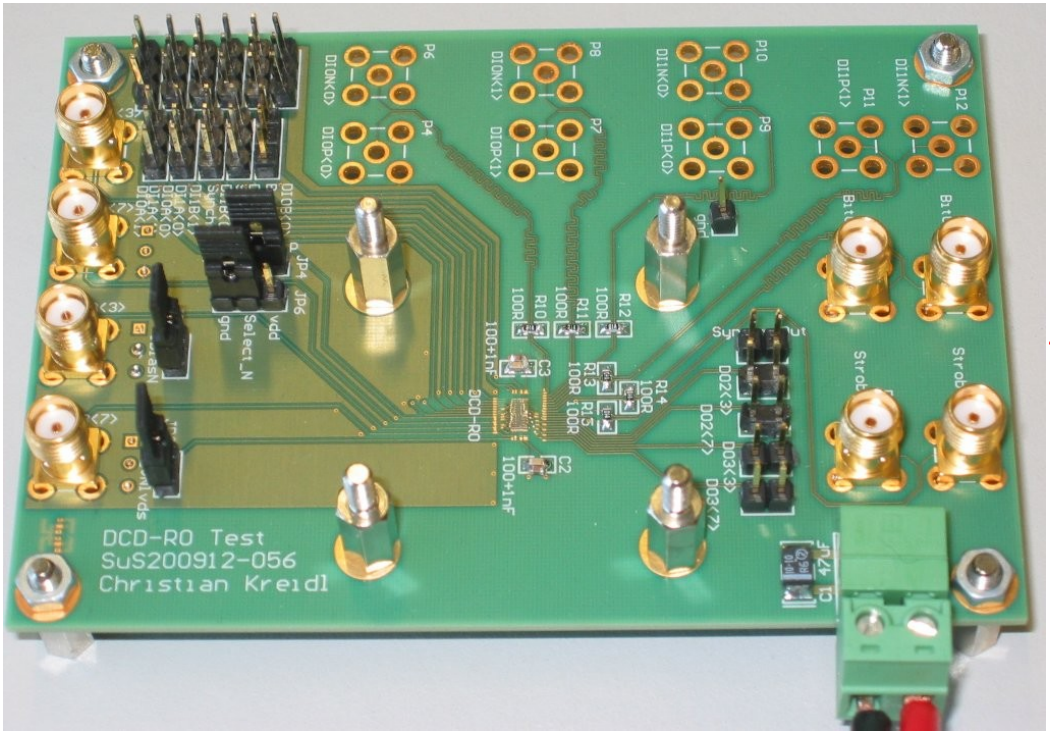


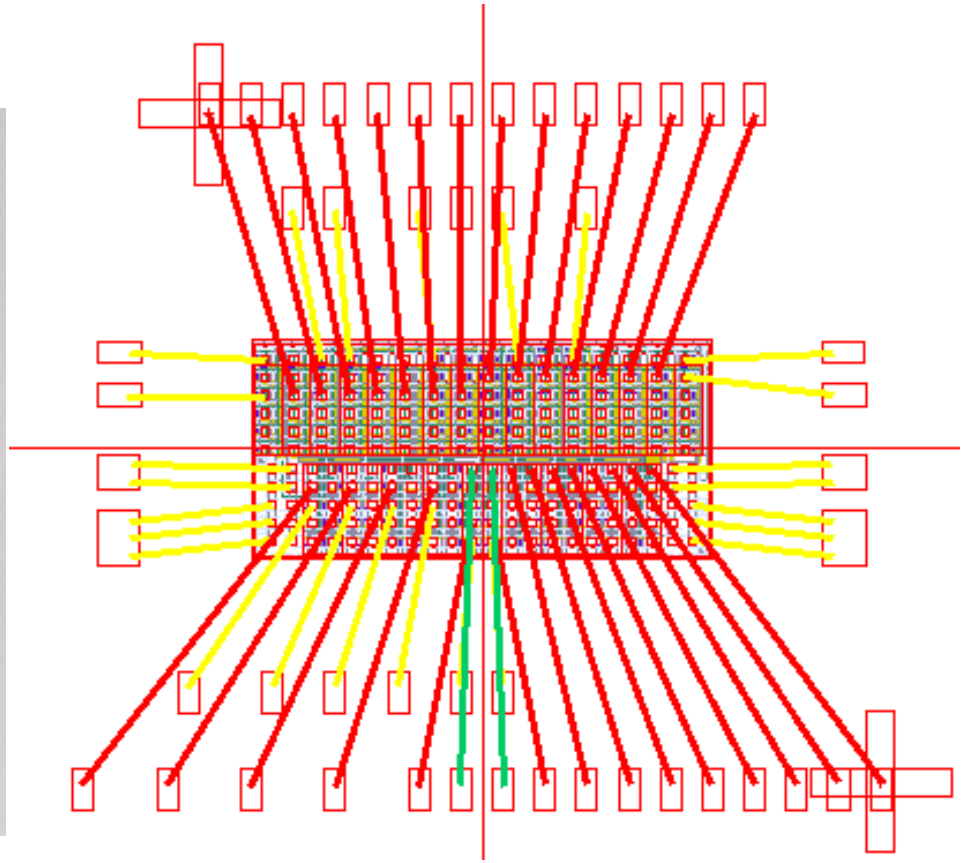
Block Diagram



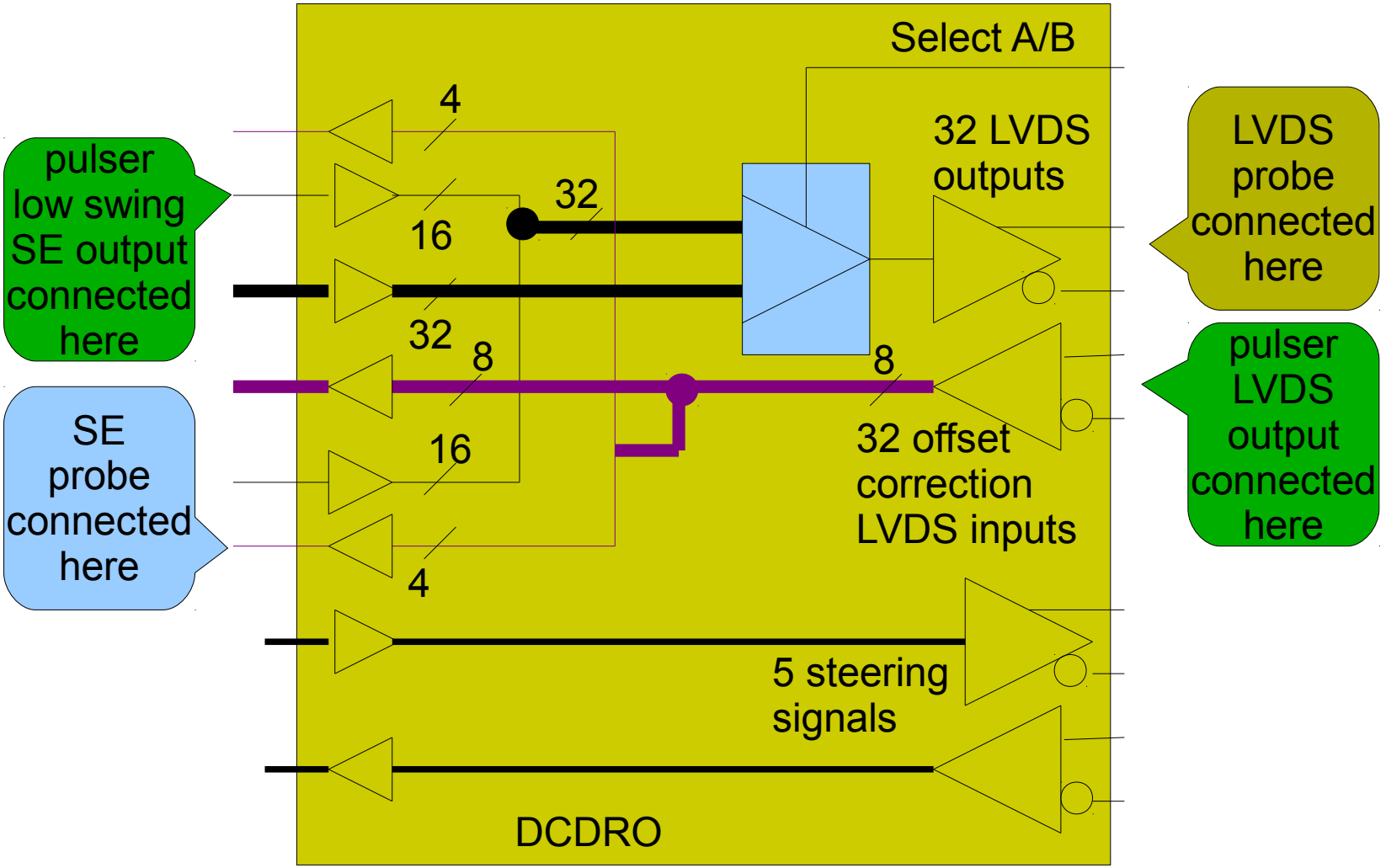
DCD-RO Testing

- PCB was designed to test DCD-RO standalone
  - Wirebonding of some bump pads
  - Differential and Singleended Inputs from Pulser
  - Outputs on Oszi
  - low swing single ended signals from pulser (DCD-B like)
    - 240mV swing



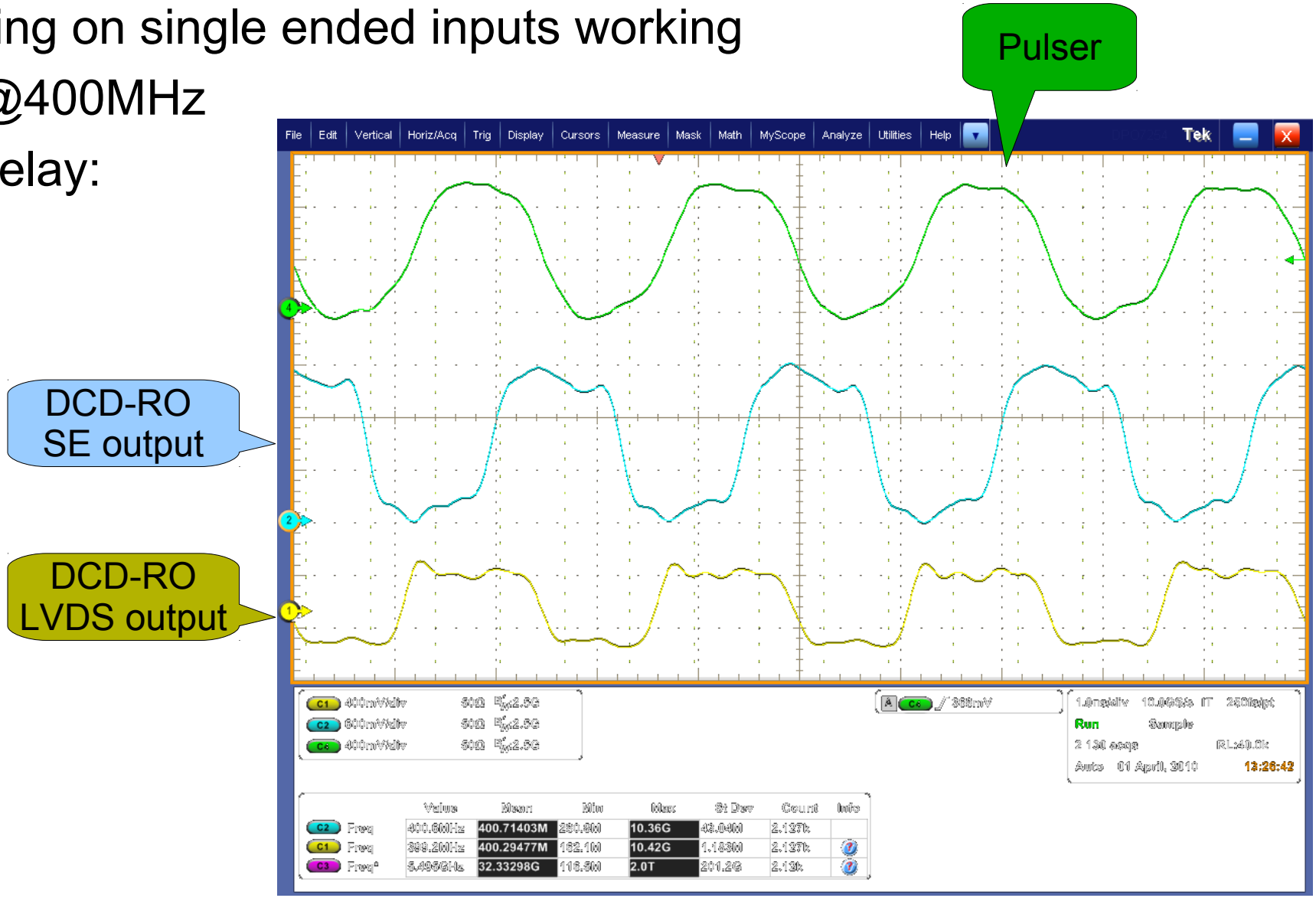


Test Setup


Select A/B
4
32 LVDS outputs
pulser low swing SE output connected here
32
16
LVDS probe connected here
32
8
8
16
SE probe connected here
pulser LVDS output connected here
32 offset correction LVDS inputs
4
5 steering signals
DCDRO

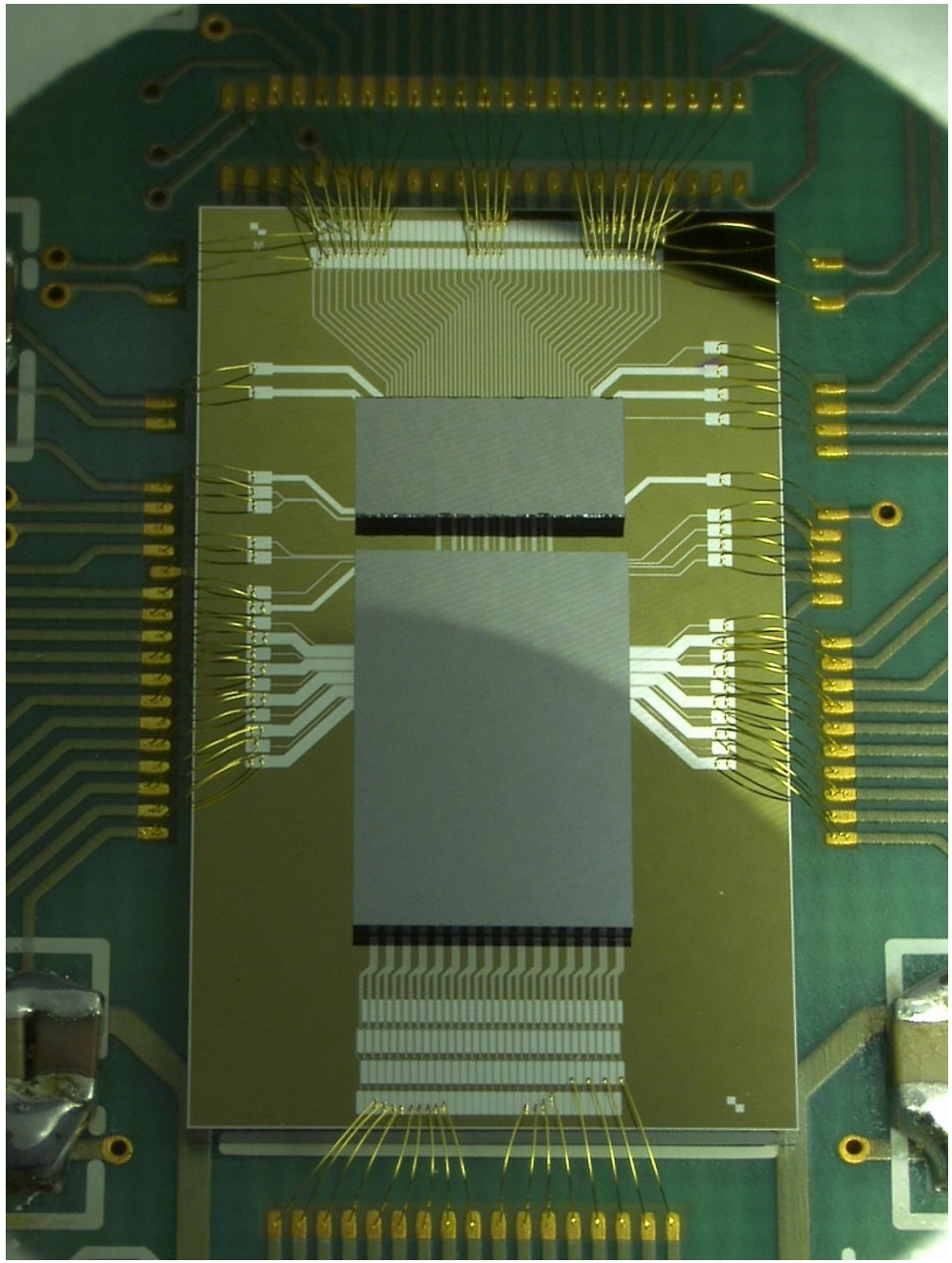
First Results Standalone Tests

- Running with 400MHz
- low swing on single ended inputs working
- 80mA@400MHz
- prop. delay:
  900ps



DCD + DCD-RO

- Wirebondadapter has been assembled
- DCD-RO is working with DCD-B
  - differential signals from/to FPGA ok
  - single ended low swing from DCD-B ok
  - single ended to DCD-B ok
- 120mA@100MHz



Thank You!