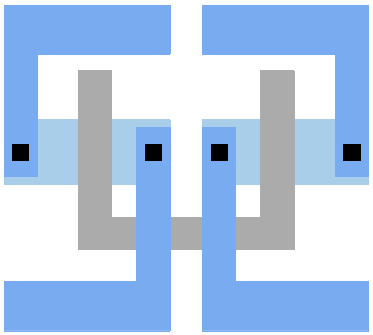
UNIVERSITÄT
HEIDELBERG

First DCDB Test Results



Jochen Knopf
jochen.knopf@ziti.uni-heidelberg.de

DEPFET Collaboration Meeting

Ringberg

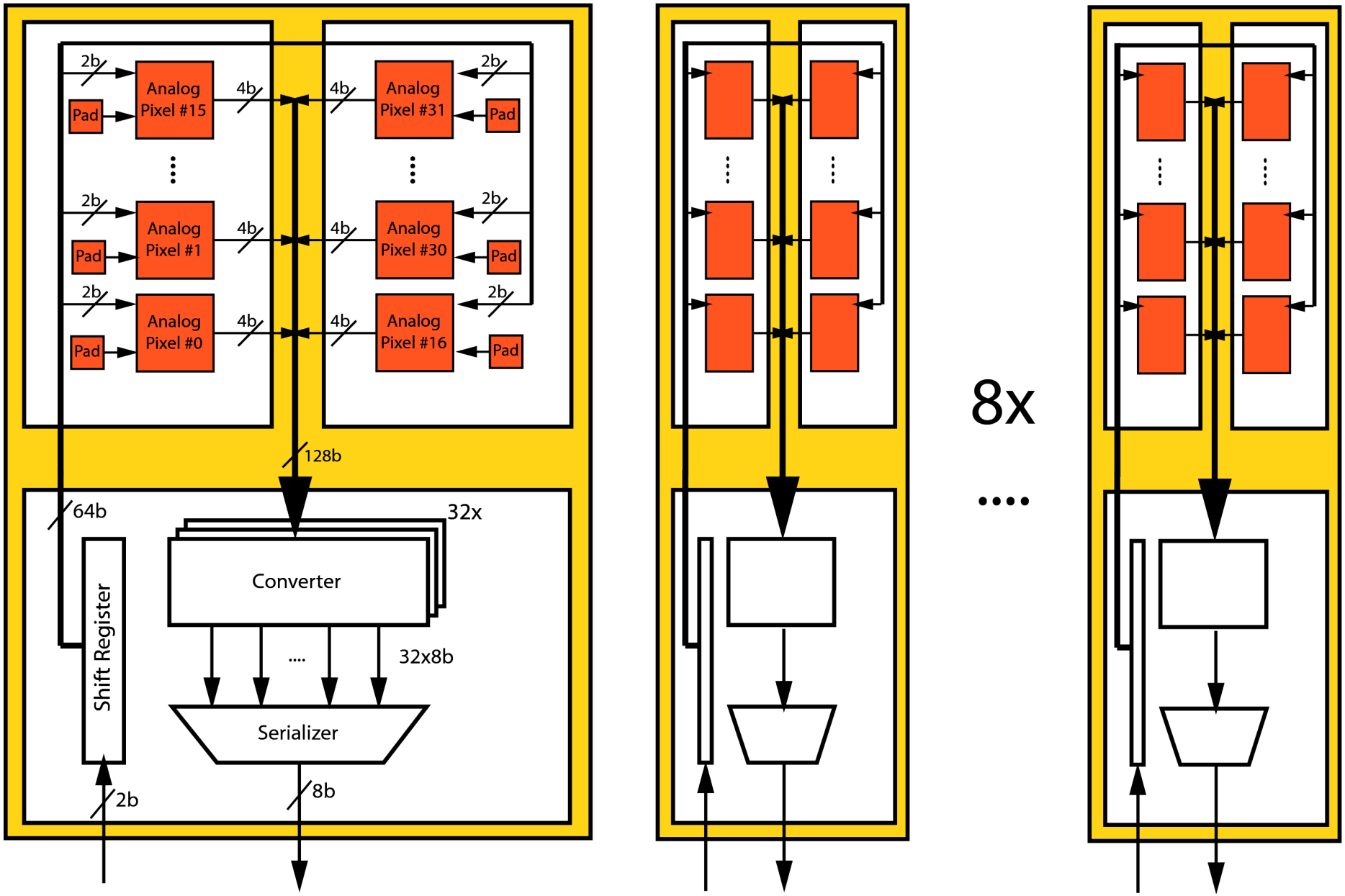
May 3rd , 2010

Outline

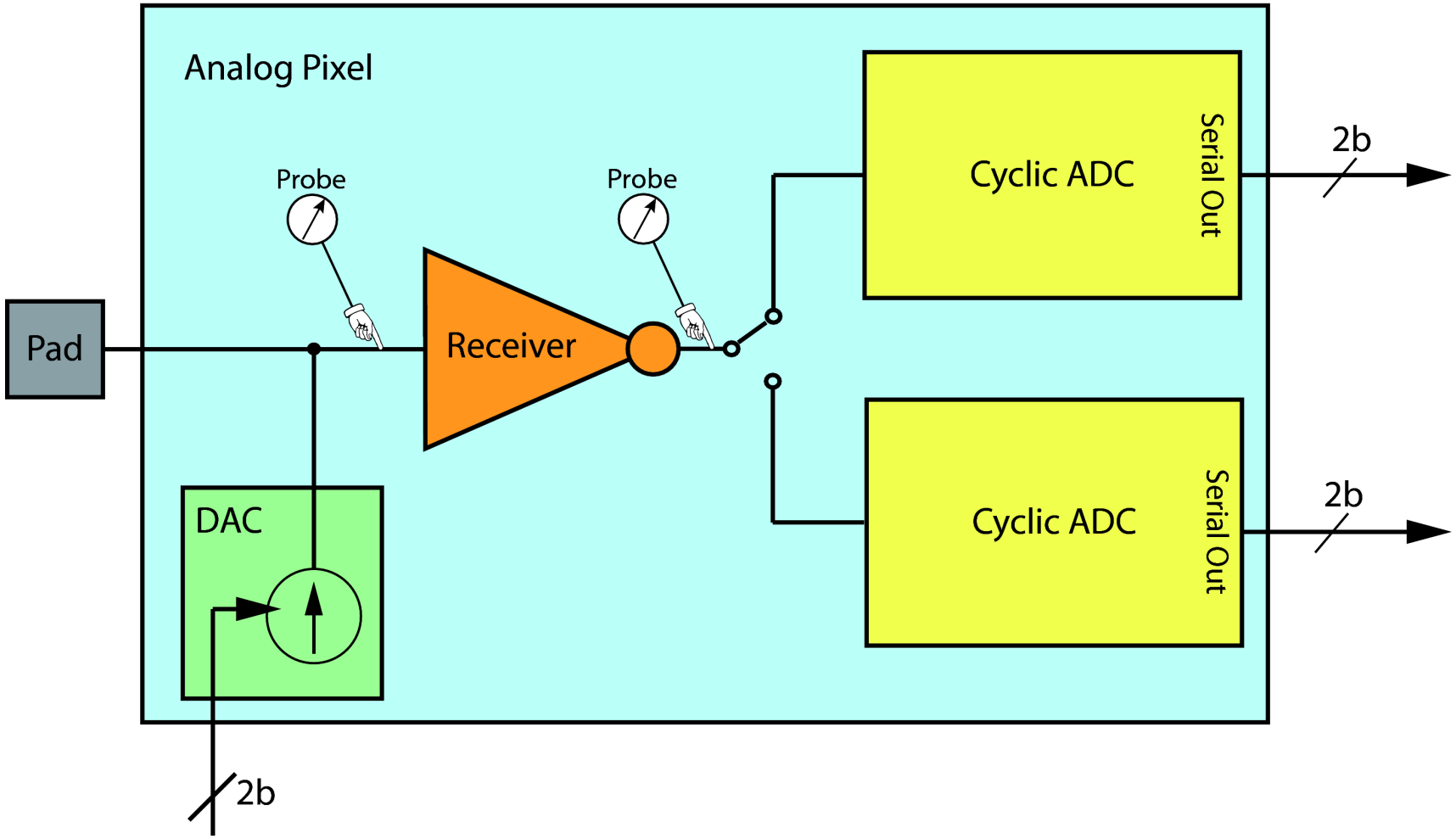
- DCDB Introduction
- DCDB Test Setup
- Measurement Results
- Next Steps

DCDB Introduction

DCDB's Internal Structure (simplified!)



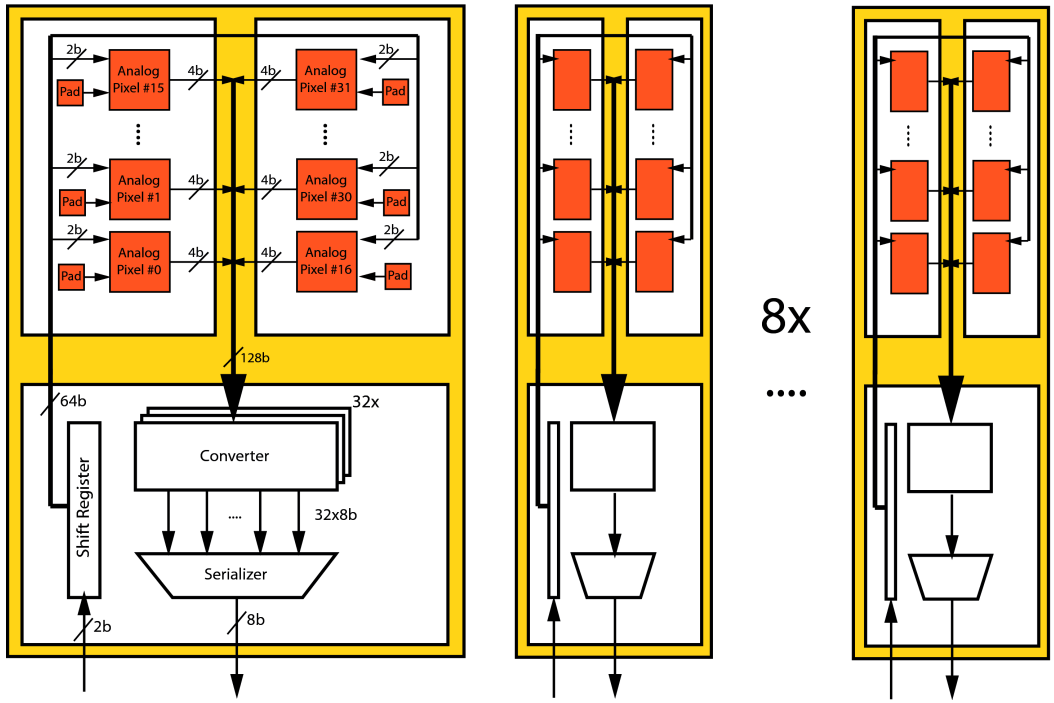
DCDB's Analog Pixel (simplified!)



- DAC: Dynamic offset correction by adding a variable current to the input node
- Receiver: Trans-Impedance Amplifier for amplification of the input current
- Two Cyclic ADCs: Alternatingly converting analog input current to digital value
- Probes: The input and output node of every pixel's receiver is accessible via the monitor pin

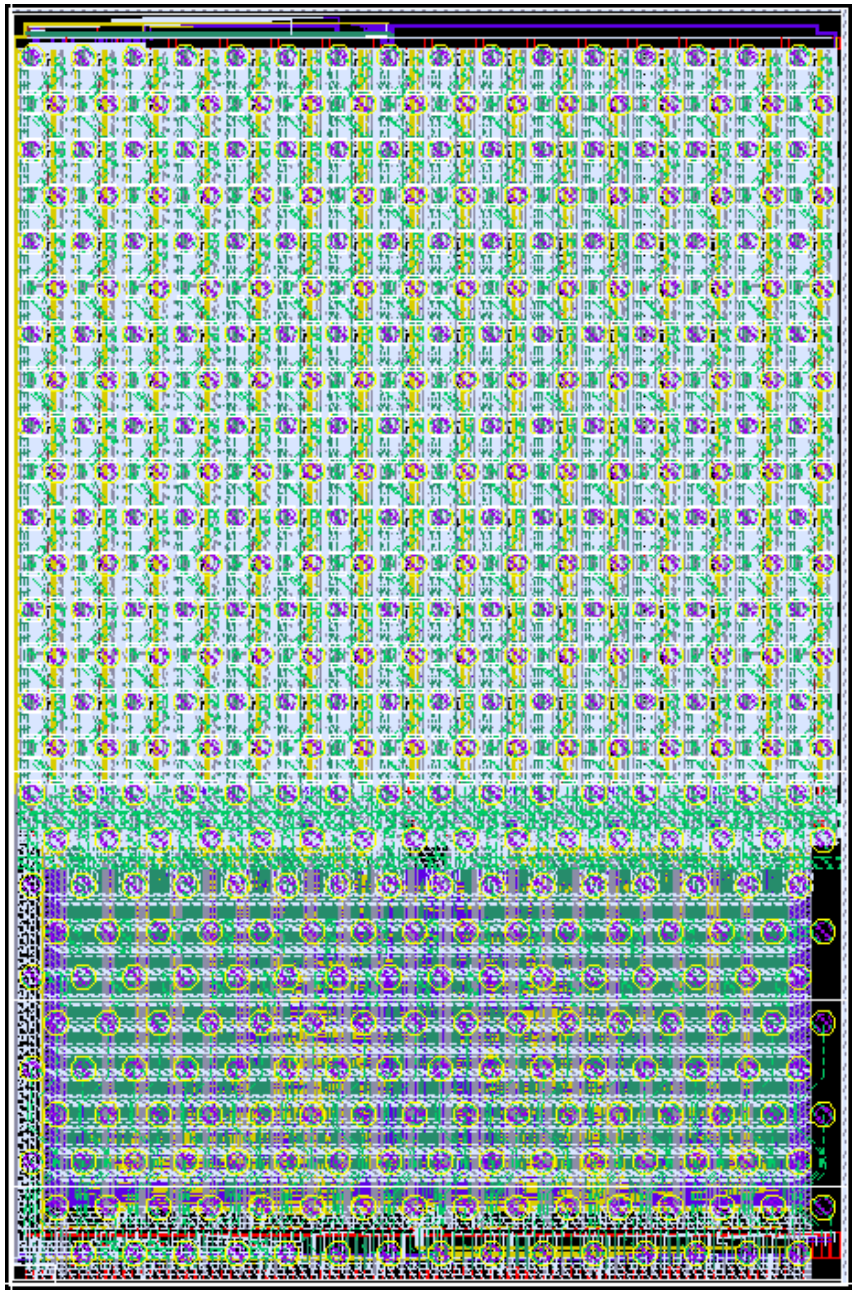
DCDB Main Features

- 256 ADC channels
  - 9 Bit data output
  - Dynamic offset adjustment
  - 80ns target sampling period
- Fully synthesized digital readout and control block
- 8x 8 Bit data output @ 400MHz
- JTAG configuration interface

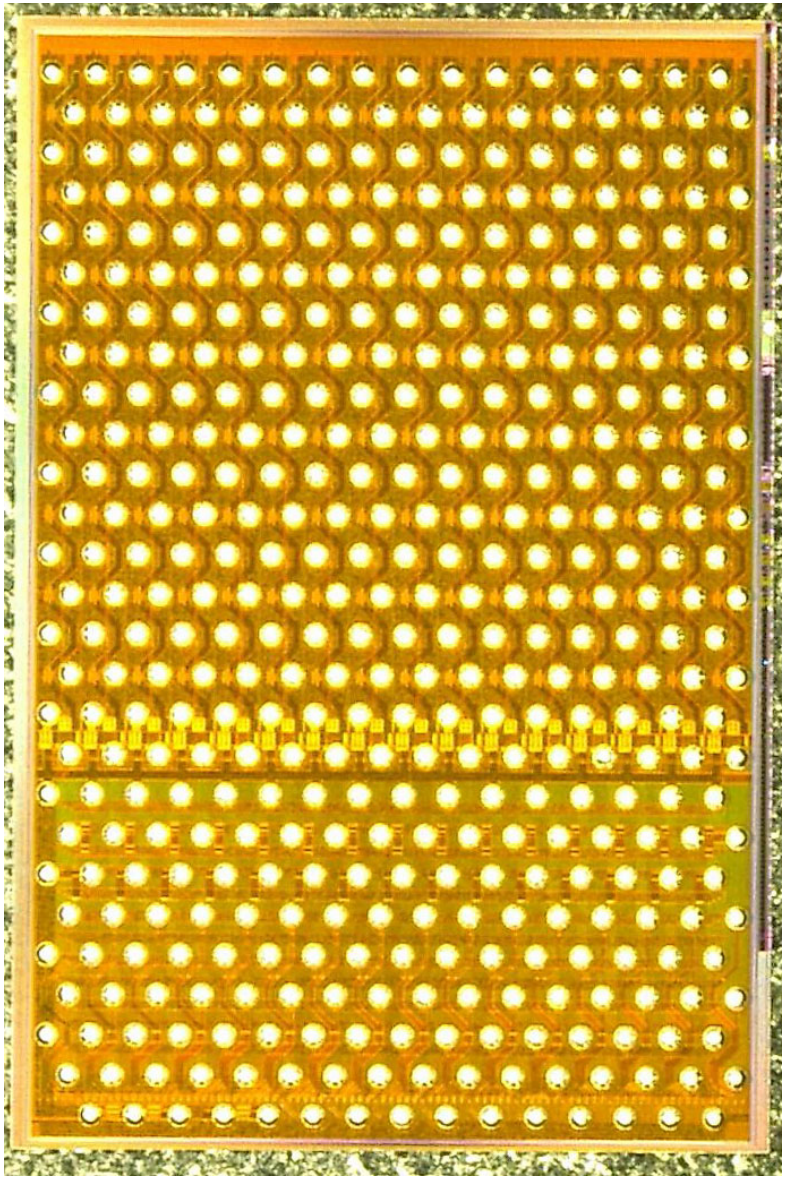


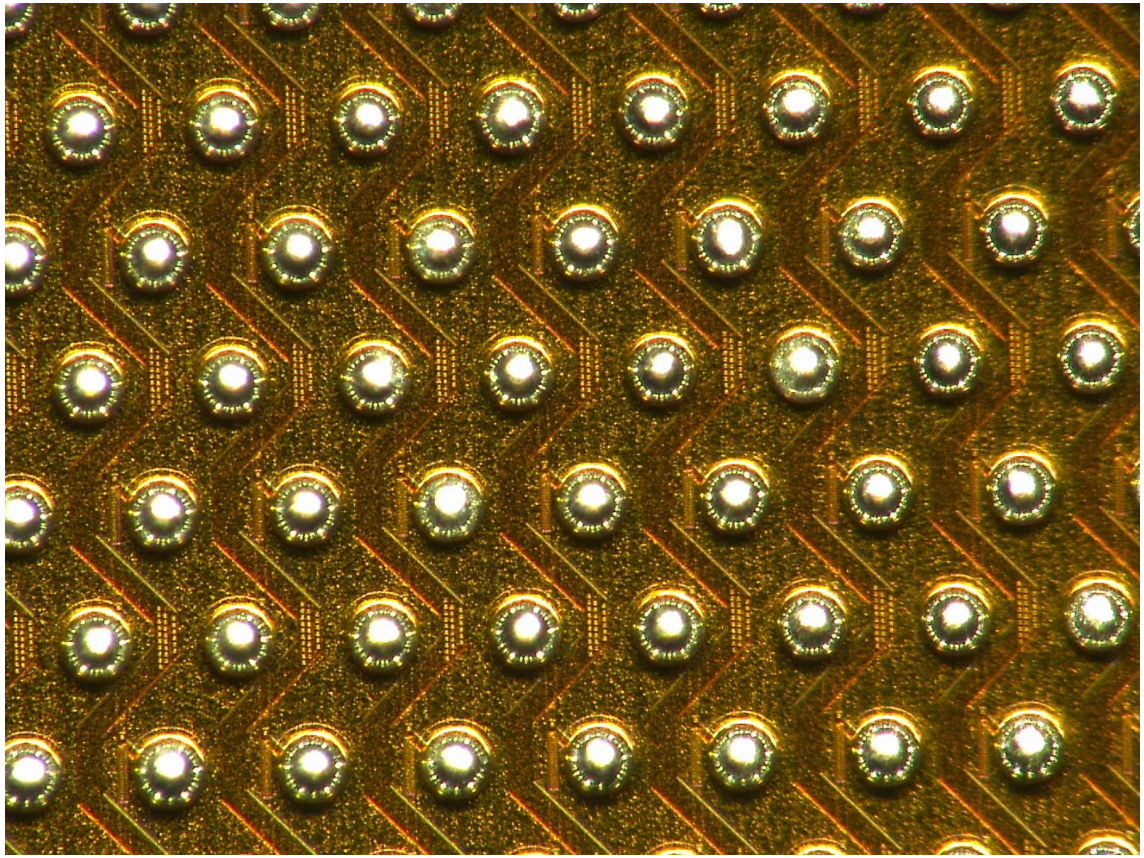
DCDB Production Details

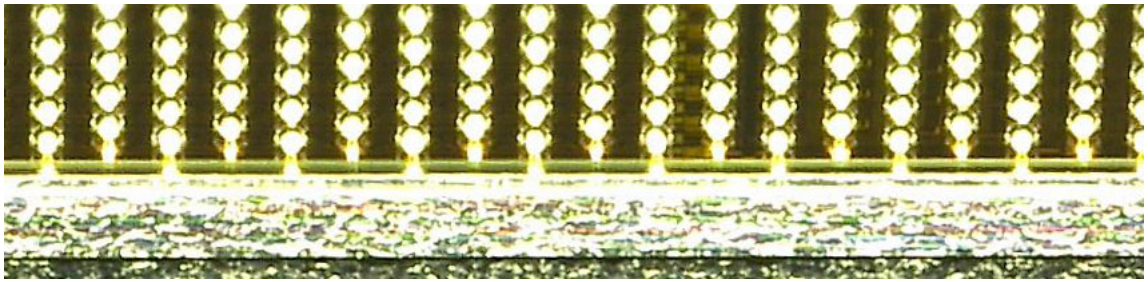
- Implemented in UMC 180nm CMOS technology
- Area: 3240x4969 µm²
  ~ 2x3 Mini@sic Blocks
- Additional 7th metal layer (redistribution layer) with bump-bond pads including bumps
- Production costs: ~ 20800 EUR (for 60 pcs.)
- Production time: 3 + 2 months



DCDB Pictures

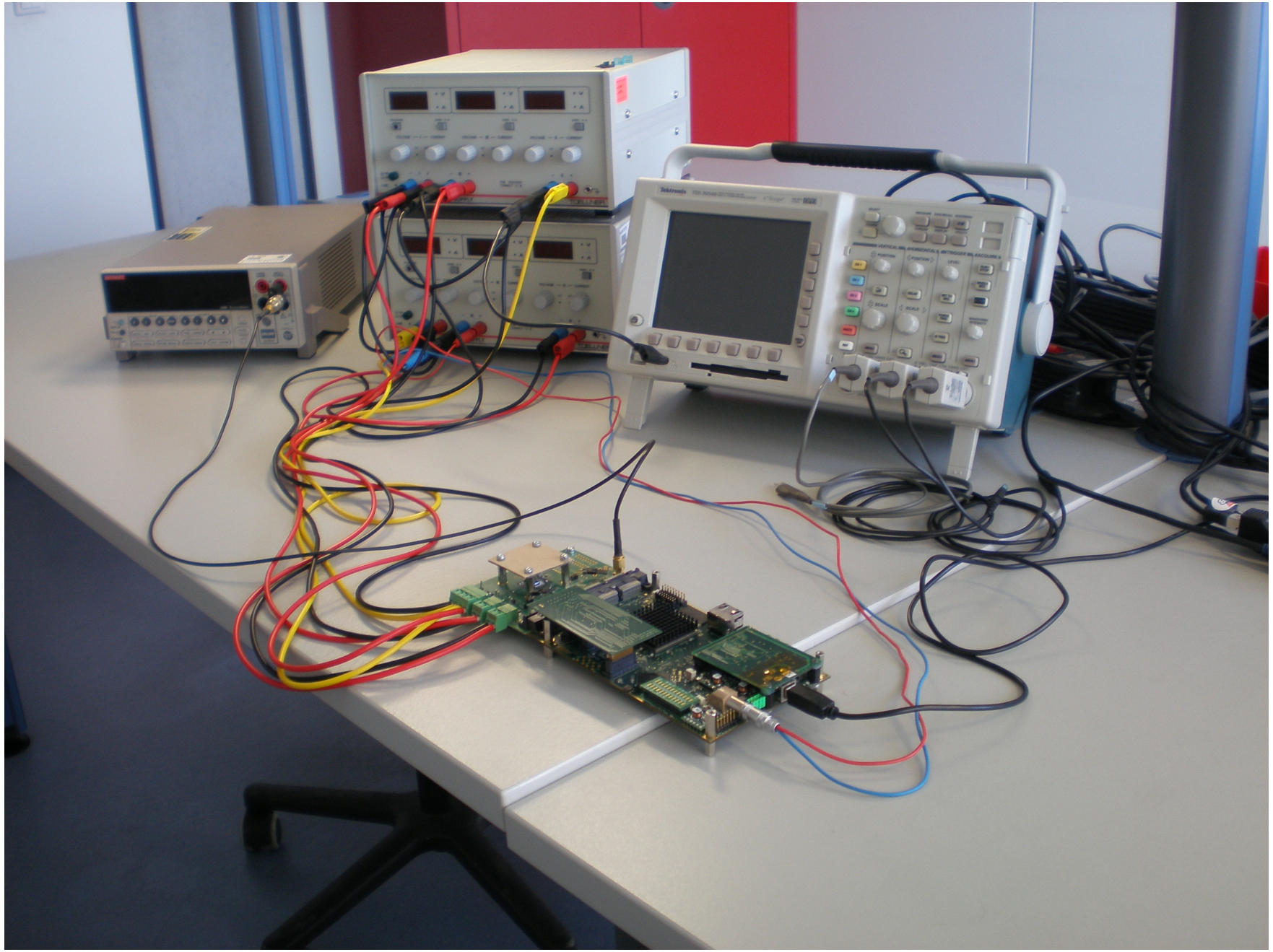




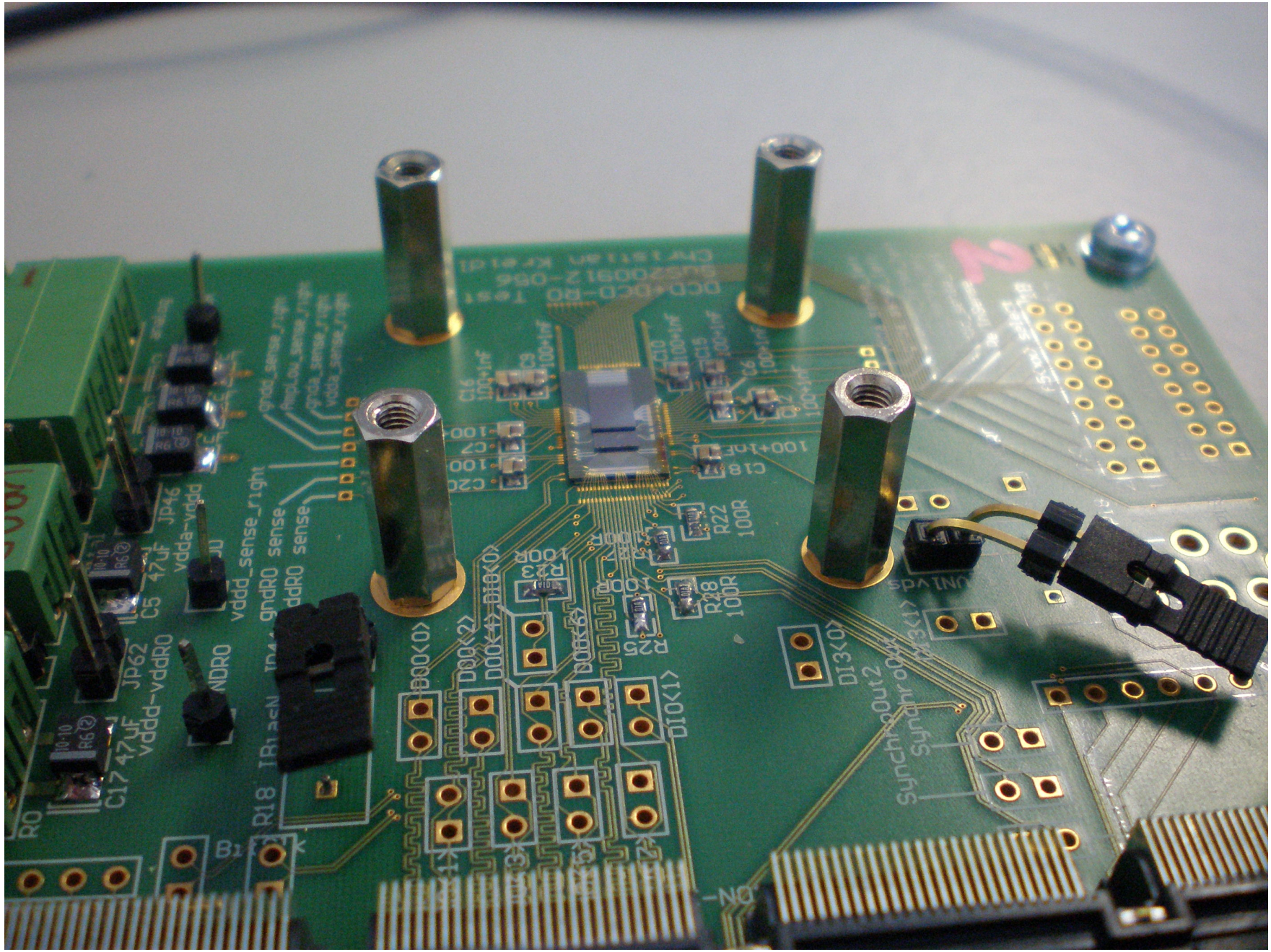


DCDB Test Setup

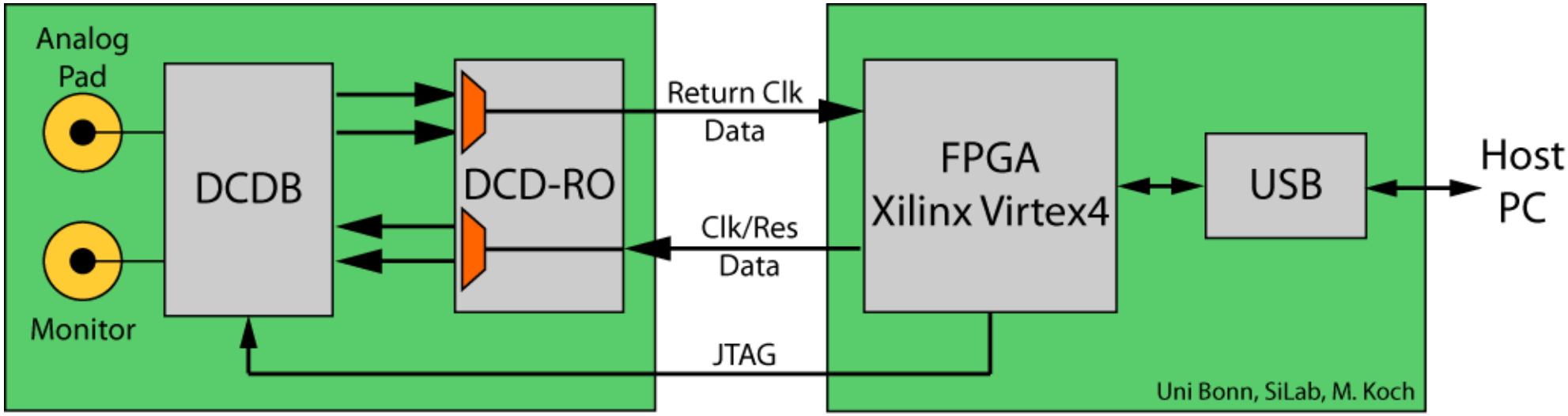
DCDB Test Environment: Pictures



DCDB Test Environment: Pictures

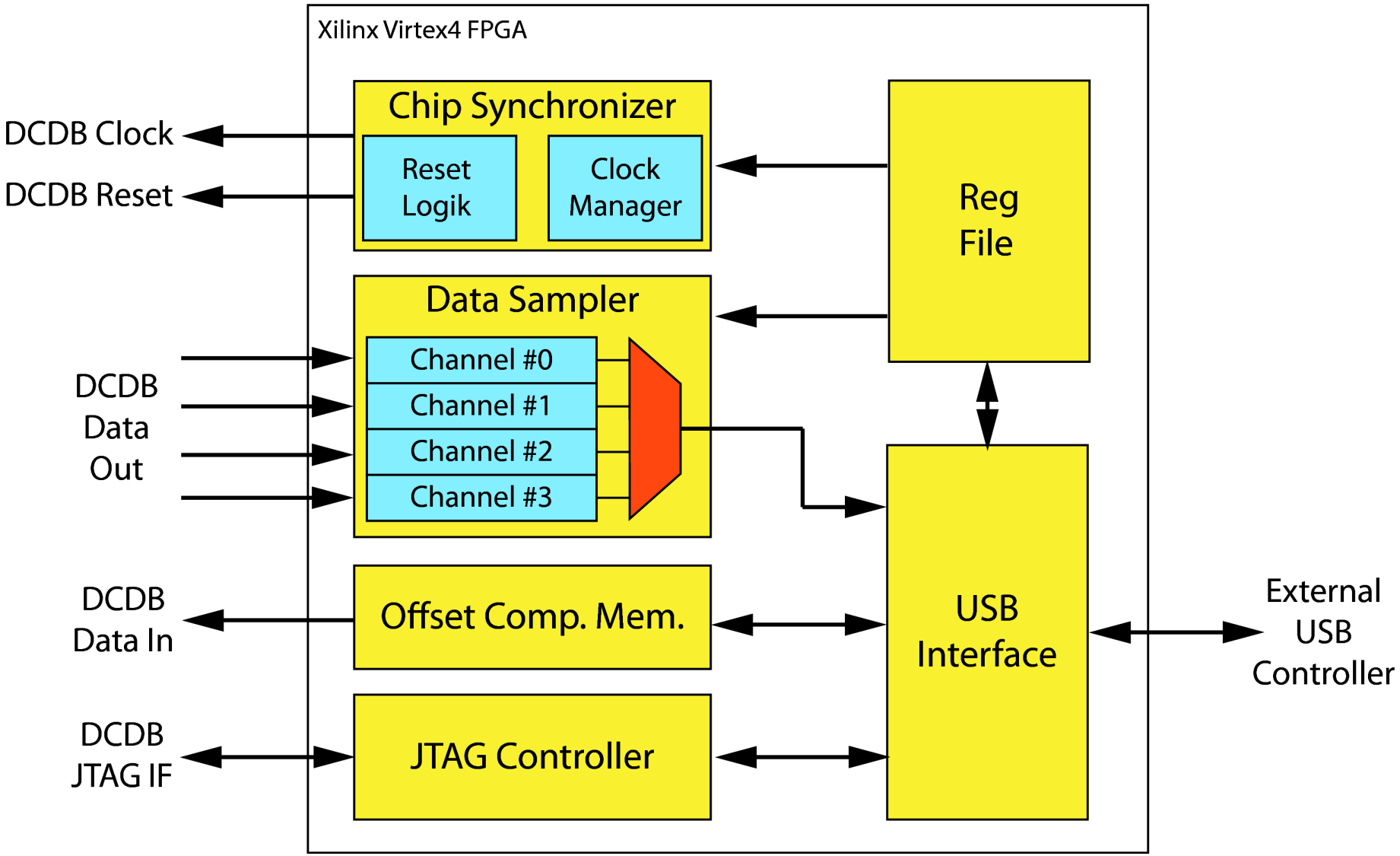


DCDB Test Environment: Hardware



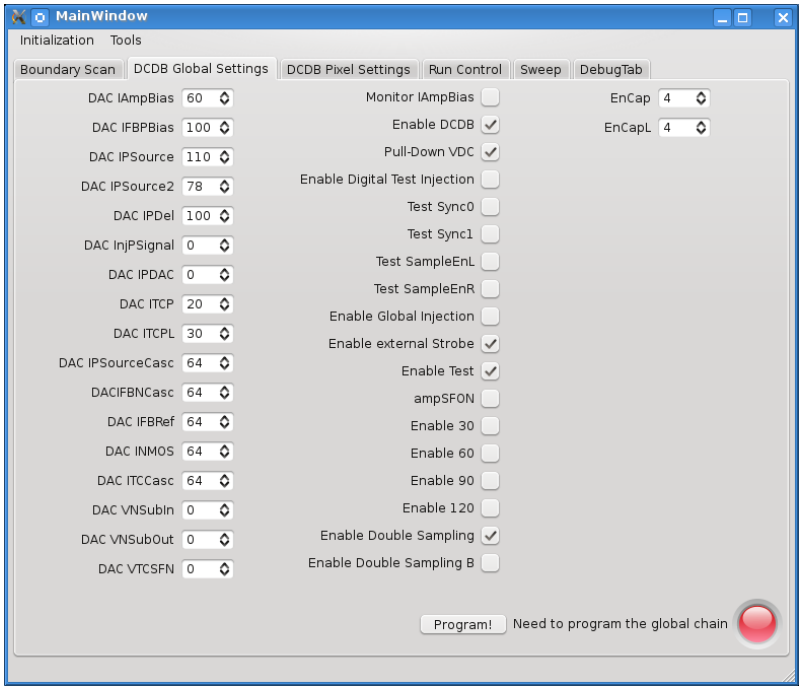
- The test environment is based on the SiLab's (Uni Bonn) Virtex4-Board
- The DCD-RO is used for signal conversion and static 2:1 multiplexing
- SMA connectors bonded to the monitor and some of the analog input pads provide direct access to the DCDB's analog pixel
- The FPGA is used for configuring, controlling and reading the DCDB

DCDB Test Environment: FPGA Firmware Details



Modular Setup: All of these Blocks are reusable for the PXD read out system!

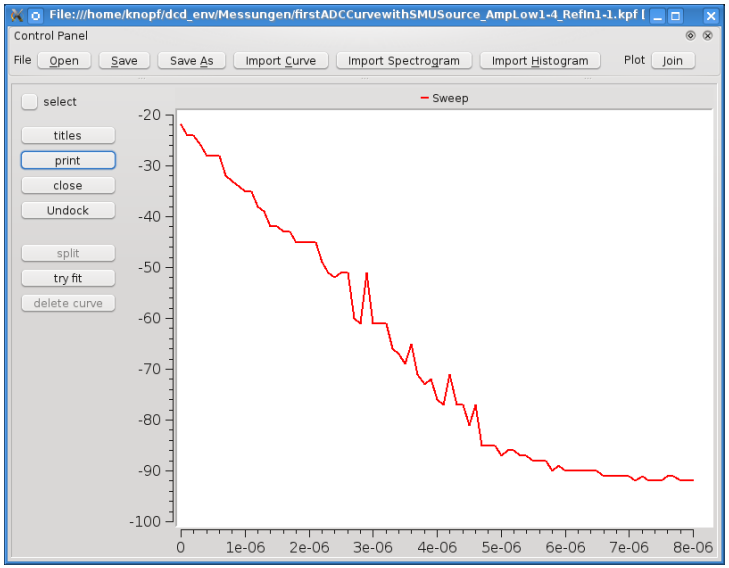
DCDB Test Environment: Software



- Read / plot raw data
- Using KUPE – our group's plot environment

Features:

- Scanning the DCDB's boundary Chain (JTAG)
- Configuring the DCDB's DACs and Registers (JTAG)
- Control the DCDB clocking
- Manipulate the data sampling (DCDB's data into the FPGA)
- Perform automated measurements (e.g. parametric sweep)



Measurements

Measurements: Power Consumption

	Clock Off	100 MHz	200 MHz	400 MHz (extrapolated)
VDDA [mA]	225 (max. 357)	231 (max. 362)	238 (max. 370)	259 (max. 390)
VDDD [mA]	78	131	183	290
RefIn [mA]	18	28	28	28
AmpLow [mA]	129 (max. 250)	128 (max. 250)	128 (max. 250)	128 (max. 250)
Total Power [W]	0,56 (max. 0,8)	0,68 (max. 0,92)	0,79 (max. 1,02)	1,02 (max. 1,25)

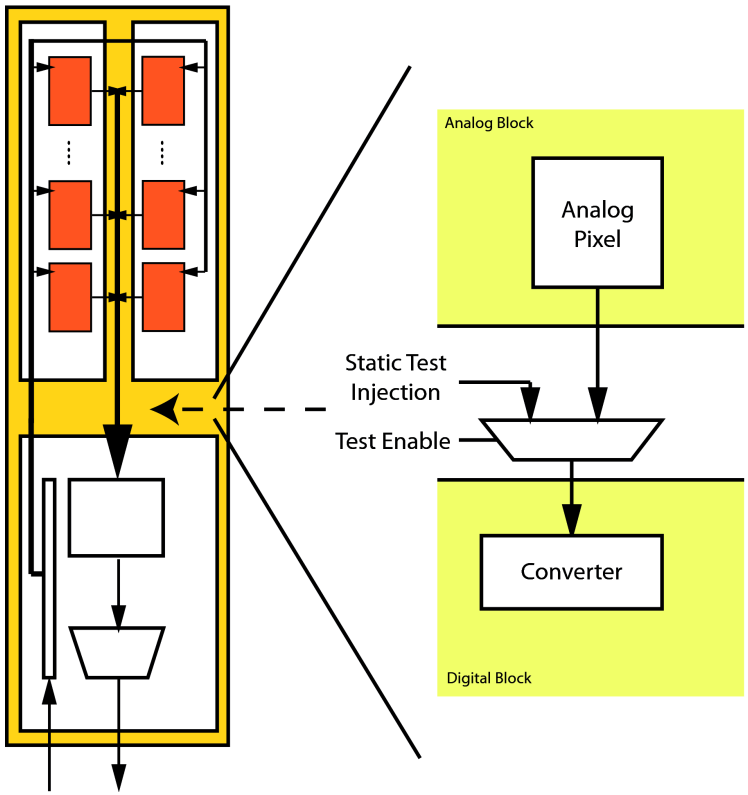
Compare to estimated total power consumption
@400MHz after design phase (→ simulated): 1,56W

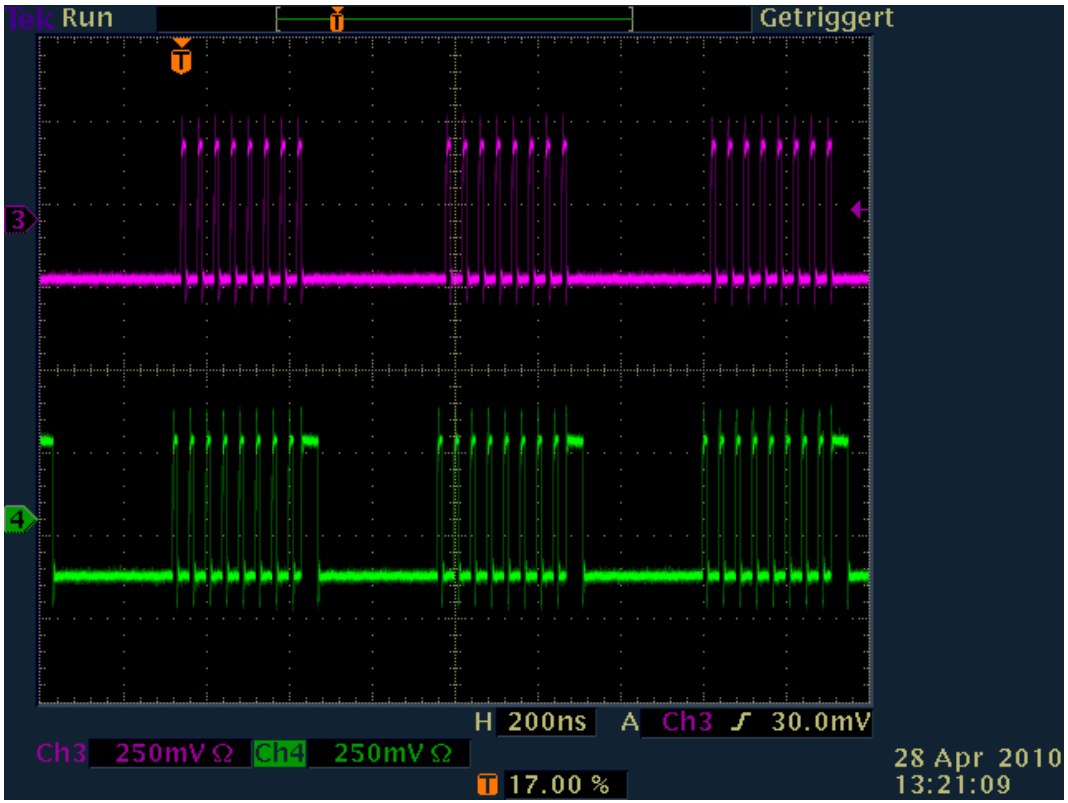
Measurement: Digital Block's Functionality

Successes:

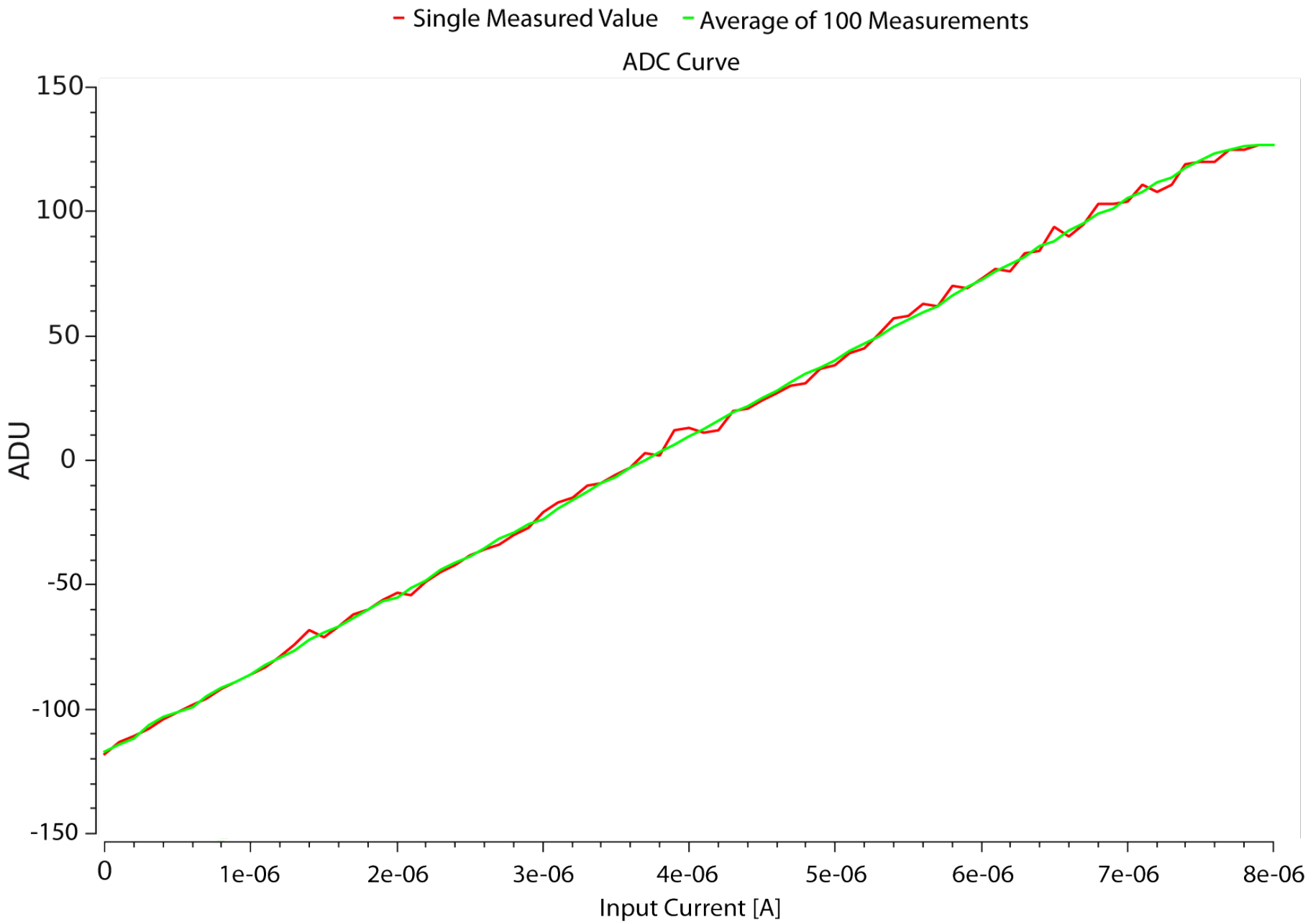
1. Observable control signal behave as simulated (ADC Control, Return Clock)
2. Internally generated test pattern is produced correctly.

Note: The timing for the synchronous reset seems to be critical

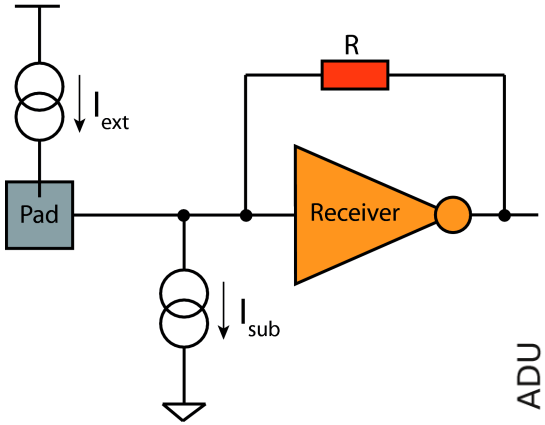


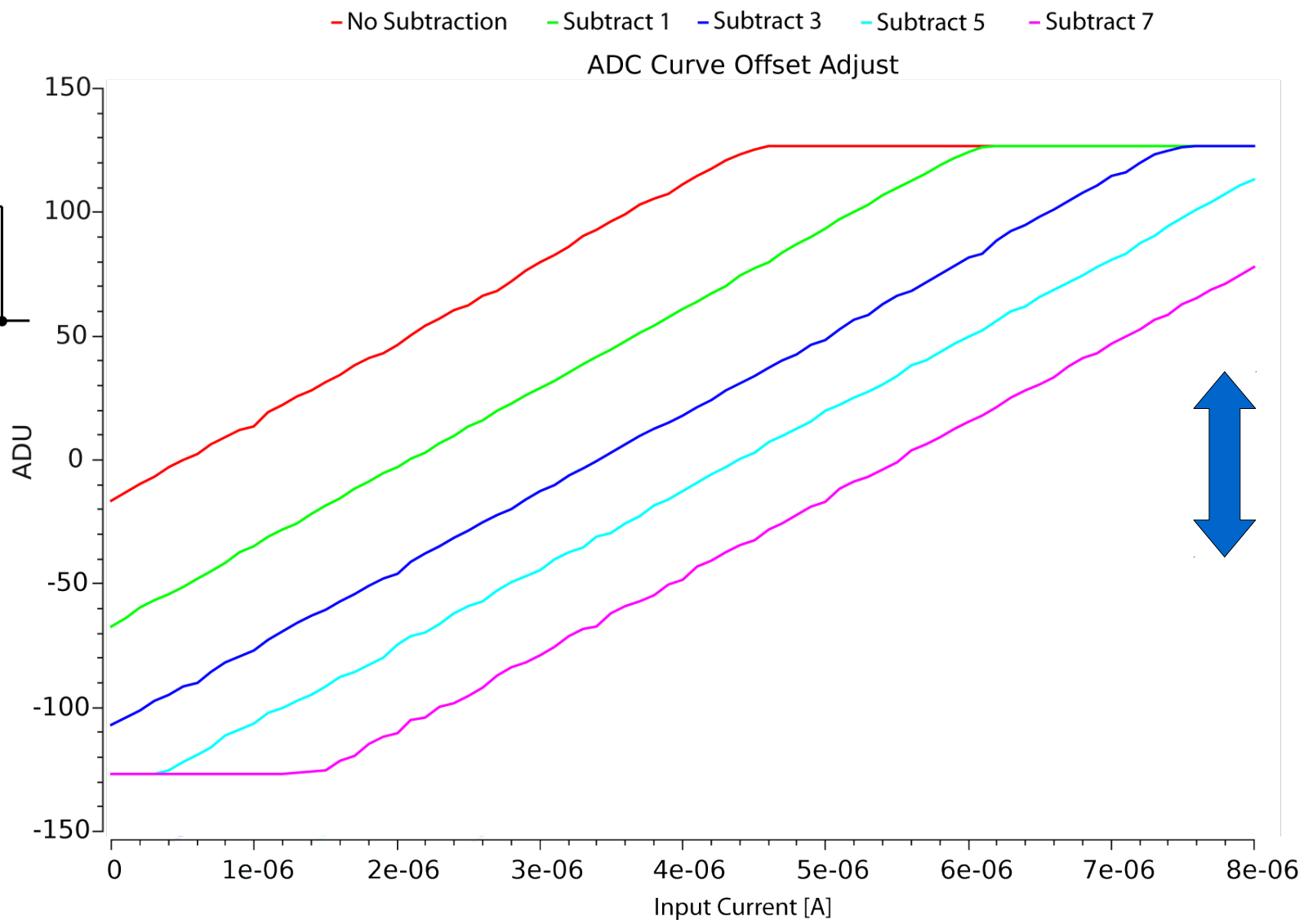


ADC's First Characteristic Curve

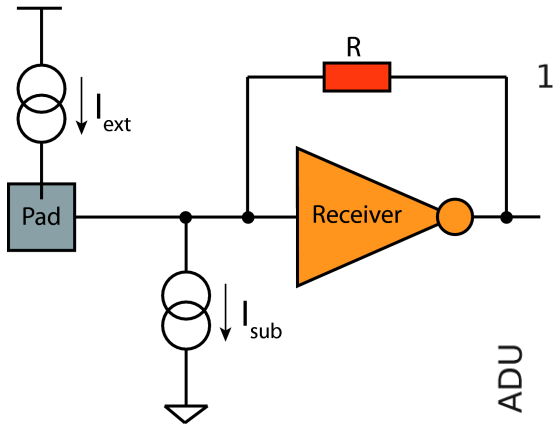


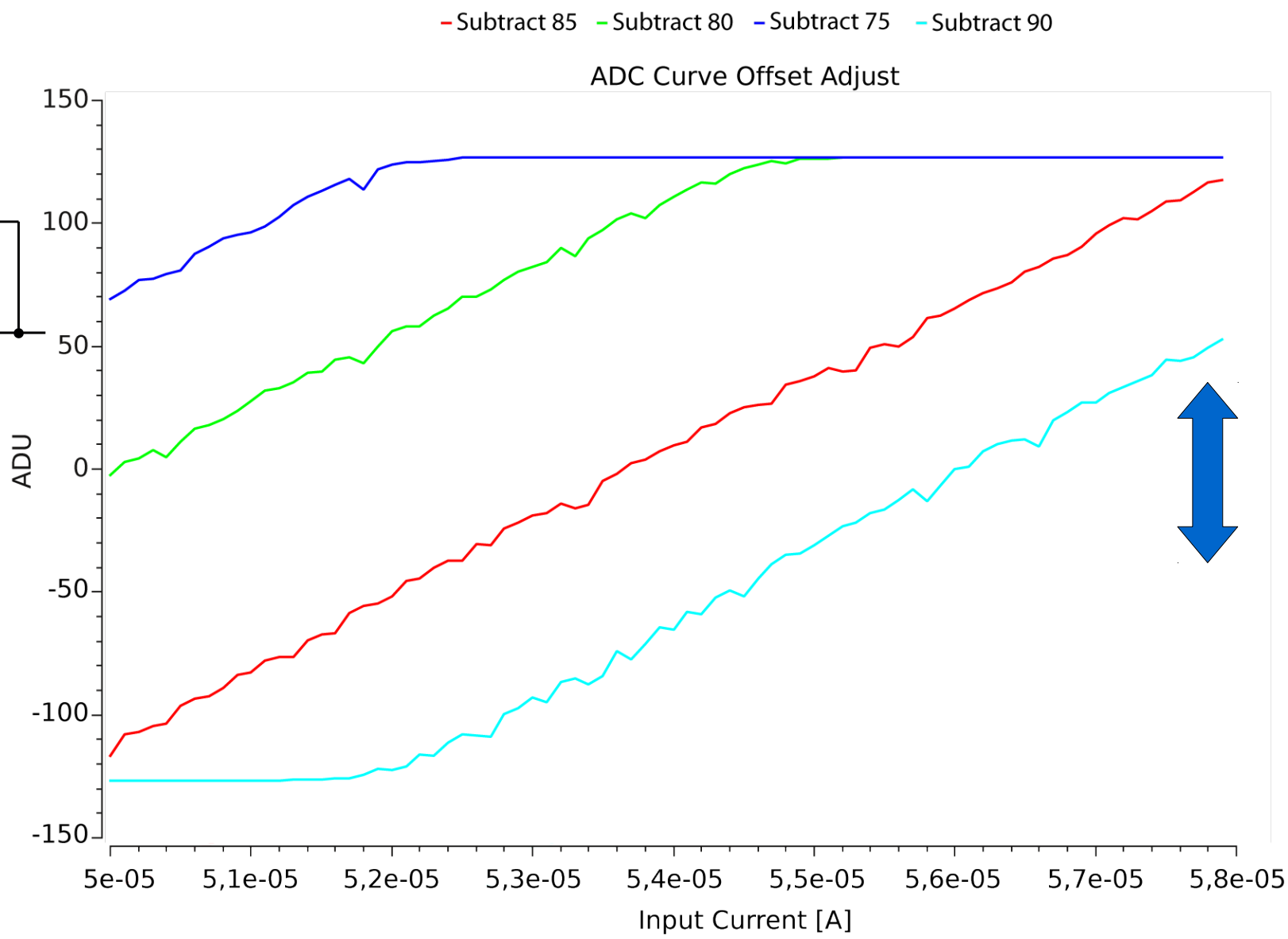
ADC Curve: Offset Adjustment (1/2)



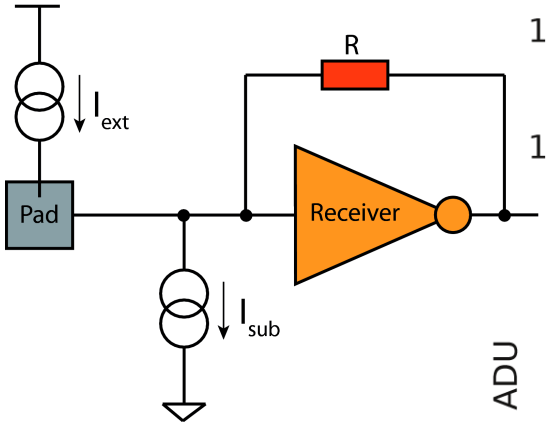


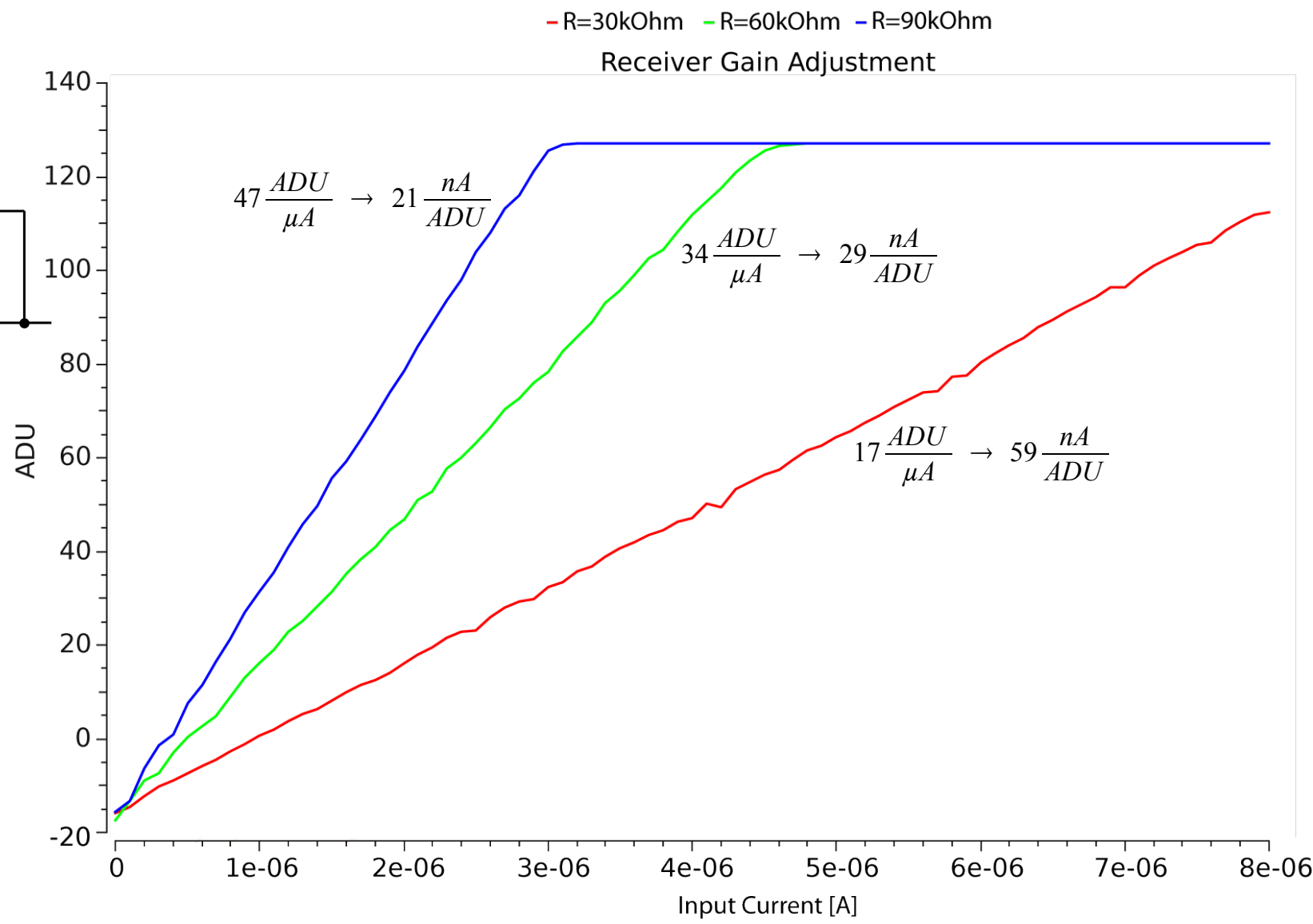
ADC Curve: Offset Adjustment (2/2)



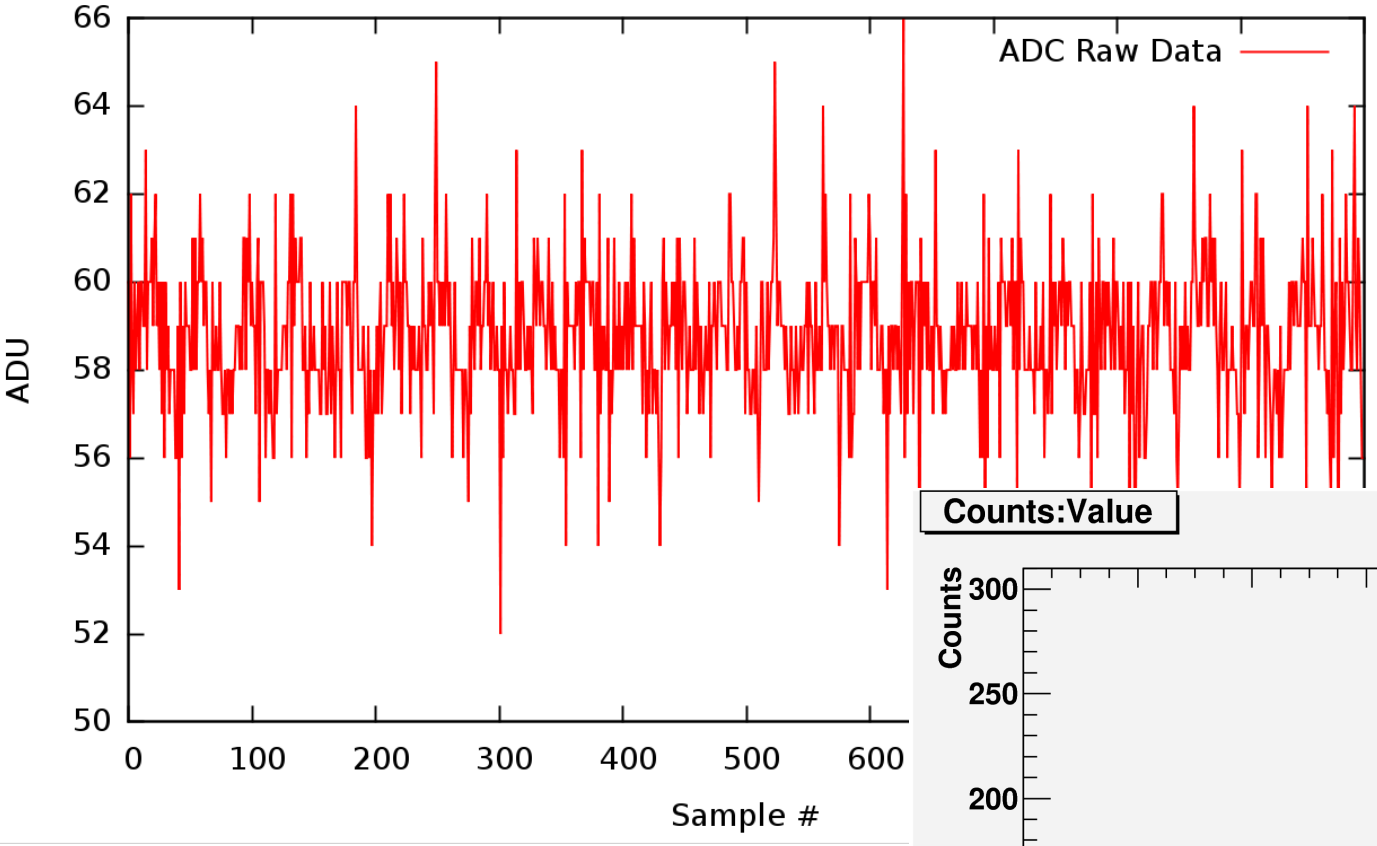


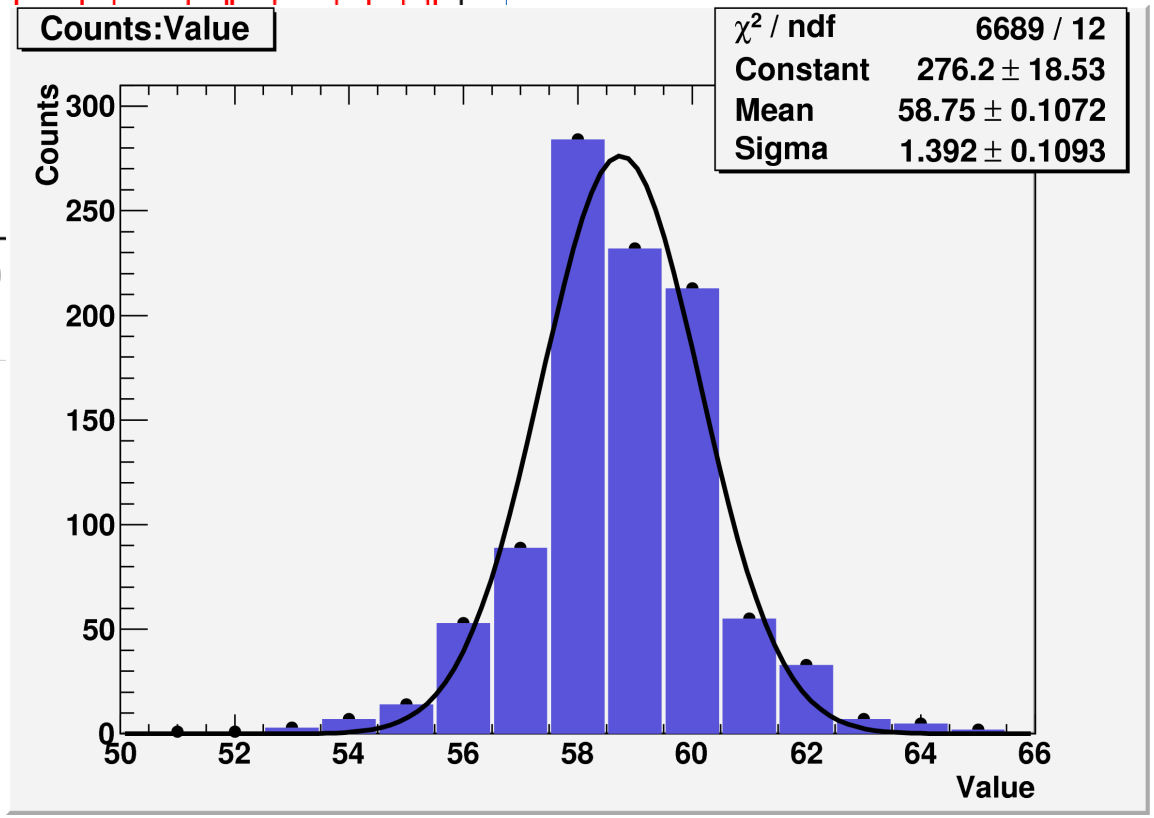
ADC Curve: Gain Adjustment





ADC Curve: Noise





Setting:
Feedback Resistor = 60k

Sigma = 1.392 ADU corresponds to 40nA

Summary

- ✔ DCDB production is finished. The 7th metal layer / bump bond process seems to work
- ✔ Test environment is set up: DCD-RO, bumping, PCB, FPGA firmware, software
- ✔ Power consumption within the expected range
- ✔ JTAG configuration interface is operating
- ✔ JTAG Boundary Scan is operating
- ✔ Digital data conversion and serialization is working
- ✔ ADC's point of operation is found

Next steps:

- Investigate reset timing
- Still some fine-tuning necessary
- Check offset compensation mechanism
- Check double correlated sampling mechanism
- Characterization of every pixel
- Find maximum operation frequency (probably PCB upgrade necessary)

Thank you!