RUPRECHT-KARLS-
UNIVERSITÄT
HEIDELBERG

SWITCHER-B

Status

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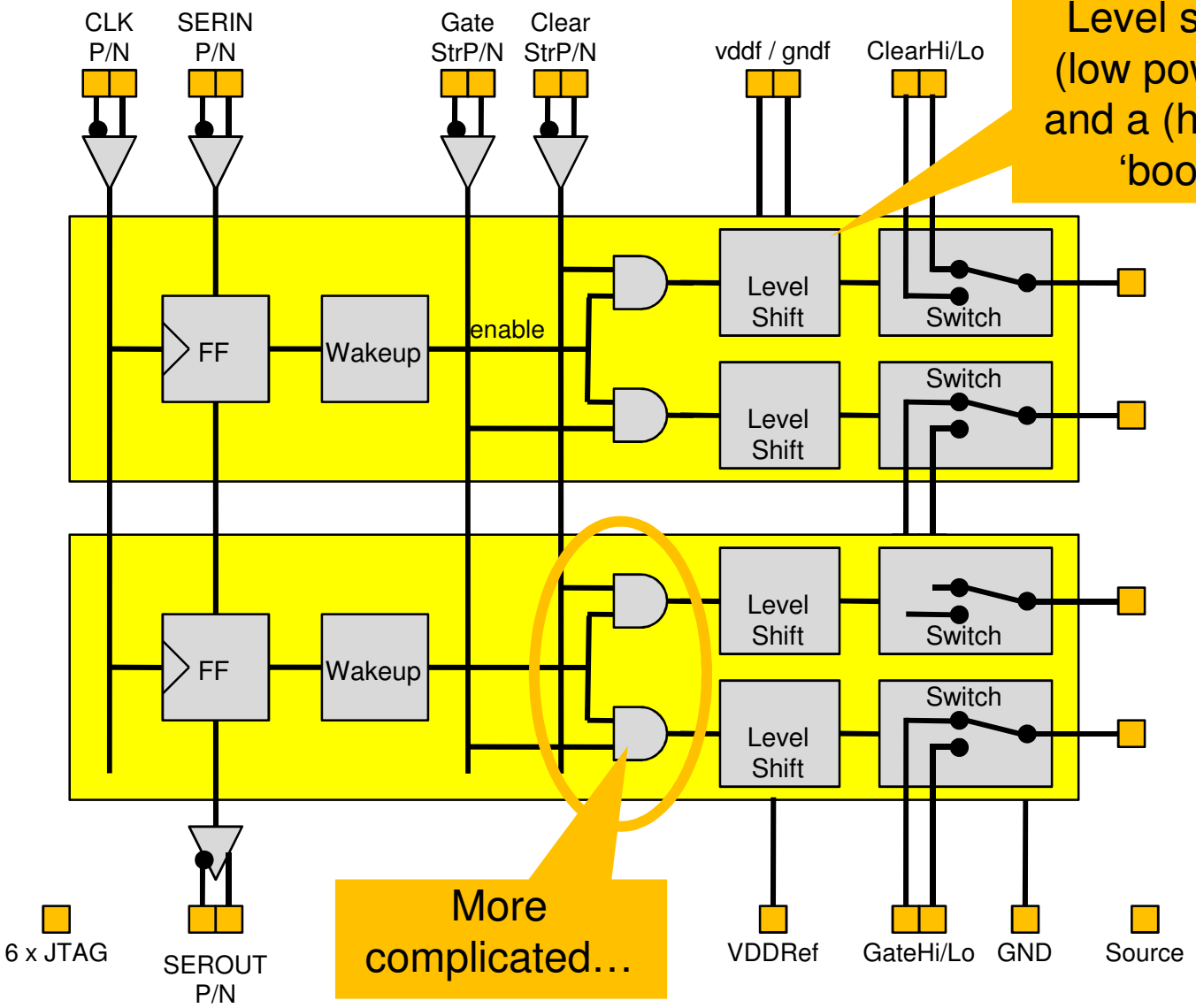
Summary

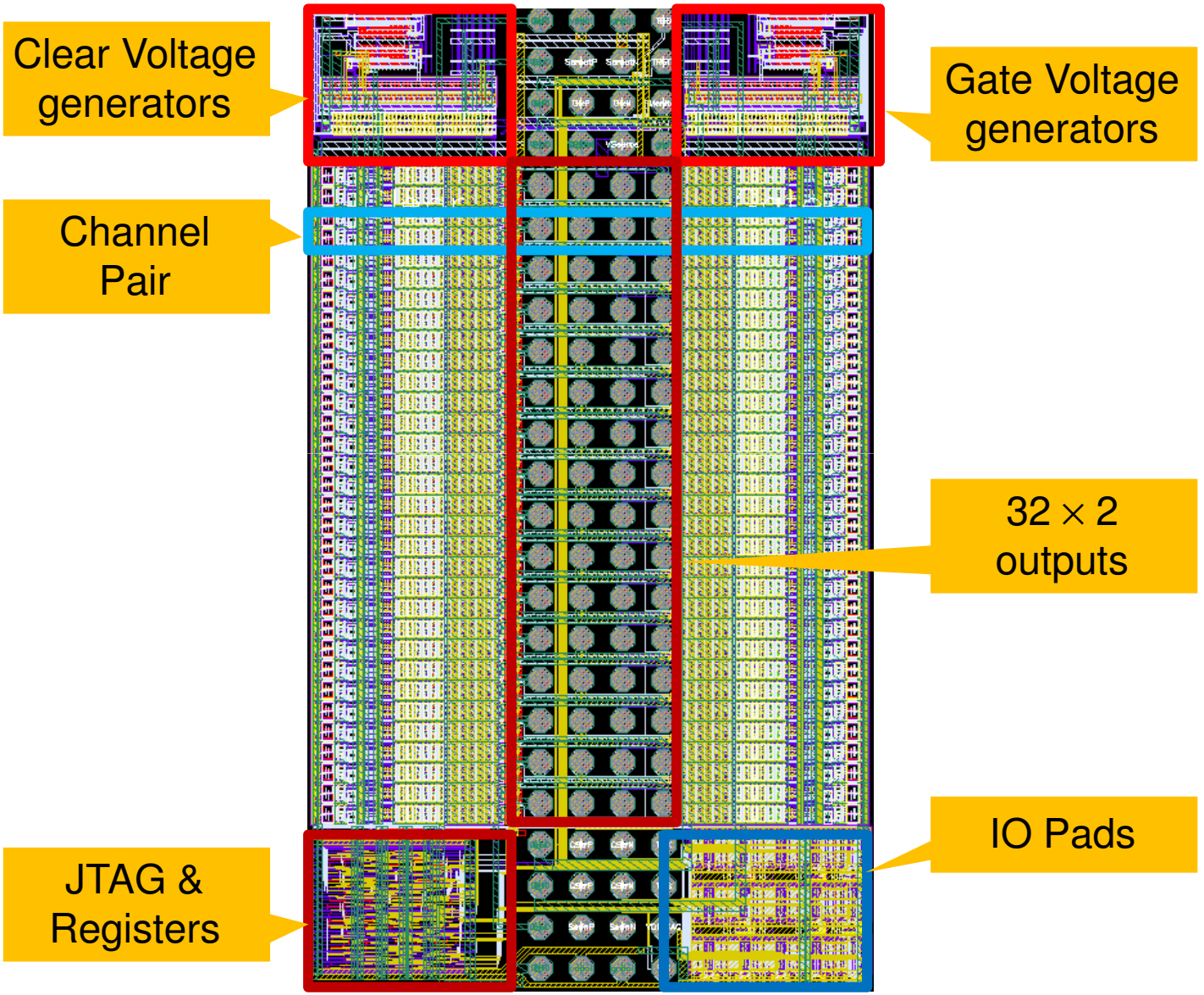
- Switcher-B has been submitted to AMS on 15.2.2010
- Chip is back since last week ! (Not tested yet)

- Main features:
  - 32 × 2 channels
  - 3600 × 2035 µm^2 (wider than planed, HV transistors!)
  - Fast HV switches up to 30V, Rad. hard-proven design
  - Internal generation of auxiliary voltages
  - JTAG Interface, IO Voltage of 1.2 – 3.3 V
  - Registers with triple redundancy
  - Bump bonding only, compatible to balcony layout (hopefully…):
    - 32 x 2 outputs
    - 32 pads for power / control
    - 150µm pitch, 80µm pad opening

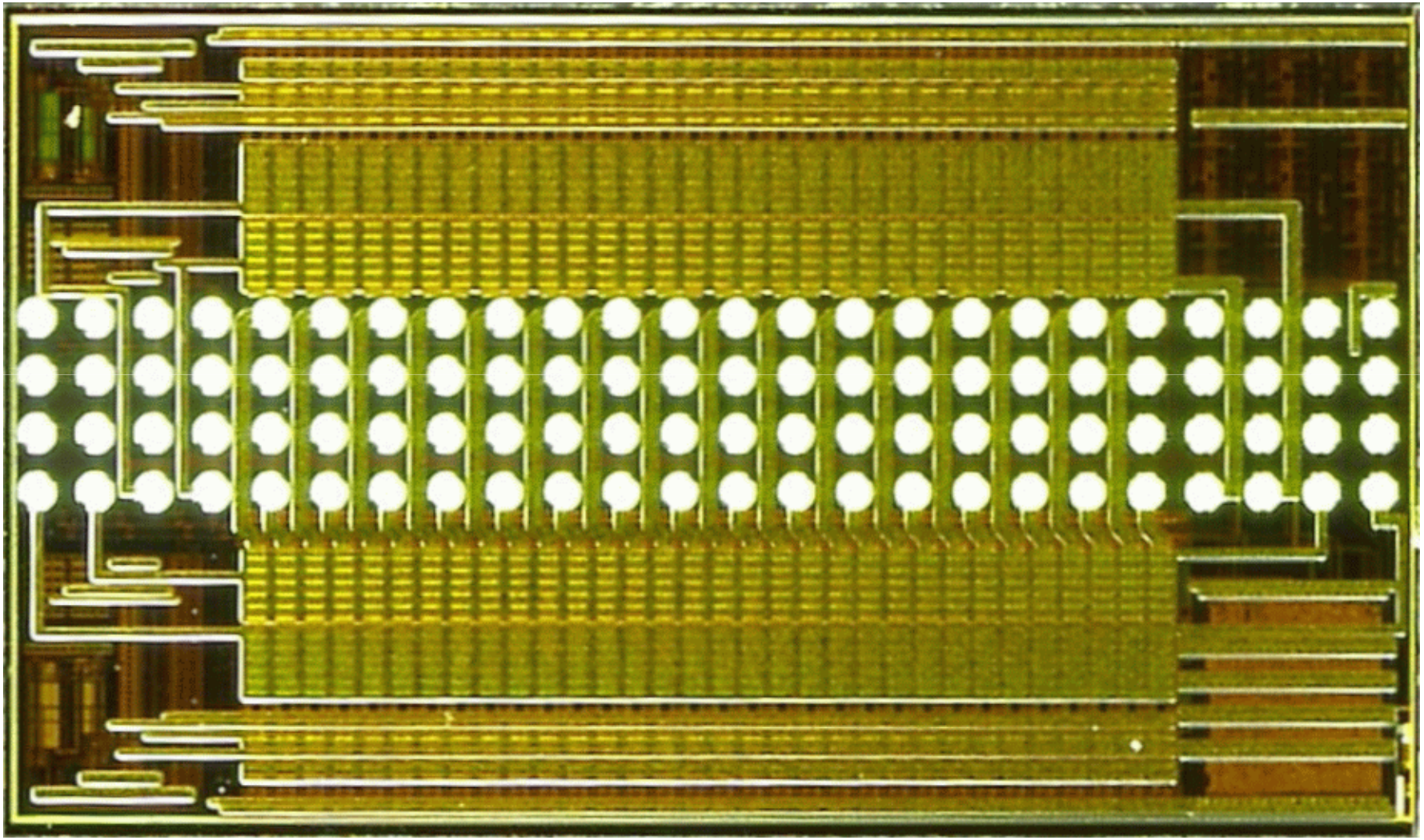
Simplified Block Diagram



Chip Layout

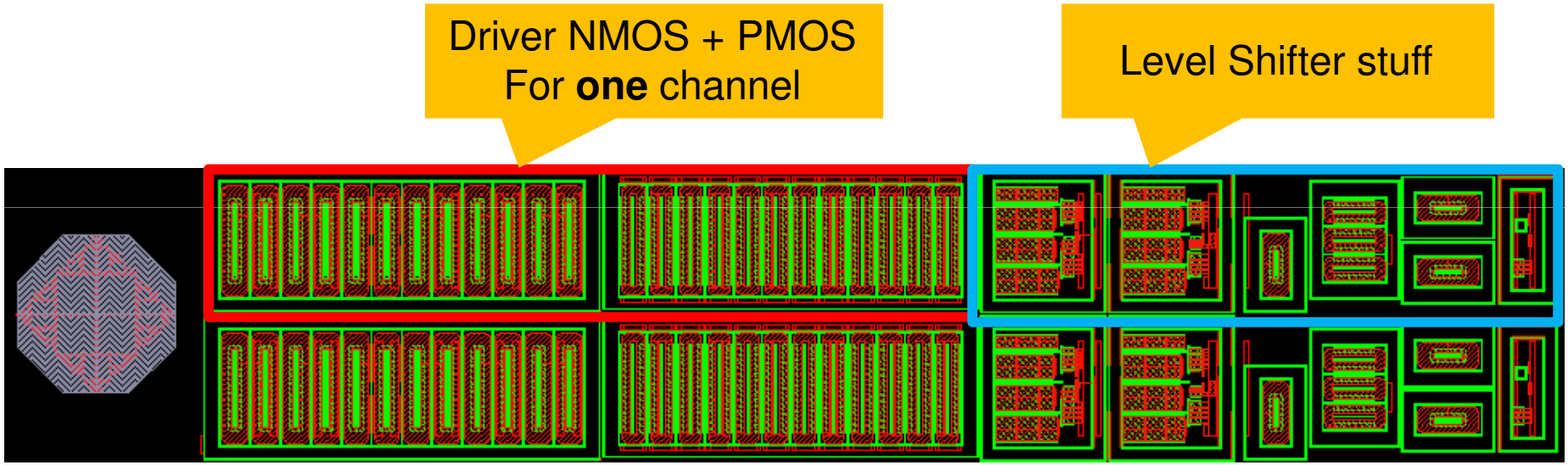

Clear Voltage generators
Gate Voltage generators
Channel Pair
32 × 2 outputs
IO Pads
JTAG & Registers

Chip Photograph



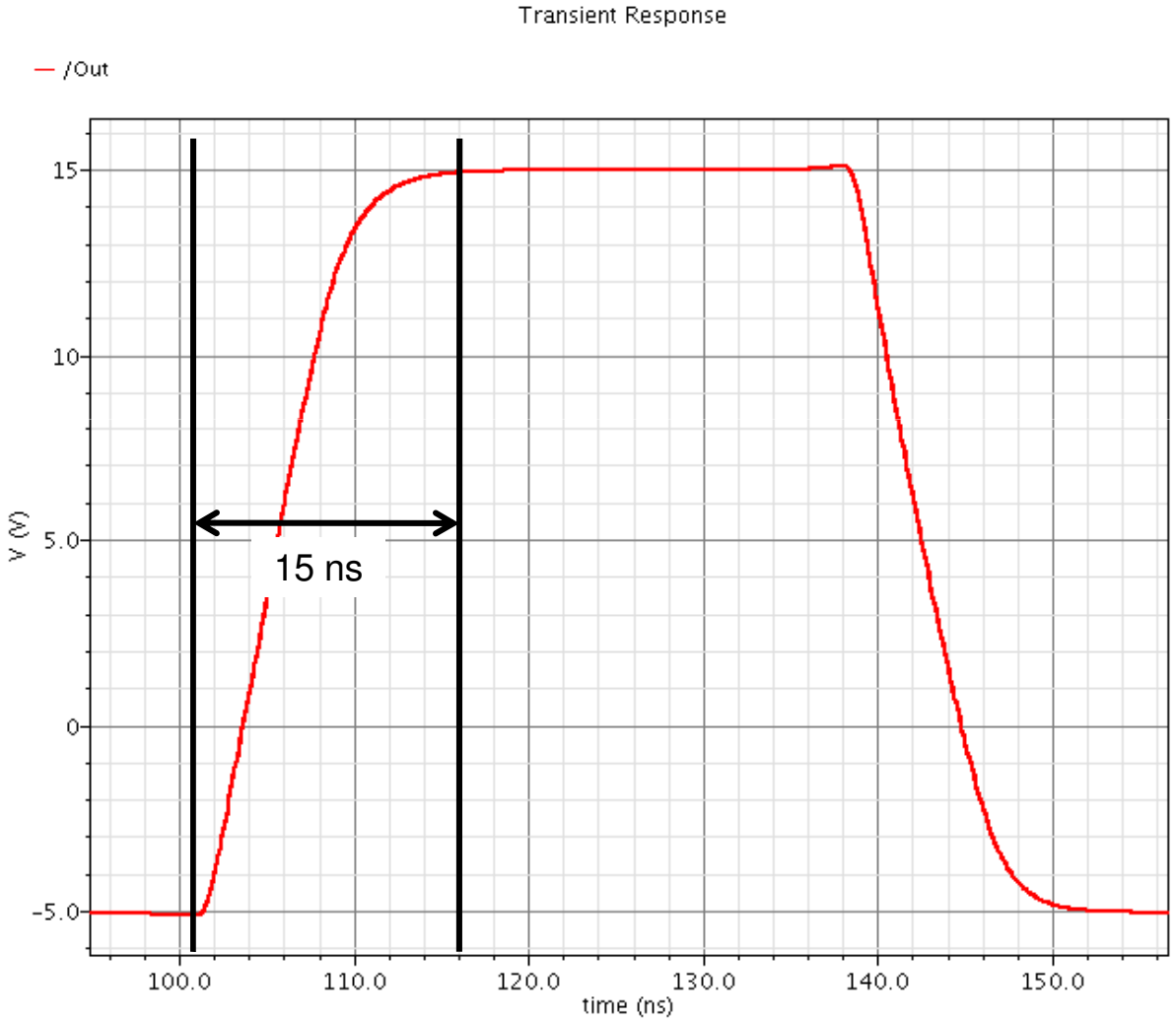
HV Channel

- Chip width is determined by required size of HV driver MOS
- Need to switch large capacitive loads of 50pF fast.



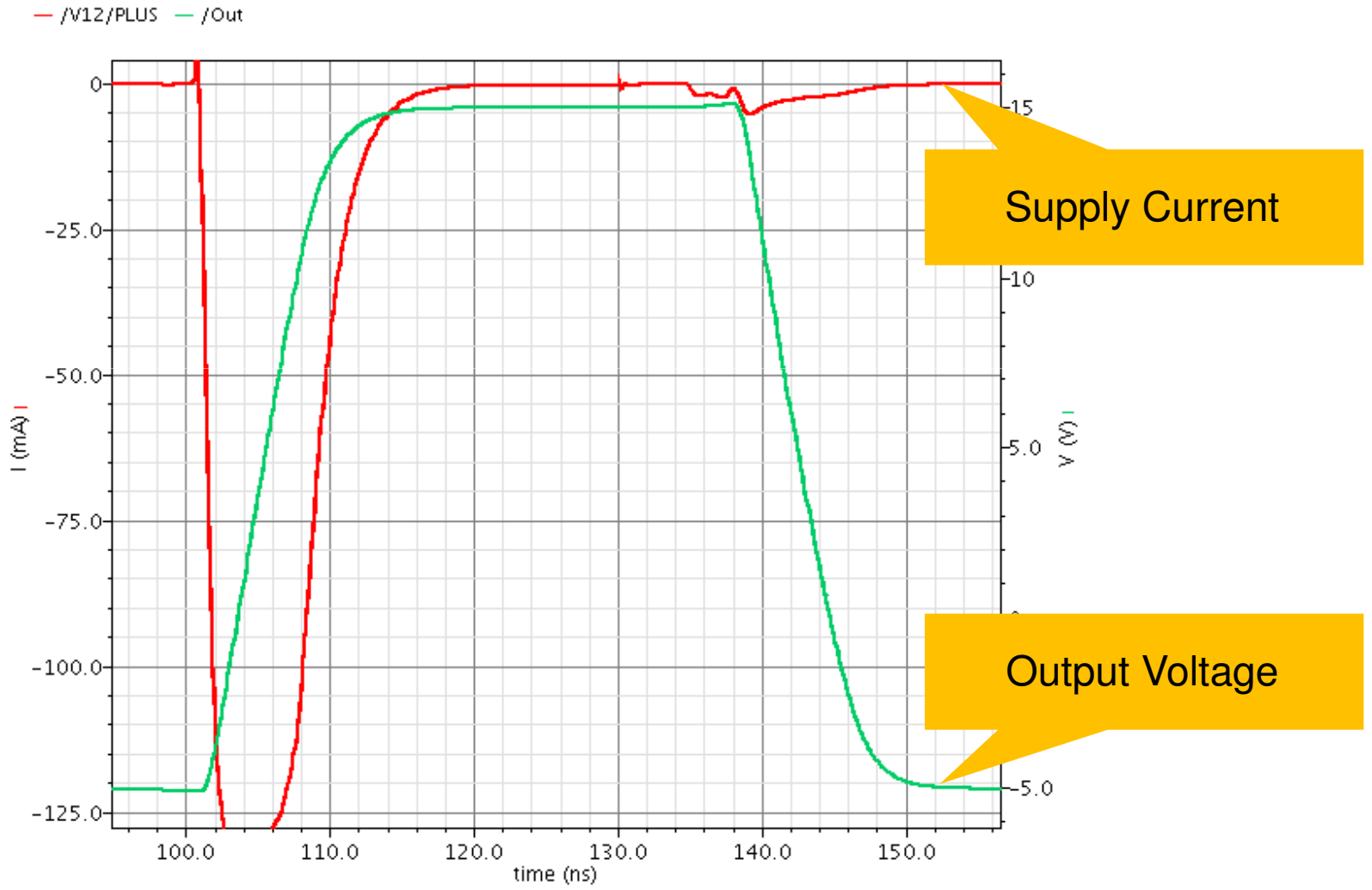
Simulated Speed

- Simulation of 20V clear pulse into 50 pF:

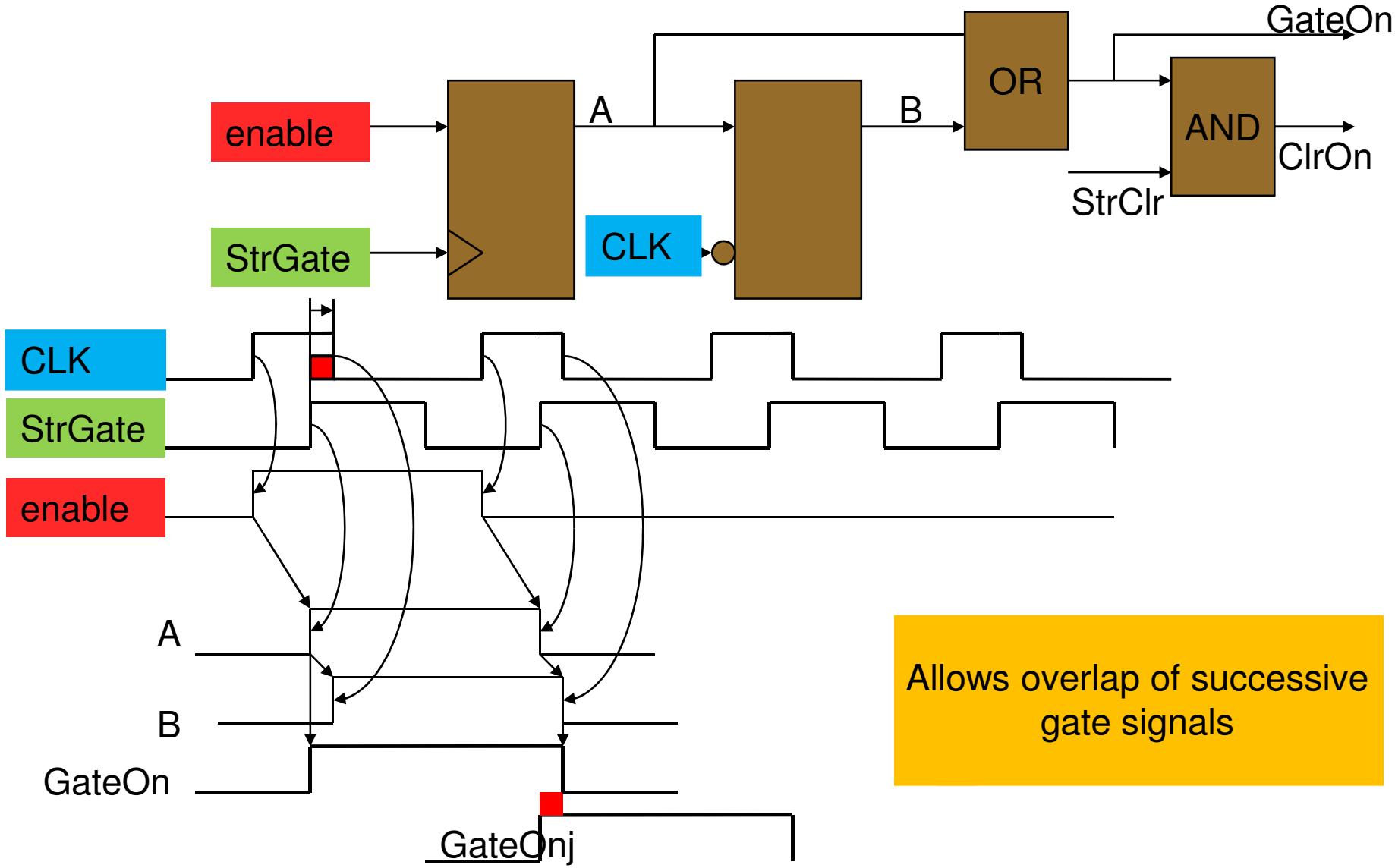


Supply Current Spike

- Q = C×U = I×T → I = C×U/T = 50p × 20V / 10n = 100 mA (!)



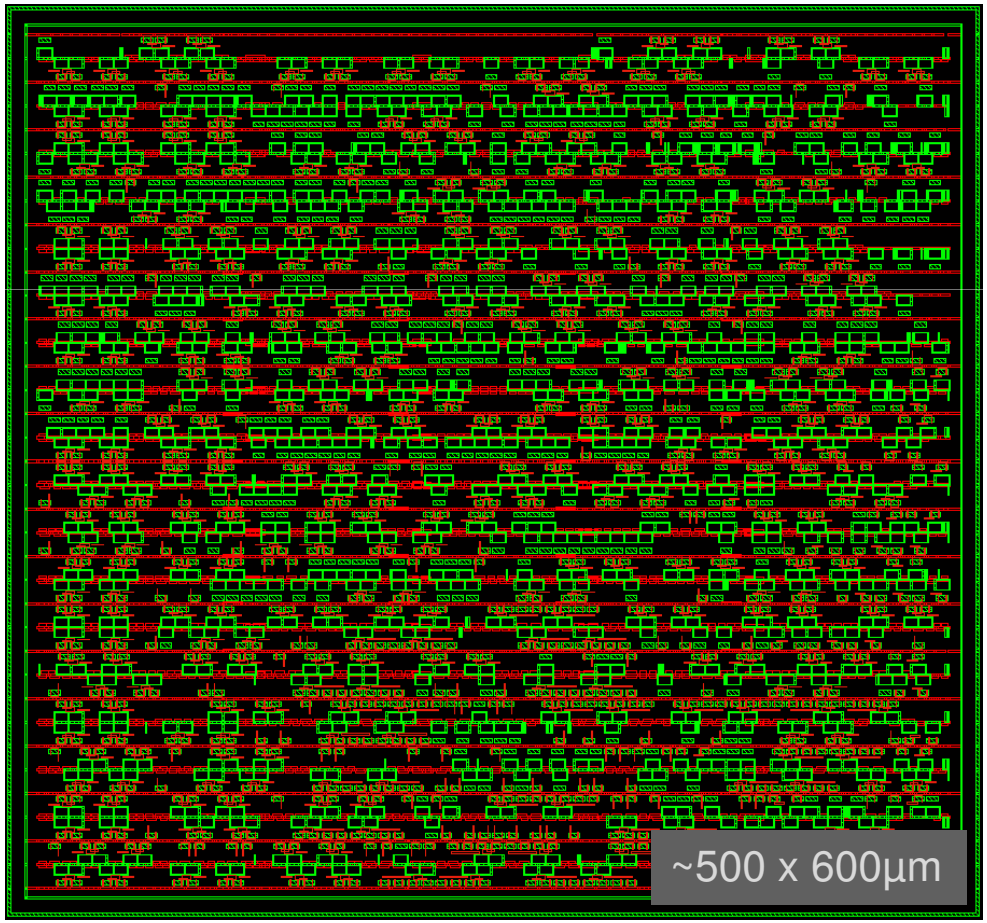
Timing Control Logic – as shown in Prague

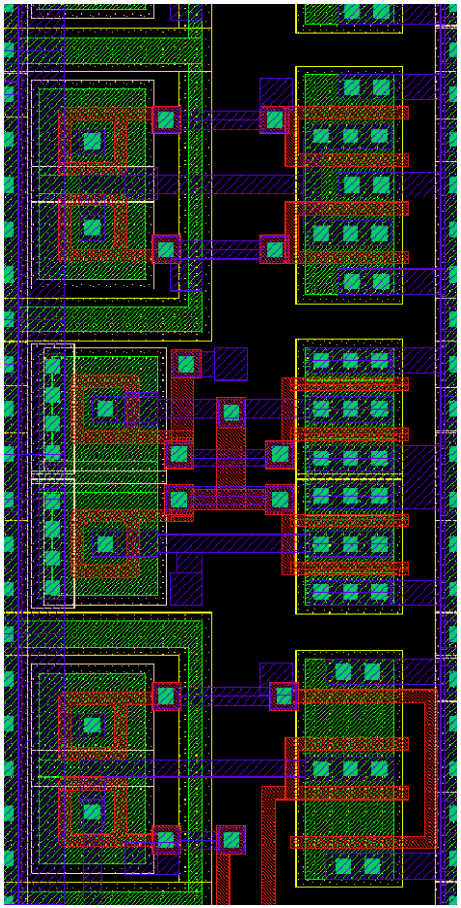


Allows overlap of successive gate signals

JTAG

- Self made rad hard lib (Peter) characterized by Cadence tools (Jochen & Michael Ritzert)
- Synthesized interface w. boundary scan, registers (Jochen)





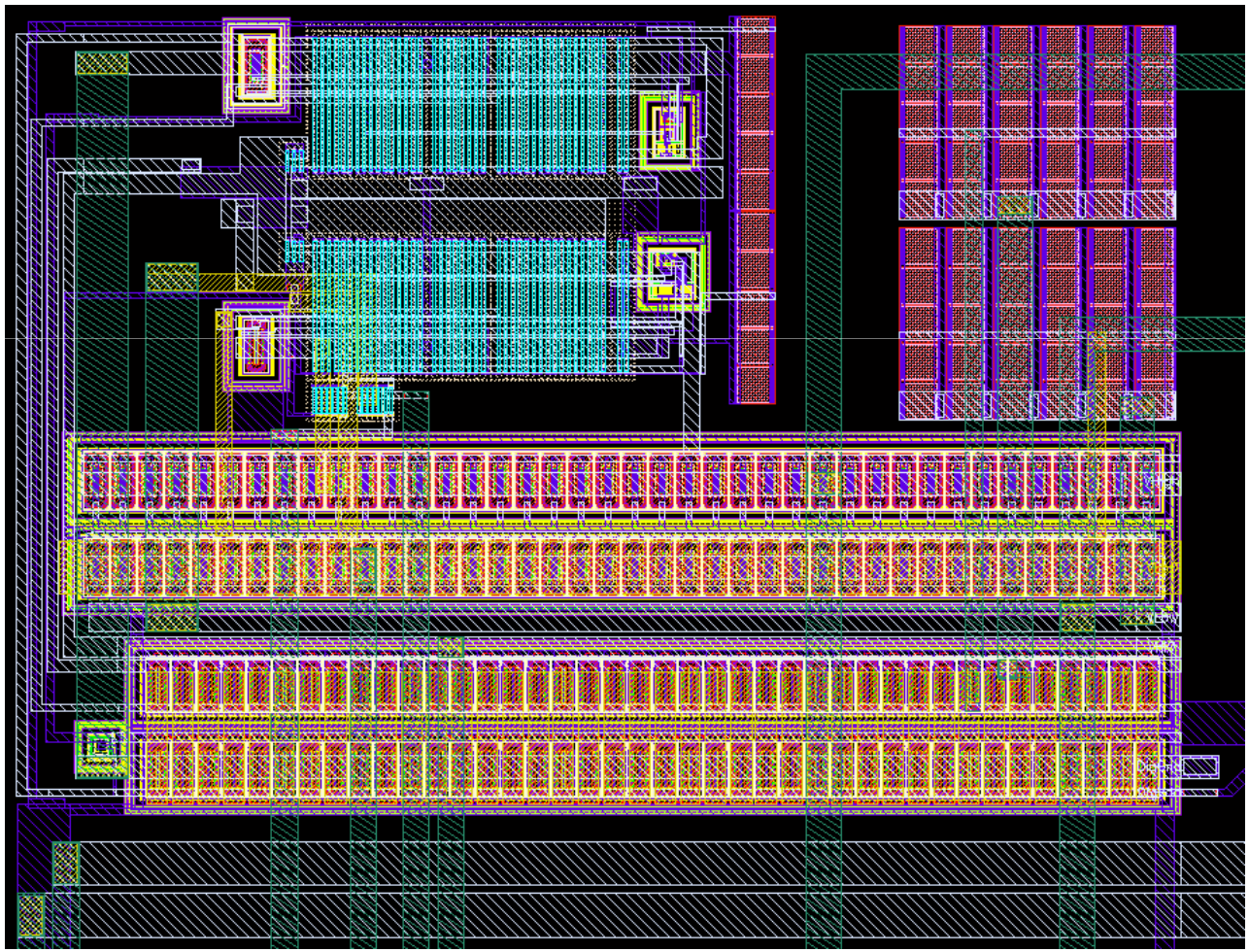
JTAG Functionality

- Full JTAG protocol, including RSTb
- Boundary Scan of all cells
- All pins have level shifters and pull down resistors
- Internal registers are triple mode redundant.
  16 available, only 4 used so far:
  - 2 x Bias of level shifter in idle mode
  - 2 x Bias of level shifter in boosted mode

- Later:
  - Termination resistors for differential inputs
  - Current in LVDS drivers / receivers

Regulators

- Generate voltages 3.3V above VLO and 3.3V below VHI
- VDDRef = 3.3V reference must be supplied! (wrt. gnd!)



Signals / Pins

Signal	Signals	Pads	Function
Substrat (gnd!)	1	1	Most negative voltage
Floating VDD and GND	2 x 2	4	Digital Supply
VDDRef (gnd! + 3.3V)	1	1	For aux. voltages
ClearHI / ClearLO / GateHI / GateLO	4 x 2	8	Switch HV Voltages
VSource	1	1	For decoupling (not impl.)
Shift register: Clk, Serin, Serout	3 x 2	6	LVDS
Gate_Strobe, Clear_Strobe	2 x 2	4	LVDS
JTAG: TCK, TMS, TDI, TDO,TRSTb	5	5	
VDDJTAG	1	1	JTAG supply voltage input
unused	1	1	Reserved for monitor
Sum		32	

NOT implemented

- Due to lack of time, some desired features could NOT be implemented:
  - No termination resistors
  - Serial output has no real LVDS pad (one pad = ½ VDD, other pad = CMOS)
  - No decoupling to Vsource (no significant layout space available, need to make regulators and IO cells compacter)
  - No monitor

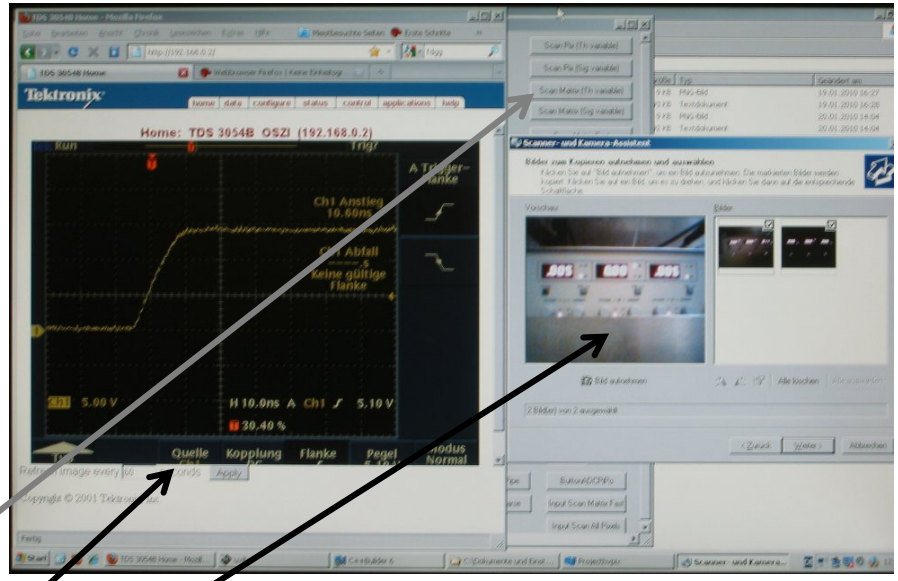
- Should be perfectly usable for our first tests!

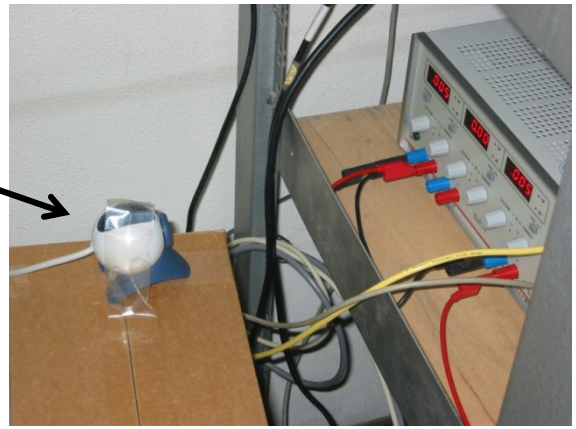
Reminder: Irradiation

- Switcher4 has same HV part as Switcher-B

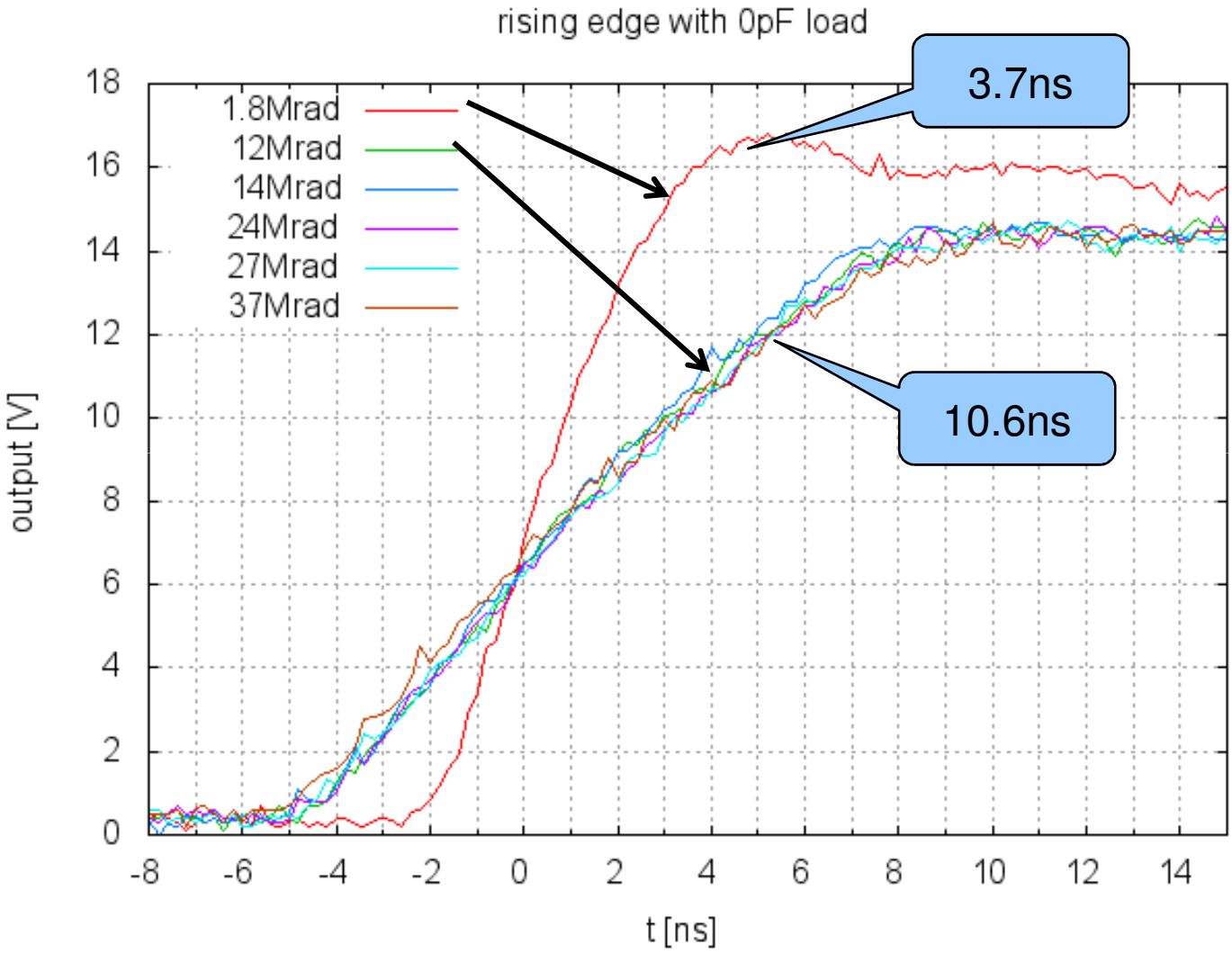
- Irradiation in Karlsruhe:
  - 60keV X-rays
  - 527 krad/h, 72h → 36Mrad
  - Chip was biased during irradiation

- Remote control of the setup:
  - PC with remote control software
  - Oscilloscope controlled via Ethernet
  - Webcam to monitor power supply :-)



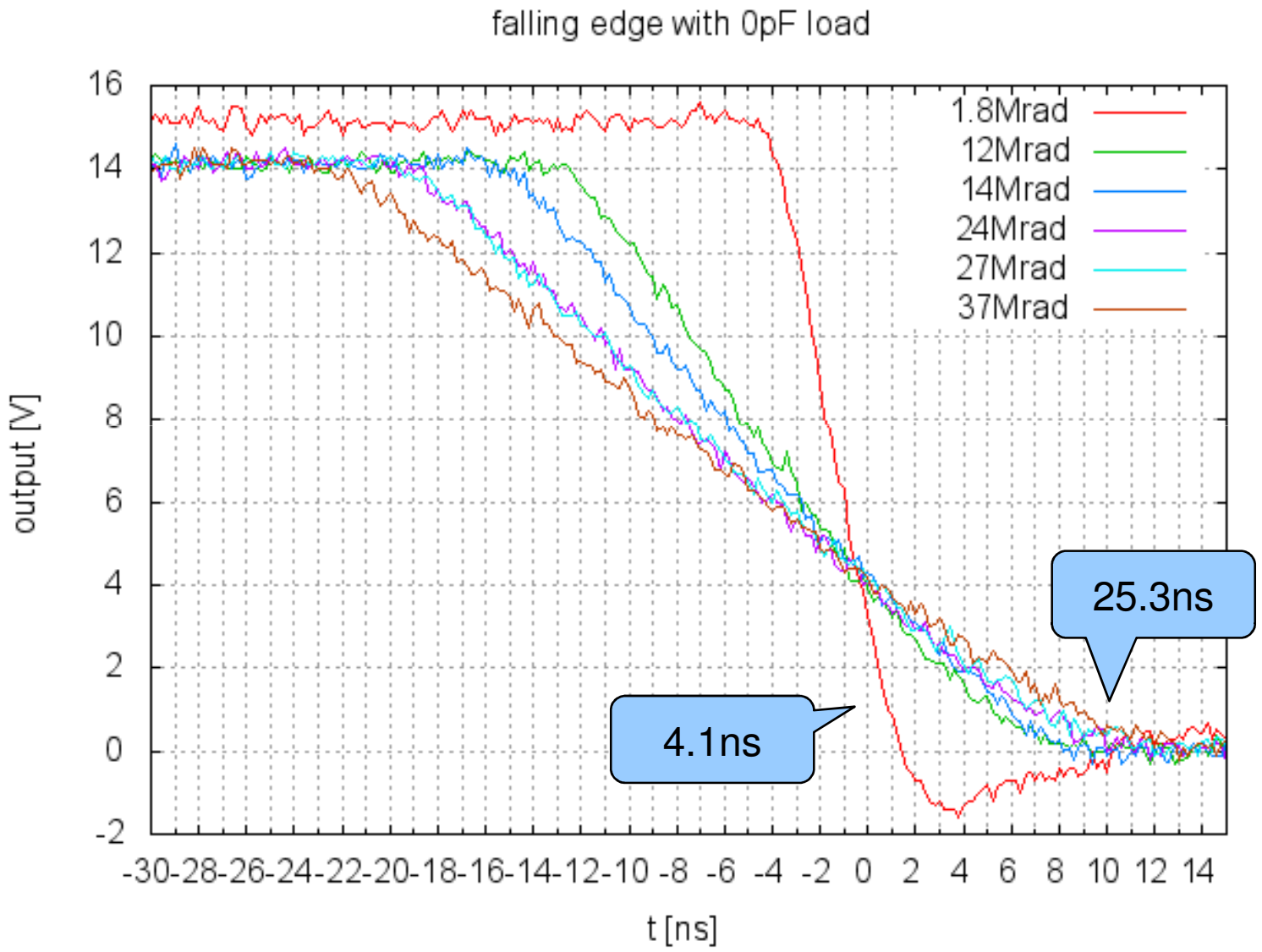


Result: Slight slow down of rising edge



- Will improve again after annealing (as seen in prev. chips)

Rising edge


falling edge with 0pF load
output [V]
t [ns]
1.8Mrad
12Mrad
14Mrad
24Mrad
27Mrad
37Mrad
25.3ns
4.1ns

Next steps

- Wait for bump bond adapters
- Prepare test setup
- Provide updated documentation
- Check rise / fall times after annealing

Thank you for your attention