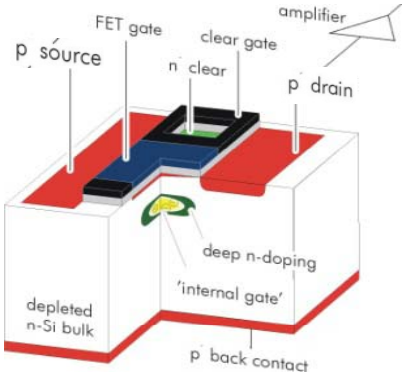
TDR: PXD @ Belle II
Questions & Answers

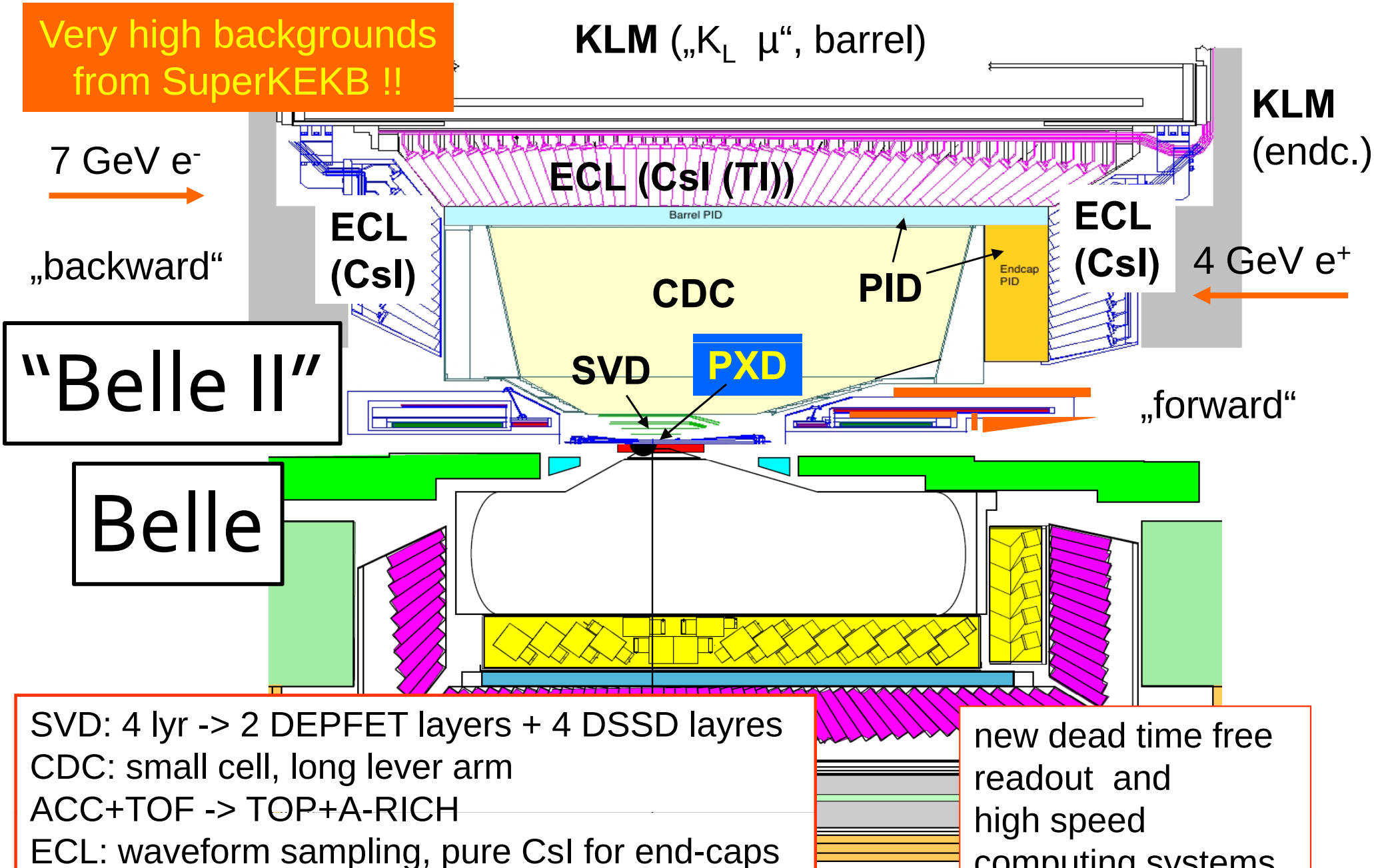
Christian Kiesling
MPI for Physics, Munich
for the DEPFET PXD Collaboration

- Overview
- Sensors
- Matrix Operation
- Pedestal Dispersion and Reponse Variation
- Bonding
- Half-Ladder Joints
- ASICs and Irradiation Tests
- Component Testing
- Data Rate and Readout
- Ladder Assembly and Testing
- Kapton Readout Cable
- Mechanical Design
- Schedule
- Specific Questions



Detector: Baseline Design

Very high backgrounds from SuperKEKB !!

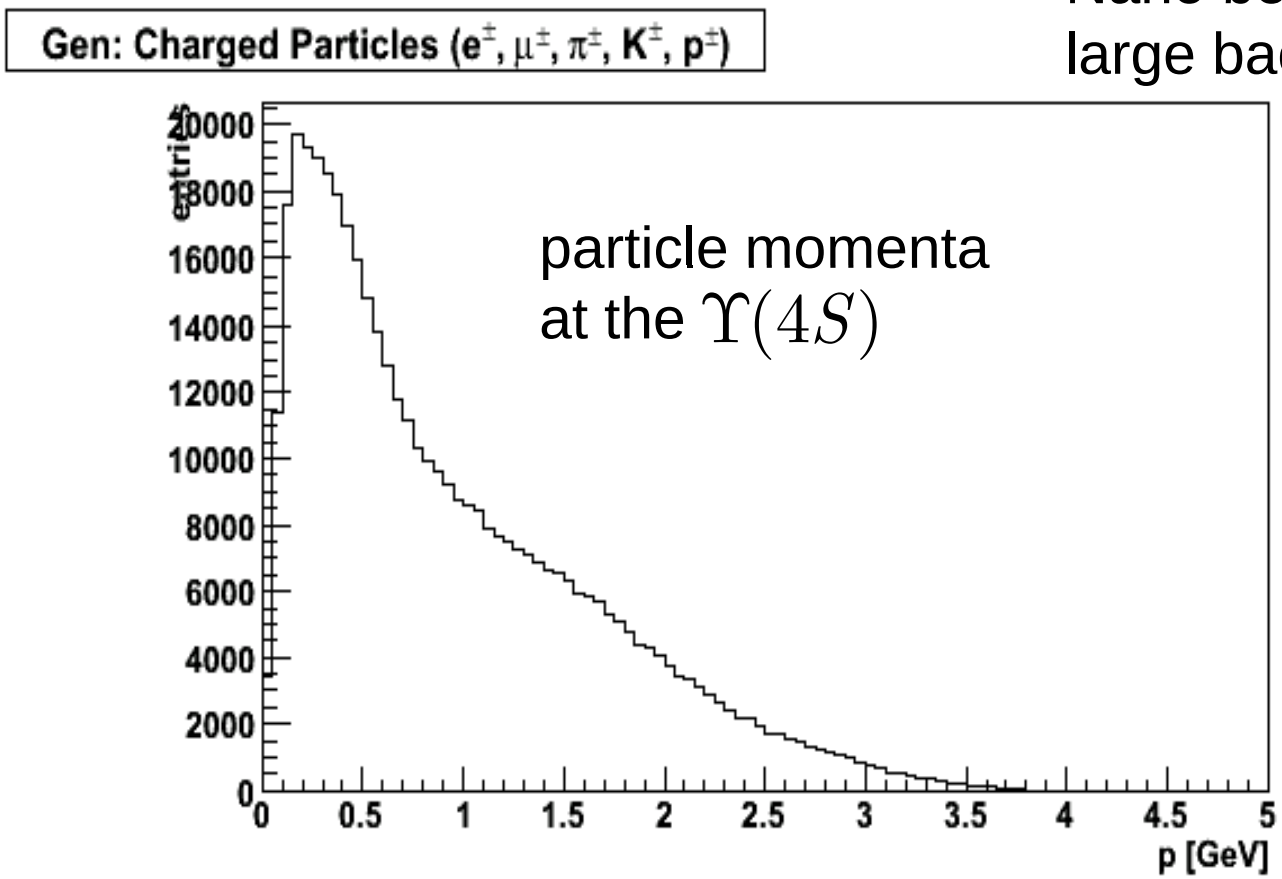


SVD: 4 lyr -> 2 DEPFET layers + 4 DSSD layres
CDC: small cell, long lever arm
ACC+TOF -> TOP+A-RICH
ECL: waveform sampling, pure CsI for end-caps
KLM: RPC -> Scintillator +SiPM (end-caps)

new dead time free readout and high speed computing systems

Pixel Vertex Detector for Belle-II

Nano beam option of SuperKEKB:
large backgrounds = high occupancy



→ must be thin,
rad. hard,
fast readout

→ ready for installation
in 2013

pixels at the innermost (<2.5 cm) radii 2 pixel layers (PXD)

Technology: „DEPFET“ (invented at MPI, fabricated at the HLL)

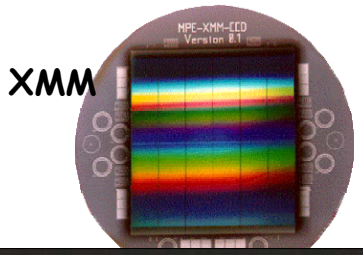
MPI Semiconductor Laboratory

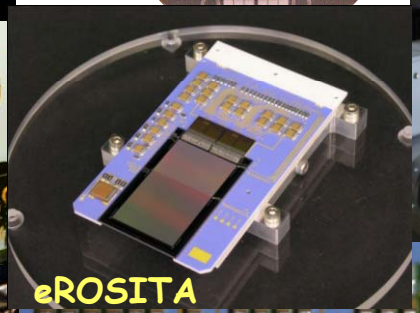
Common project of

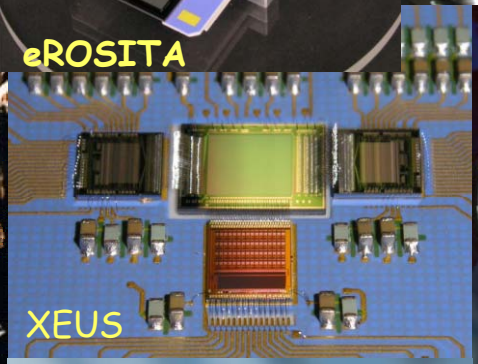
Max-Planck-Institut fuer Physik (Werner Heisenberg Institut), Munich
Max-Planck-Institut fuer extraterrestrische Physik, Garching

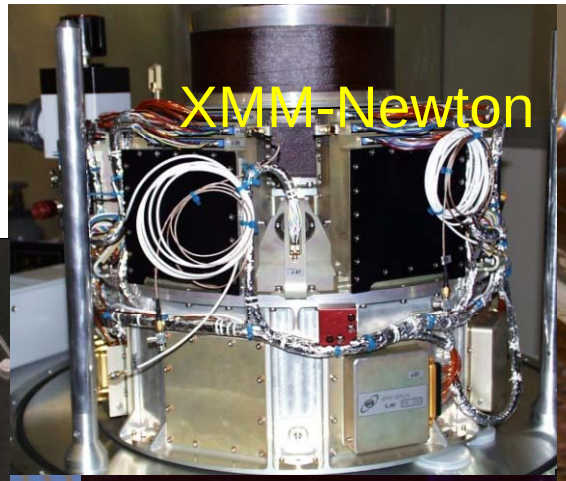
founded in 1992, since 2000 located in the Siemens plant in Neu-Perlach, Munich

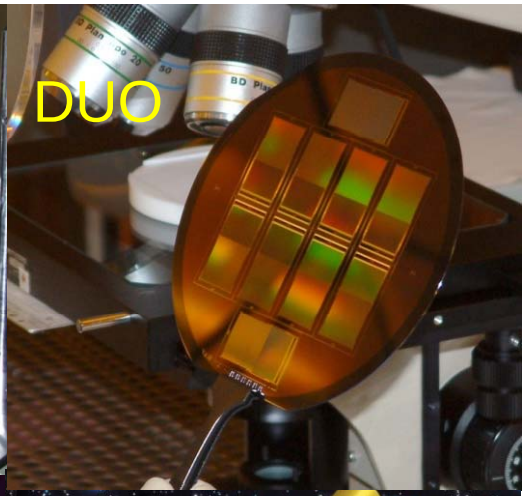
Scientific Activities at MPE

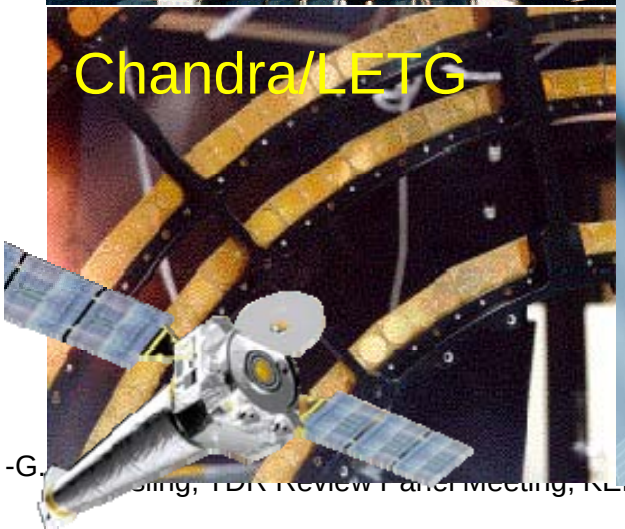


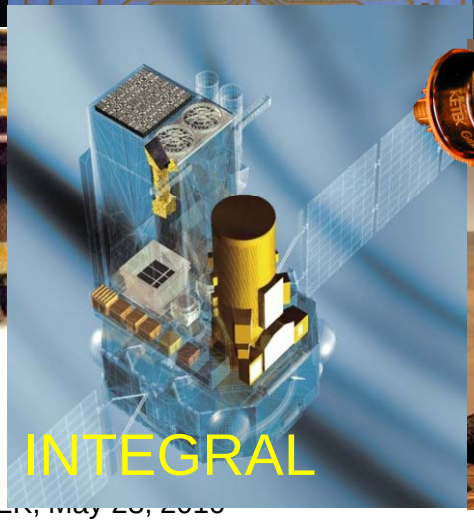




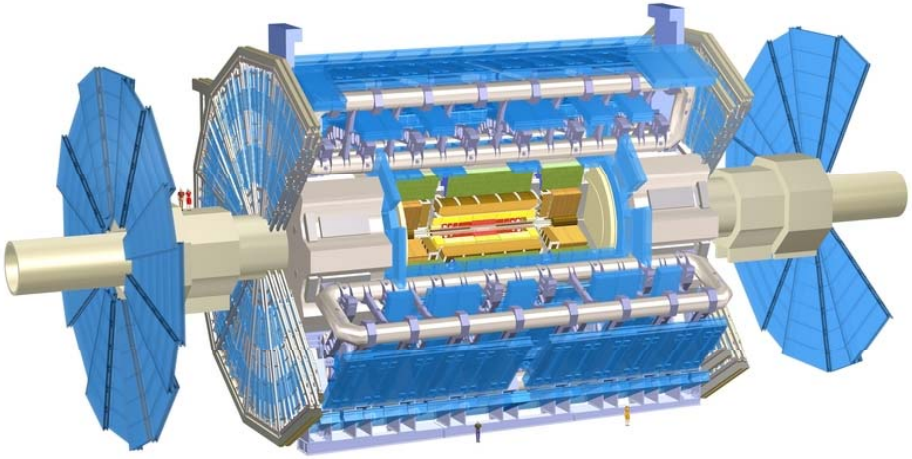




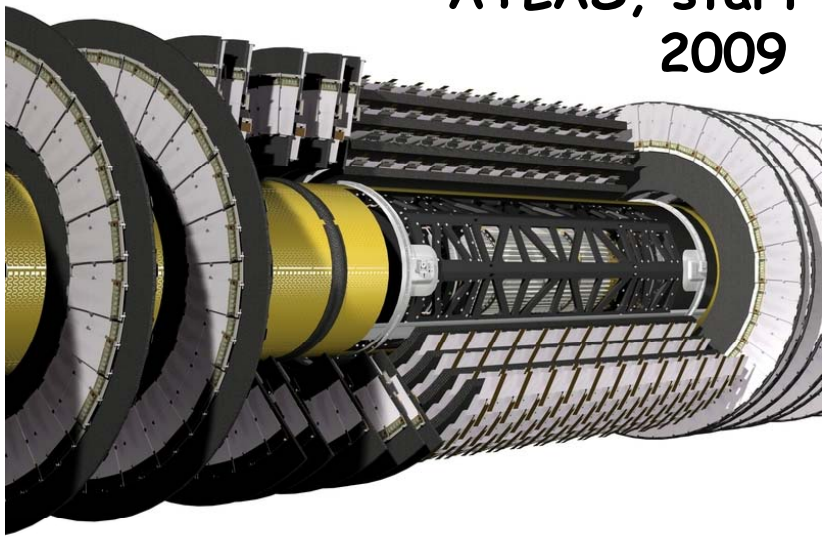


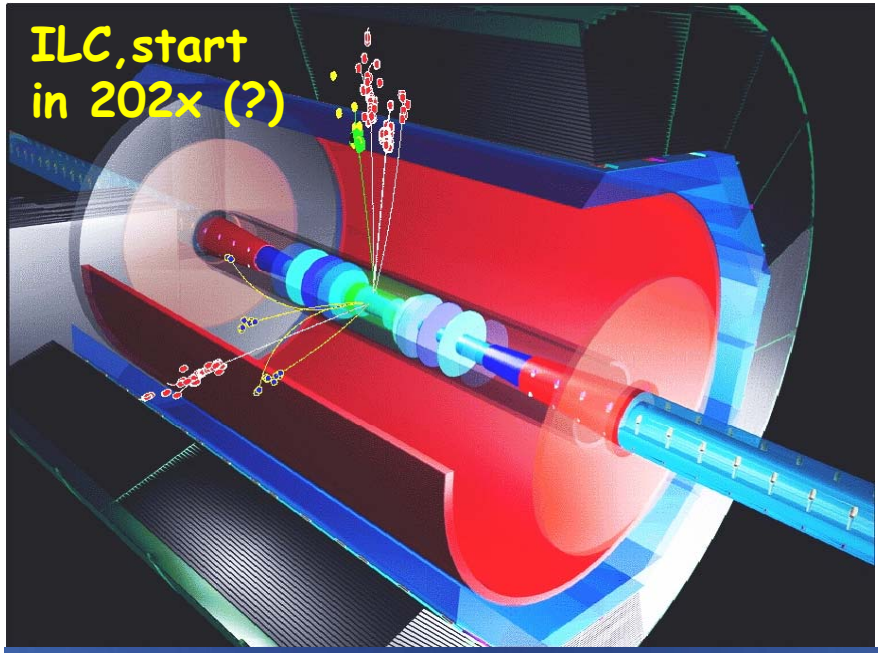


Scientific Activities at MPP



ATLAS, start in 2009





MAGIC, operational todate

HLL Fields of Competence

Complete Design and Manufacturing Chain

- Facilities for Layout and Simulation of Semiconductor Devices
- Production of Silicon Detectors
- Mounting and Tests

- Special Features:

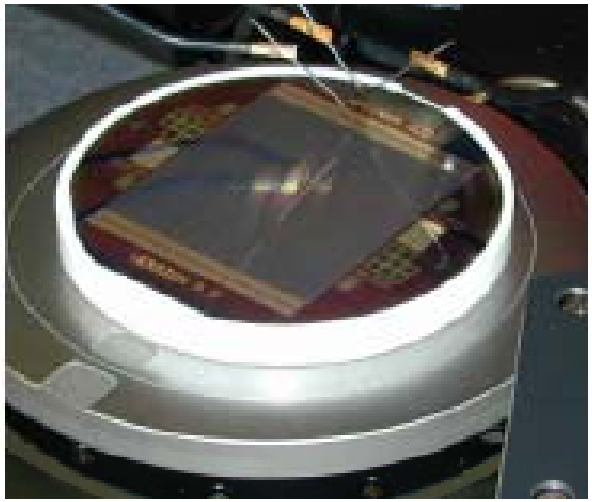
- Processing of ultra-pure silicon wafers (10^{12} impurites/cm^3)
- Double sided wafer processing
- Wafer scale detectors (up to 50 cm^2 area)

HLL Facilities

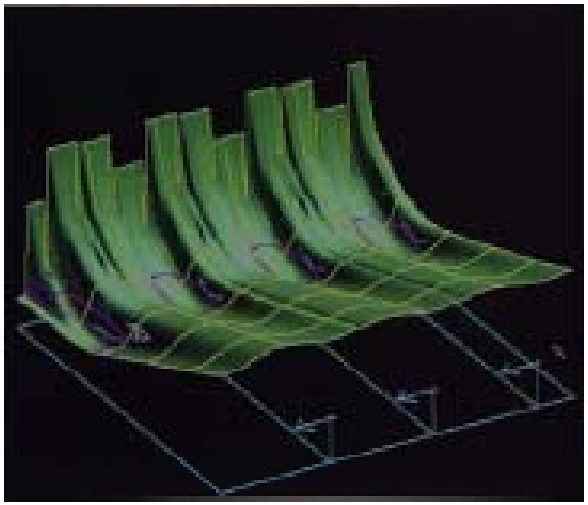
800 m² cleanroom up to class 1 ...

... with modern, custom made equipment ..... for a full 6" silicon process line

mounting & bonding



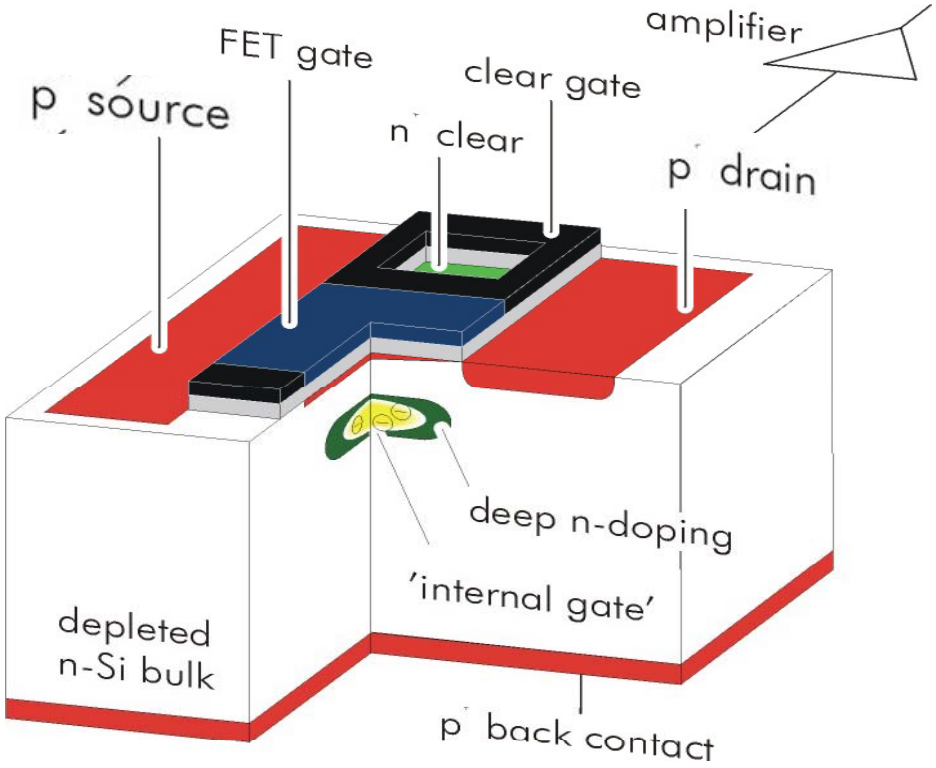
test & qualification

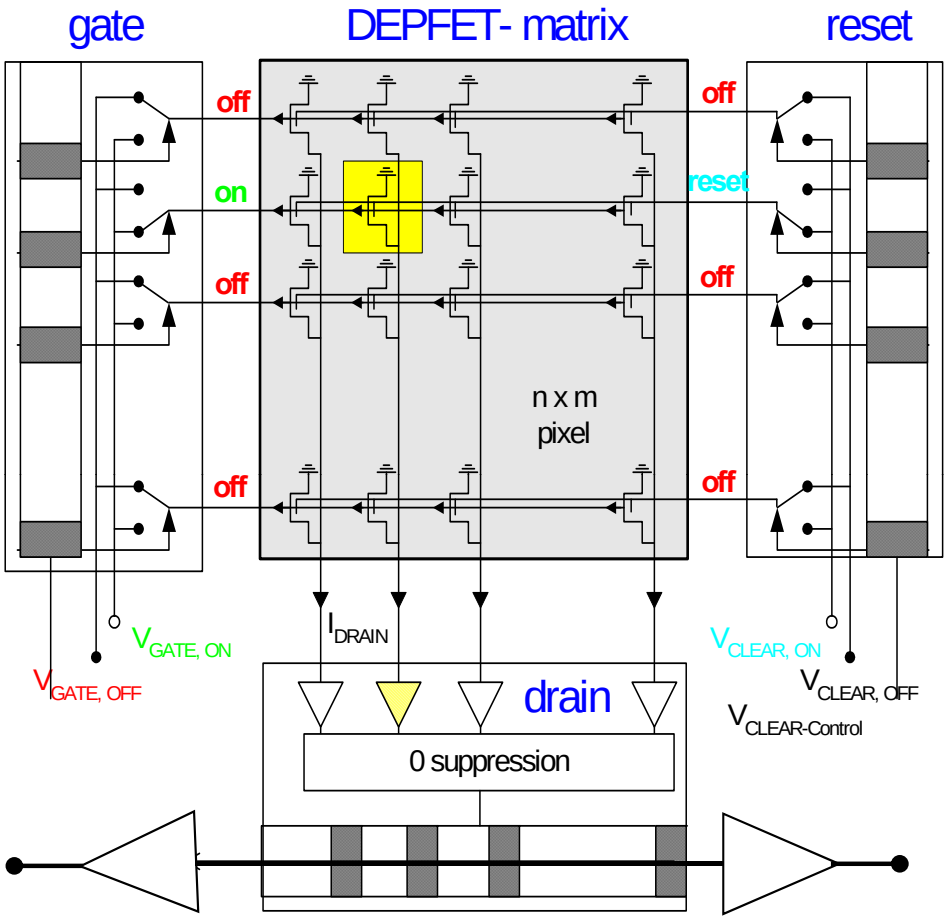


simulation, layout & data analysis

Overview of DEPFET Sensor

Depleted p-channel FET





- thin sensor, still large signal, fast signal collection
- low noise
- low power

ASICs on sensor:

- Switcher
- DCD (drain current digitizer)

PXD Layout, Control & DAQ

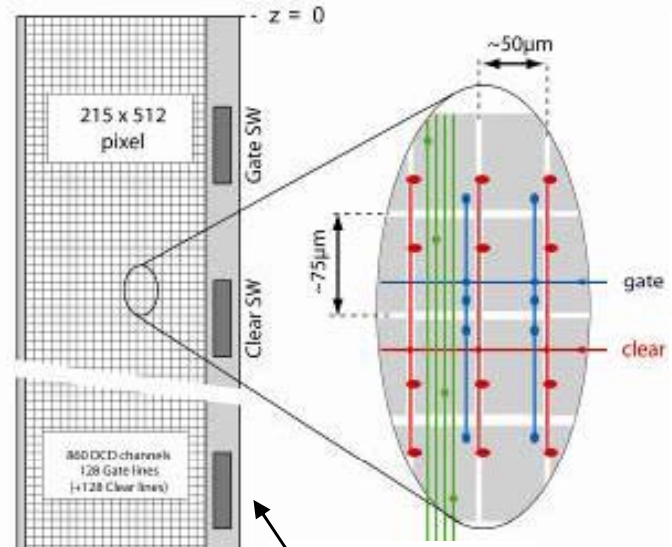
2 layers: @1.4(2.2) cm

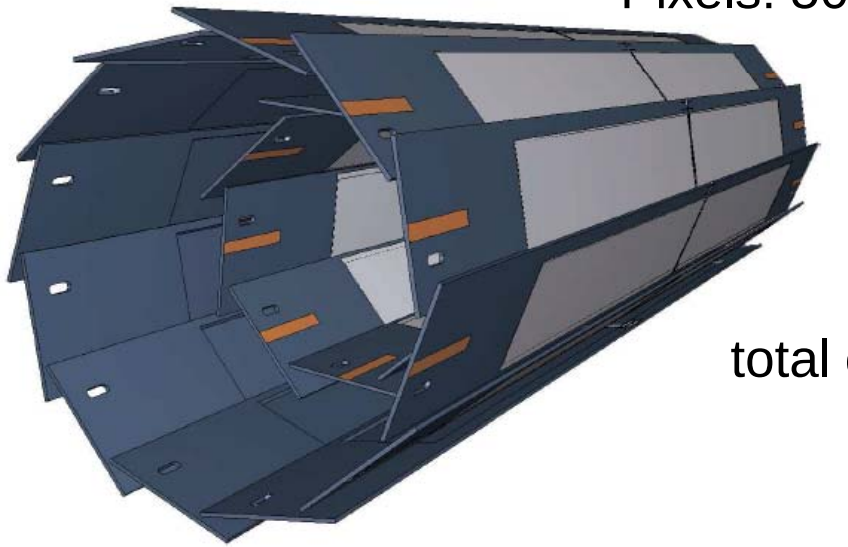
Pixels: 50 x 50(75) µm

half ladder: 800 rows

250 cols

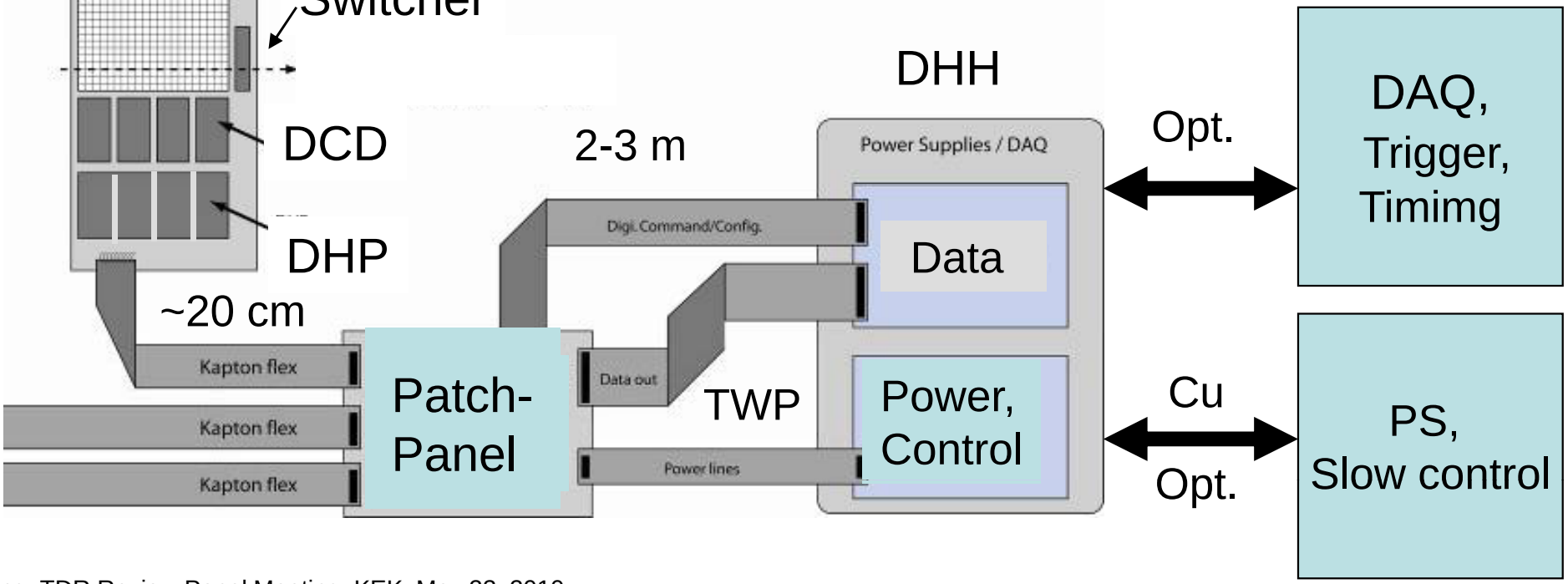
15 x 70 (85) mm





Thickness: 75 µm

total of 8 Mpx



DEPFET-Collab. @ Belle-II

Original Collaboration: DEPFET pixel detector @ ILC (since 2002)
now: Unite efforts to deliver a PXD by 2013 for Belle-II

University of Barcelona, Spain
CNM, Barcelona, Spain
Universitat Ramon Llull, Barcelona, Spain
Bonn University, Germany
Heidelberg University, Germany
Giessen University, Germany
Goettingen University, Germany
Karlsruhe University, Germany
IFJ PAN, Krakow, Poland
LMU Munich, Germany
MPI Munich, Germany
Techn. Univ. of Munich, Germany
Charles University, Prague, Czech Republic
University of Santiago de Compostela, Spain
IFIC, Valencia, Spain

with important help from KEK, Vienna, Hawaii

DEPFET@Belle-II

Management:

- IB- Board
- Project Leader
  C. Kiesling
- Technical Coord.
  H.-G. Moser
- Integration Coordinator
  Shuji Tanaka (KEK)

The DEPFET (PXD) Collaboration

List of Institutions contributing to DEPFET @ Belle-II

			Contact	email
Germany				
	MPI	Max-Planck-Institute for Physics, Munich	Christian Kiesling	cmk@mpp.mpg.de
			Hans-Günther Moser	hgm@hll.mpg.de
	BON	University of Bonn	Hans Krüger	krueger@physik.uni-bonn.de
			Norbert Wermes	wermes@physik.uni-bonn.de
	GIE	University of Gießen	Sören Lange	Soeren.Lange@exp2.physik.uni-giessen.de
	GOE	University of Göttingen	Ariane Frey	ariane@mail.cern.ch
	HEI	University of Heidelberg	Ivan Peric	peric@rumms.uni-mannheim.de
			Peter Fischer	peter.fischer@ziti.uni-heidelberg.de
	KAR	University of Karlsruhe	Michael Feindt	Michael.Feindt@physik.uni-karlsruhe.de
			Thomas Müller	mullerth@ekp.uni-karlsruhe.de
	LMU	Ludwig-Maximilians-University of Munich	Jochen Schieck	jochen.schieck@lmu.de
	TUM	Technical University of Munichj	Stephan Paul	stephan.paul@ph.tum.de
Czech Rep.				
	PRA	Charles-University Prague	Peter Kodys	kodys@ipnp.troja.mff.cuni.cz
Poland				
	KRA	Institute of Nuclear Physics, Krakow	Henryk Palka	Henryk.Palka@ifj.edu.pl
Spain				
	IFV	Instituto de Fisica Corpuscular (IFIC), Valencia	Carlos Lacasta	Carlos.Lacasta@ific.uv.es
	URL	University Ramon Llull, Barcelona	Jordi Riera Babures	jriera@salle.url.edu
	UBA	University of Barcelona	Angel Dieguez	dieguez@el.ub.es
	CNM	Centro Nacional de Microelectronica, Barcelona	Enric Cabruja	enric.cabruja@cnm.es
	USC	University of Santiago de Compostela	Pablo Vazquez Regueiro	fpvazquez@usc.es
	IFC	Instituto de Fiisica de Cantabria (IFCA), Santander	Ivan Vila Alvarez	vila@ifca.unican.es
Japan	KEK	KEK	Shuji Tanaka	shuji.tanaka@kek.jp
Austria				
	VIE	Institute for High Energy Physics (HEPHY), Vienna	Markus Friedl	friedl@hephy.oeaw.ac.at
USA	HAW	University of Hawaii	Gary Varner	varner@phys.hawaii.edu

Questions by the Review Panel

PXD6 sensors, together with PXD-TO (thin oxide) structures are currently being produced. To the best of our understanding, the following are still open options for the final design of the sensors and are only now being studied with test structures rather than full sensors:

- channel length and smoother and smaller transistor gates

- gate oxide thickness
- gate with nitride layer to improve radiation hardness

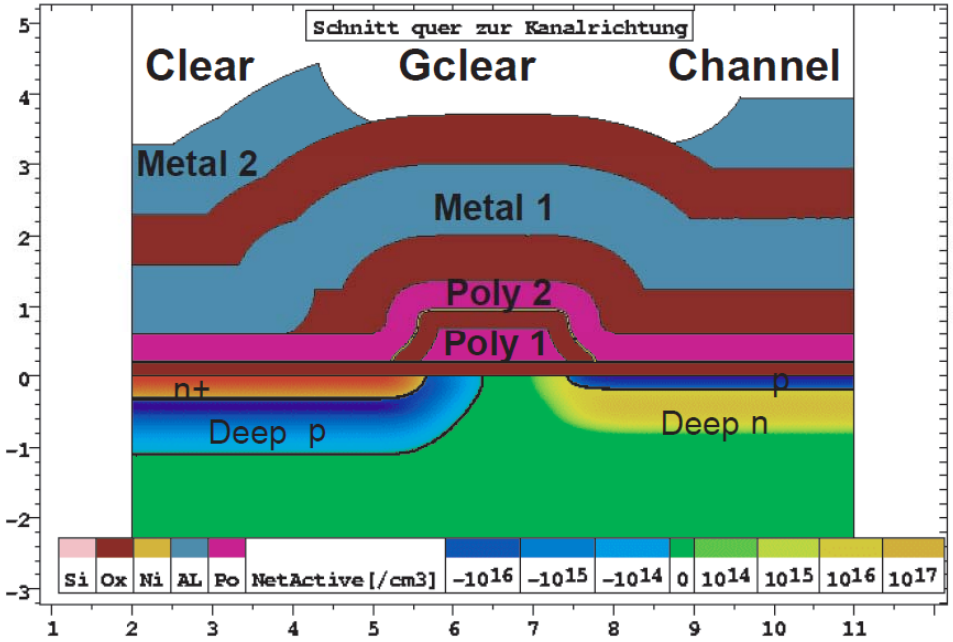
- third metal layer

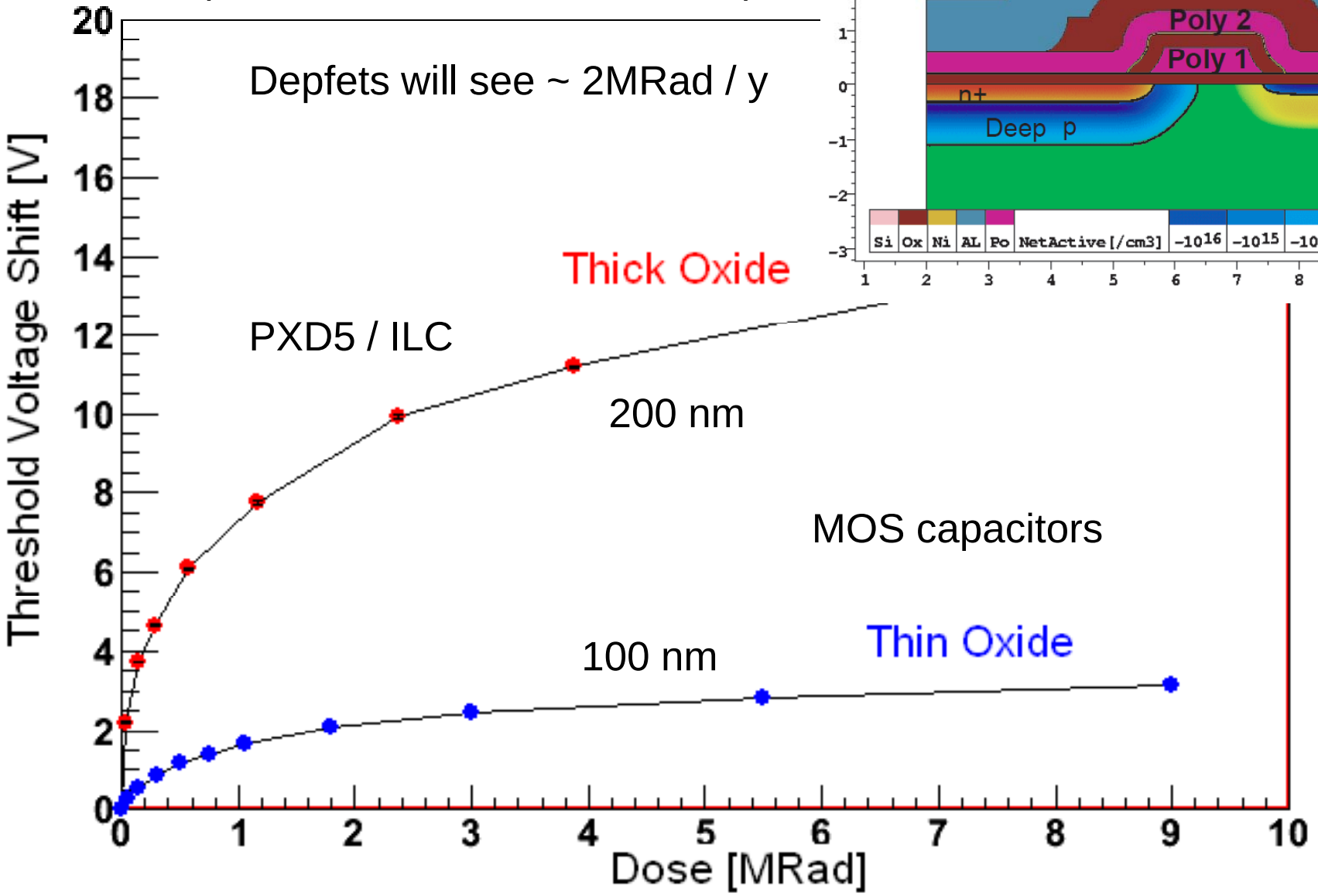
(Options concern radiation hardness and on-sensor bonding)

Radiation Hardness

(irradiations done in Karlsruhe)

Depfets will see ~ 2MRad / y





important new technological step

Sensor Design Options

Answers

We have a very tight schedule for sensor development and production which makes some compromises necessary. There is no time for a second prototype run with the final radiation hard technology and the final sensor design.

Channel length:

A moderate reduction of channel length is necessary to ensure a high internal amplification gQ (S/N).

We have to compensate the reduction of gQ caused by the thinner gate dielectrics by a moderate reduction of the channel length according to the DEPFET scaling rules:

Answers: Sensors (cont.)

DEPFET scaling rule:

$$g_q = \frac{dI}{dQ} = c\sqrt{\frac{d_{ox}}{L_G^3}}$$

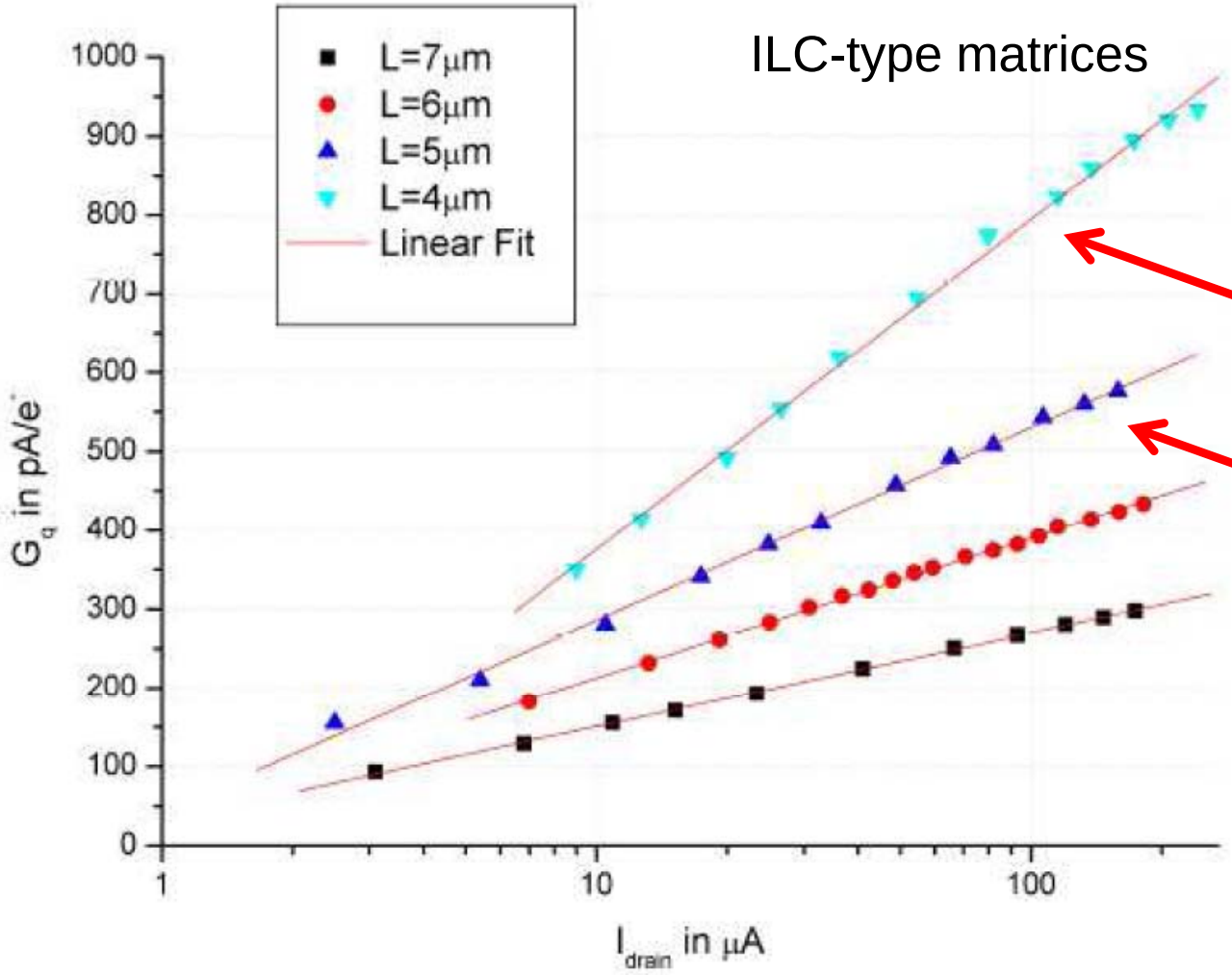
decrease oxide thickness
(make depfet rad hard)

need also to decrease gatelength
(to retain same gQ)

Decrease of oxide thickness by a factor of 2 requires a gate length reduction by 1.2 µm (from 6 µm to 4.8 µm).

Already experiences with gate lengths in this range and below on the basis of single structures and matrices
(ILC-type 20x20 µm² matrix)

Answers: Sensors (cont.)



ILC-type matrices

Variation of g_q as function of the gatelength

4 µm

5 µm

we need 4.8 µm

Answers: Sensors (cont.)

For reasons of yield (pedestal spread) only 'equipped' a smaller fraction of the PXD6-DEPFETs with smaller gates.

(In parallel) significantly improved the homogeneity of our polysilicon etch techniques (both plasma as well as wet etching) compared to the PXD5 technology: will result in less gain and pedestal variations of the ongoing PXD6 devices production

We are confident that we can reduce the gate length moderately in a controlled way.

Furthermore, with this choice of reduced gate length the large matrices of the PXD6 prototypes ("thick oxide" and "long channel") will have the same gain as the final ones ("thin oxide" and "short channel"), which is important for representative tests of S/N, timing etc.

Answers: Sensors (cont.)

Gate dielectrics (thin oxides):

The reviewer comment is true. We don't have enough time to test the thinner gate dielectrics on full size matrices before the start of the production run.

However, we don't expect a reduction of yield since also the new thin oxide is still very thick (100 nm) compared to the gate oxides used in standard microelectronics. Thus it can stand easily the voltages necessary to operate the DEPFET.

Concerning device physics: many of the new implantation parameters will be tested already within the PXD-TO project (parallel production with thin oxides), where p-channel MOS transistors with 'DEPFET relevant' doping profiles will be produced, providing the relevant IV curves and field distributions.

Answers: Sensors (cont.)

In order to keep this production short and simple no backside processing and no double poly/metal layers are processed.

The entire DEPFET device and technology development was only possible by the use of technology and device simulation tools where we achieved a high prediction capability. If necessary the simulations can be tuned on the PXD-TO results.

In this way we minimize the inherent risks caused by the thin oxides.

Answers: Sensors (cont.)

Third metal layer:

The results of the 'Copper Technology' development are very promising. We will reserve a few PXD6 wafers in order to test the third metal layer on the full size DEPFET matrices which will be deposited and tested by the end of the year.

The Cu-layer is a new development where we electroplate copper as a back-end process on the front side of the DEPFET wafers. This process module is being qualified with external partners (CNM Barcelona) and we do not see any issues in integrating it into the DEPFET process flow.

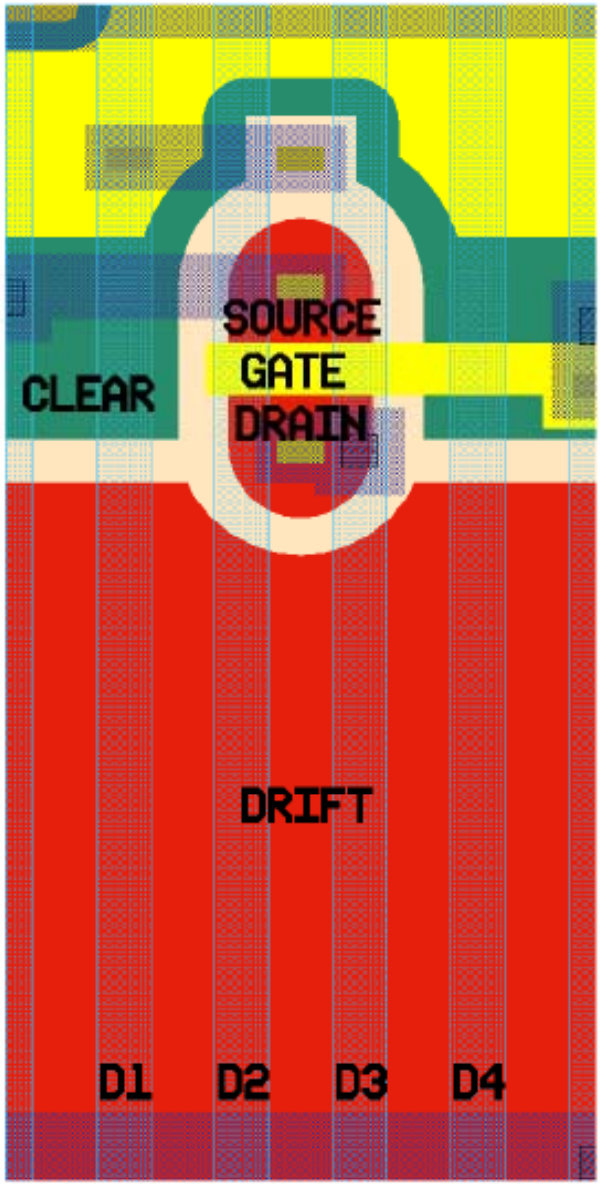
Test diodes show excellent behaviour and the line / width ratio of the deposited Cu lines meets the expectations to better than 5µm / 5µm. This process will be installed at the HLL in the course of 2010.

Answers: Sensors (cont.)

Questions:

Furthermore, the design of individual source and drain regions embedded in drift and clear regions are only now being studied.

Q1: A fallback solution is the ILC design with shared contact region. This is a rather imposing parameter space still to be explored. As the text states, minor design changes can dramatically influence yield and radiation hardness.



Answers: Sensors (cont.)

Answer:

We have much confidence in our simulations. At PXD6 we try three different design options + fall back 'ILC option' which are behaving nicely in the 'simulation world'. In addition, there exists already a lot of practical experience with 'individual source - drain' designs for astrophysical applications.

Of course, those have a much larger – circular – DEPFET geometry which is too slow for Belle II.

Nevertheless, the Belle II designs may be considered as a new combination of already proven design features.

Answers: Sensors (cont.)

Q2: Could the currently produced PXD6 be used in the Belle II detector?

Answer:

The matrices on PXD6 cannot be used for Belle II. They still have thick (non rad hard) oxides and their outer dimensions (chip size) are not in accordance to the recently developed mechanical design. Moreover, due to the four different design options on the PXD6 wafers there are not enough matrices of one type available to equip a full layer.

Answers: Sensors (cont.)

Q3: Has the collaboration set a hard, definite date for decision on final layout. In other words, what is the latest a decision can be taken for submission of final design for production sensors? What is that date?

Answer:

The final production is planned to be started by beginning of next year. At this time the wafers will be sent out for wafer bonding and therefore the outer dimensions and the p+ backside implantations have to be defined. An important date is December 2010 when the sensor geometry will be frozen. Until then all Belle II parameters affecting the geometry of the PXD must be known, such as the length and outer radius of the beam pipe and its orientation relative to the Belle II solenoid, and other constraints from the machine. The production of the top side starts in April 2011 which sets the dead line for pixel designs.

Answers: Sensors (cont.)

Q4: Is there a plan to have a prototype run with all parameters at their final values? How long will that run take and when will production devices be available?

Answer:

As stated above there is no time for a further prototype run due to our turnaround times of about 16 months. The plan is to have the sensor available by May 2012.

Next: Matrix Operations

Matrix Operation

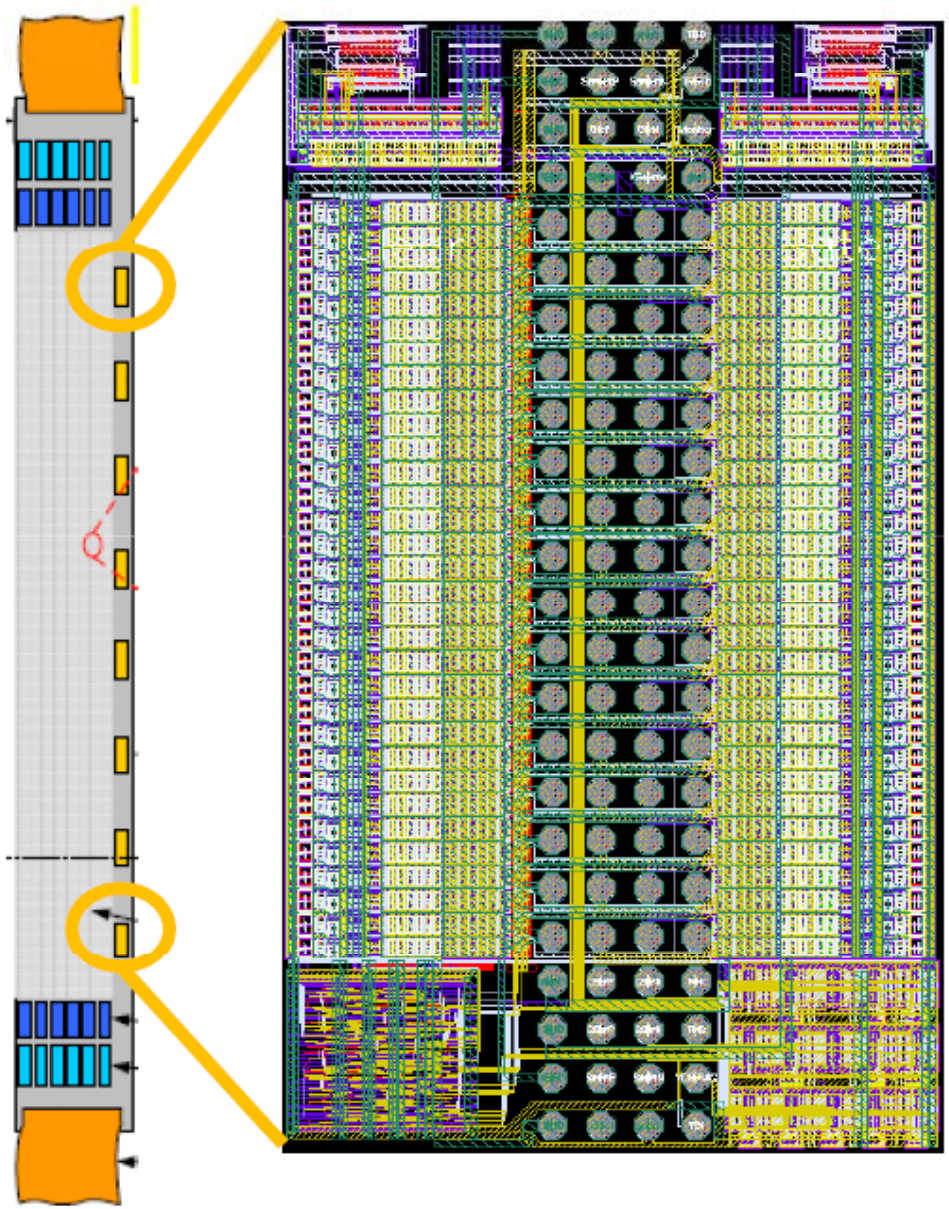
There are large voltage swings during the operation of the DEPFET. Voltage swings of up to 30 V are foreseen on column lines with a load capacitance of 50 pF in 10 ns. This corresponds to a current of 10 mA per row.

Q1: There is clearly a lot of current flowing through the device with many opportunities for serious noise and grounding issues.

Answer:

We intend to place significant decoupling (mainly on the final Switcher ASICs), so that the majority of the charge is coming from the local capacitors. A local source connection from the matrix to the chip should close the current loop (and see also answer to Q3).

ASIC Production: „Switcher B“



- Matrix steering of Gate & Clear
- 32 × 2 channels

- 3600 × 2035 µm²
- Bump bonding only
- Compatible to balcony layout
- ‘Final’ geometry

- Fast HV switches up to 30V
- Radiation Hard design

- Submitted to AMS on 15.2.2010

(Heidelberg, just arrived)

Answers to Matrix Operation (cont.)

Q2: The Switcher also has a floating digital ground which could be susceptible to pick-up.

Answer:

We use a digital 3.3V supply with a very large tolerance in voltage range (~2.5V-3.5V). All signals operating during matrix operation (clock and strobes) are differential. We do not expect crosstalk / pickup problems here.

Answers to Matrix Operation (cont.)

Q3: Has a thorough electrical analysis been performed of current flows and grounding?

Answer:

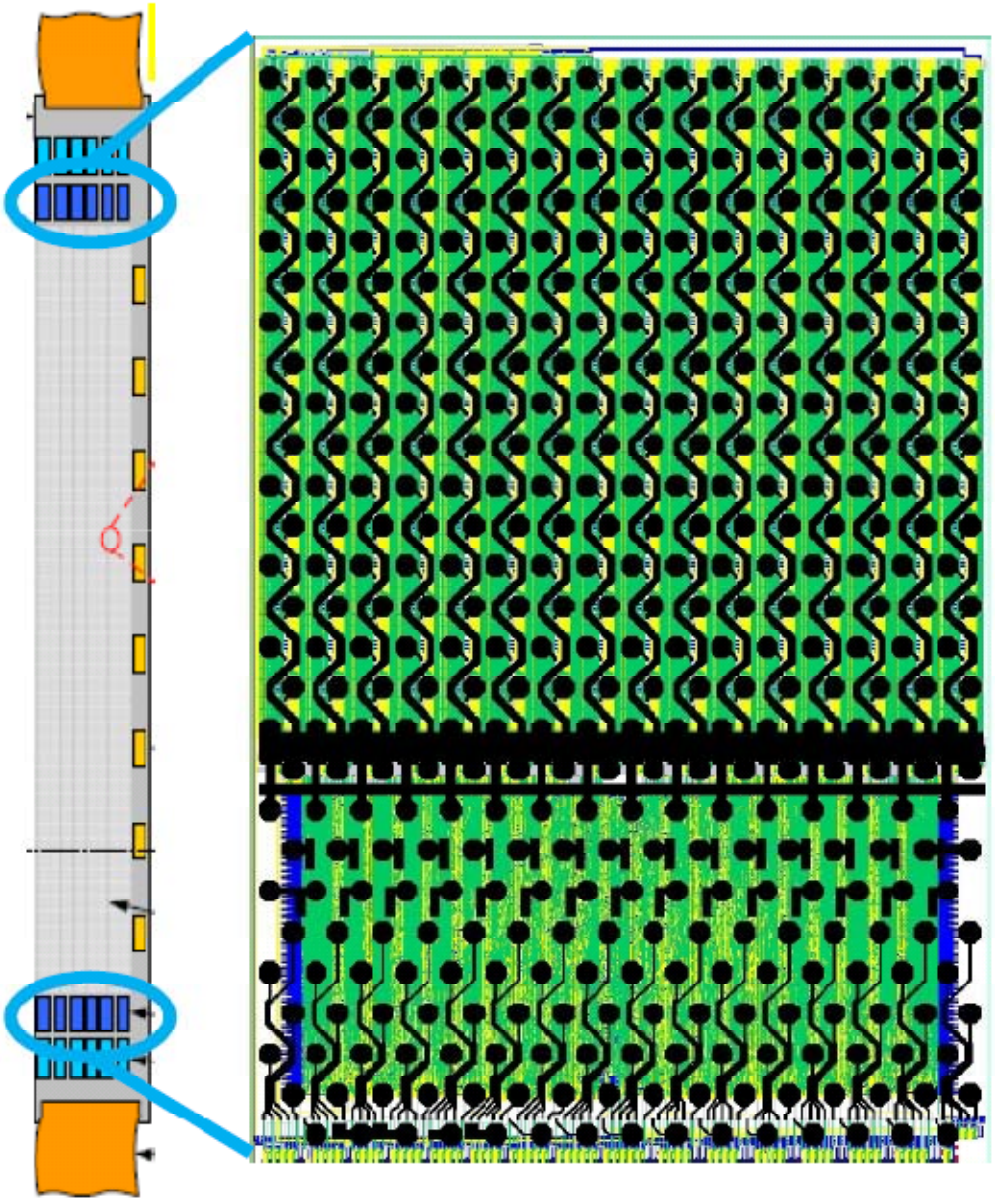
Such a simulation is not easy as the capacitive couplings in the matrix are expected to be very important and need to be modeled carefully. We are working on this issue on three fronts at least:

- A full mixed mode system level simulation of DEPFET / matrix (rc) / switcher / DCD has been set up and is running. It uses a self-made detailed DEPFET model and detailed level transistor models for the chips.

- The electrical interconnect of the balcony signal & power traces has been extracted (to a certain level of detail) and is being included in this system level simulation.

- 3 D extraction tools are being used to extract detailed capacitive models of the DEPFET and the on-sensor wiring. This will be an important ingredient for a refined system simulation.

DCD („DCDB“)



- Amplification & Digitization of Drain Currents
- 256 analog inputs
- 64 digital outputs @ 350 MHz

- 3240×4969 um^2
- Bump bonding only (w. redistribution)
- ‘Final’ geometry

- Sampling period: ~92 ns
- 8-bit ADC in **every** channel
- 30 - 60 nA simulated input noise

DEPFET: mip: ~1600 nA

Chip is back now, including bumps, seems to work !!

Answers to Matrix Operation (cont.)

Q4: Is there a plan to characterize the noise performance with real module as soon as possible? (see also comment below on support structure).

Answer:

We agree that this is one of the crucial questions and are aiming at early measurements. The problem is that large matrices with realistic RCs are required for worst case situation. These will become available in the fall of this year (PXD6 prototypes).

Answers to Matrix Operation (cont.)

Q5: If the anticipated smaller threshold shifts after irradiation due to thinner oxide layers and added nitrite layers are not achieved, what is the maximum voltage range of the control electronics and at what radiation dose would that be reached?

Answer:

Since we have already tested a thinner dielectric showing drastically reduced flat band voltage shifts of only 3V at @10Mrad the operation is not limited by the (even improved) voltage range of the switchers. The goal of PXD-TO is to find a sandwich dielectric with an even better radiation hardness in order to be prepared for inhomogeneous radiation damage within one ladder.

Next: Pedestal Dispersion and Response Variation

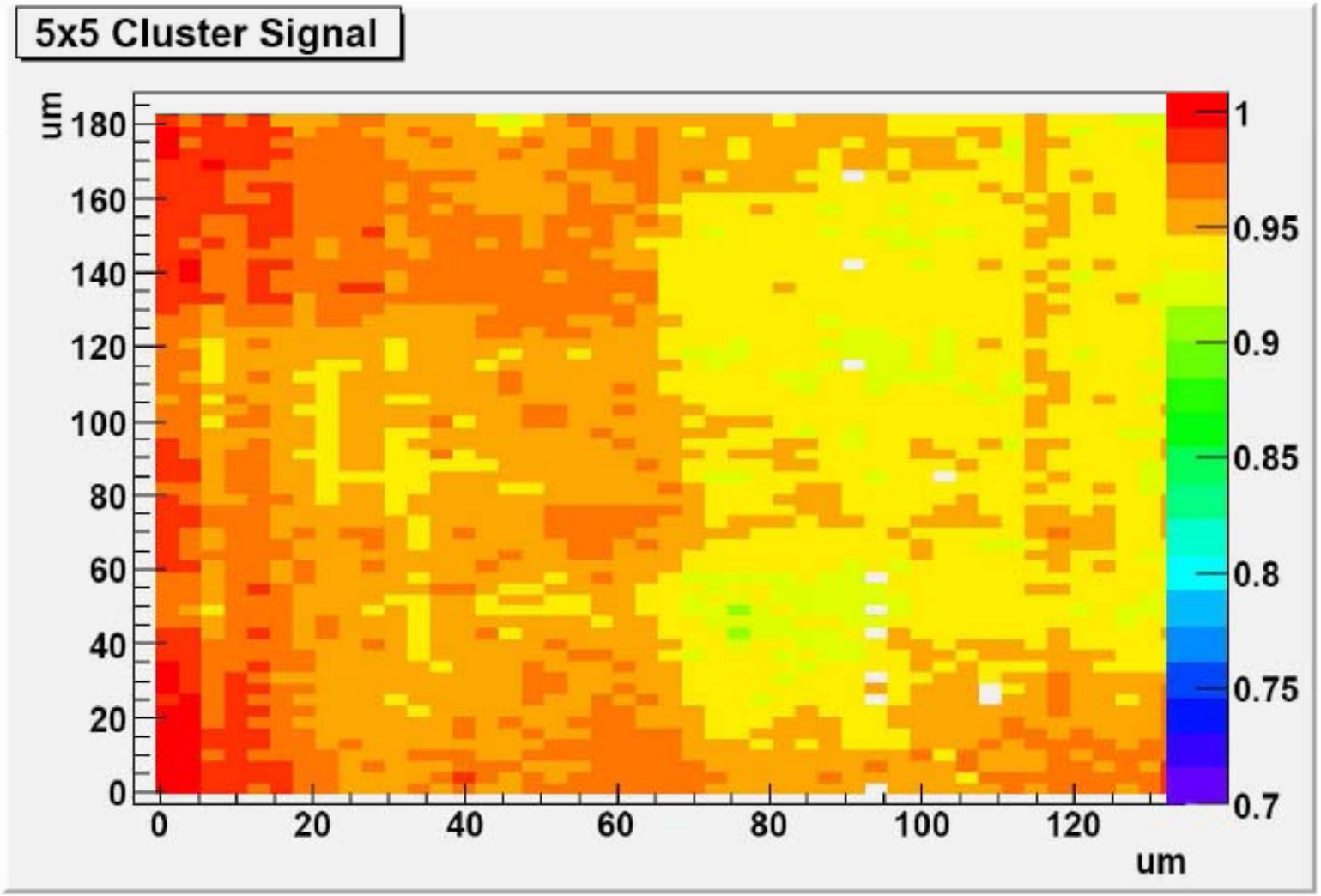
Pedestal Dispersion & Response Var.

Q1: In figure 4.21 there seems to be a more than 10% variation in response across the pixel matrix. Is that expected? The pedestal dispersion might still be rather large in single sampling mode.

Answer:

Figure 4.21 shows the dispersion of a 5x5 cluster signal, not the pedestal dispersion. We do not see a problem since Landau fluctuation will dominate in any case. However, gain and pedestals variations are caused mainly by the spread of channel length and implantation doses. Both are now much better under control due to improved etch techniques and a recently installed implanter at HLL. The observed variations are not a problem for the operation of the matrices. The resulting gain variation can be corrected if necessary by the pre-calibration of the matrices. Additionally, operation of the matrices in the last year (probably because of the more stable power supplies) resulted in more homogeneous behavior of the matrices. A gain correction was not necessary.

Answers: Pedestal Disp. & Response Var. (cont.)



10% variation

Signal Dispersion (ILC-type, PXD5)

(mainly caused by spread of channel length and implantation doses now better under control

Answers: Pedestal Disp. & Response Var. (cont.)

Q2: Why was a 2-bit rather than a 3-bit DAC in the DHP chosen to address the dispersion?

Answer:

The initial strategy was a straight forward design with an ADC with a wide range to cope pedestal variations (the 8 bit are not needed for resolution / noise reasons). In the R-C-R scheme, NO DAC is needed, if the input sampling cell can take enough current variation. This is possible, but adds noise. One reason to add the DAC was therefore to relief the sampling cell from large currents and thus to reduce noise. But again, it is NOT mandatory for this mode. As it turns out, the theoretical advantage of the RCR (1/f noise cancellation, current independence) is eaten up by the required shorter processing time (increased white noise) and therefore the single sampling (Read-Clear) has been (re-) introduced.

Answers: Pedestal Disp. & Response Var. (cont.)

We think that 2 bits are sufficient from the following estimation:
- 2 Bits, if set ideally, effectively quadruple the ADC range.
- This leads to 8 + 2 = 10 Bit, i.e. 1024 steps.
- Assuming a 50uA DEPFET bias current and a conservative 20% variation gives a 10uA dynamic range (the major part of the bias current is subtracted with a constant current source).

- Using the above 'ideal' 10 Bit would lead to a LSB of 10nA which still better than what we need (This corresponding to an ADC noise of 30e at a gq of 300pA/e, which is significantly below our noise goal of 200e.). In practice, the present gain setting of the chip does not allow to come to such small LSB steps of 10nA. The highest possible gain range has a LSB of 16nA, an ADC range of 4uA and a full range (with DAC) of 16uA. We are therefore prepared for an even larger current spread in the matrix.

Answers: Pedestal Disp. & Response Var. (cont.)

Note that the gain of the TIA in the DCD can be decreased in the present design via software, so that the LSB can be further increased, yielding an even higher range.

The least sensitive range has an LSB of 64nA, an ADC range of 16uA and a full scale range (with DAC) of 64 uA, so that we can basically work without the extra fixed current source. As we store the DAC data in the DHP and transfer it to the DCD (to avoid memory in the DCD), we have to limit the amounts of pads/signals and therefore the number of bits.

It is clearly a possible later optimization to increase the DAC resolution while decreasing the ADC resolution.

Answers: Pedestal Disp. & Response Var. (cont.)

Q3: What is the preferred pedestal subtractions scheme: R-C-R?

Answer:

We presently prefer single sampling (if dispersion allows) for its better noise performance and safer 'fast' operation.

Q4: What is an acceptable pedestal dispersion and drift before it starts affecting the data quality and data analysis?

Answer:

From the electronics point of view, we can safely live with a 20% pedestal variation. We envisage to do an online pedestal update during data taking.

Bonding

Under-bump metallization (UBM) for the frame done at HLL. The DCD and DHP chips have 200 µm bump pitch.

Q1: Have chips been obtained from vendors with the UBM?

Answer:

The ASICs DCD and DHP are delivered bumped from external companies (UMC and IBM). These standard processes are widely used in the micro-electronics industry with commercially available area bumps with the pitch of 200 microns.

The DCD chip is already delivered with these bumps (SnAgCu) and is currently under test.

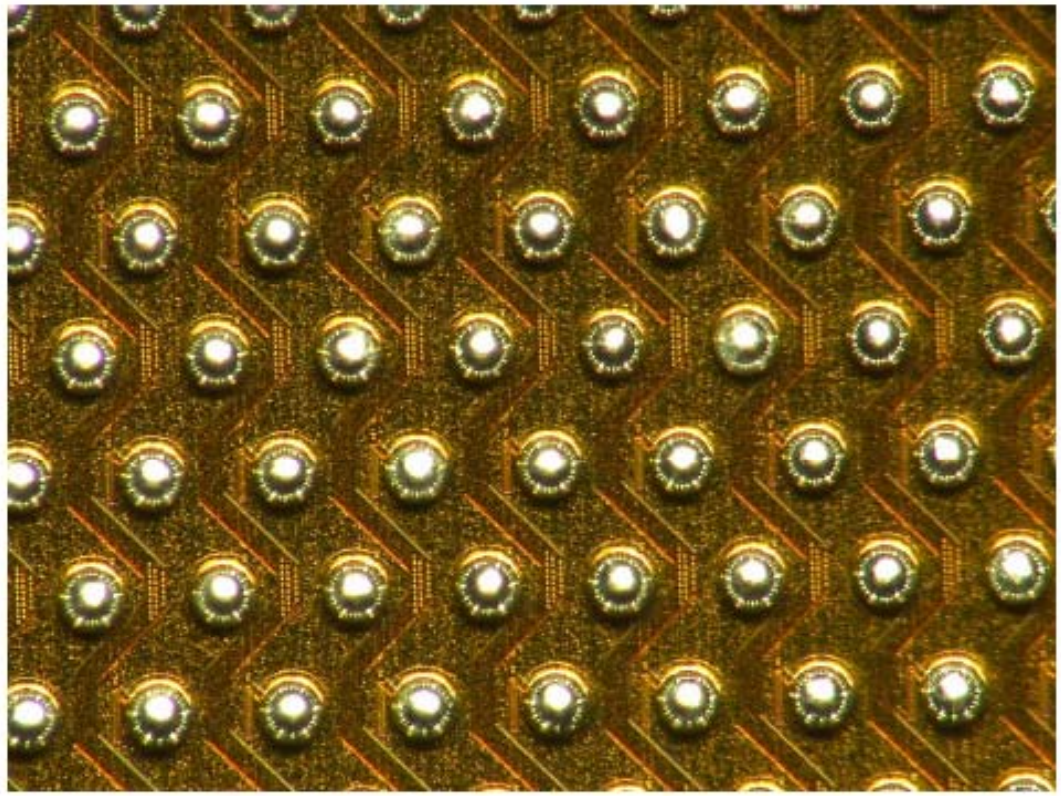
The DHP is ordered at IBM with "C4 bumps" (SnAg). We currently do not see any issues with the bumping of these chips.

Bonding (cont.)

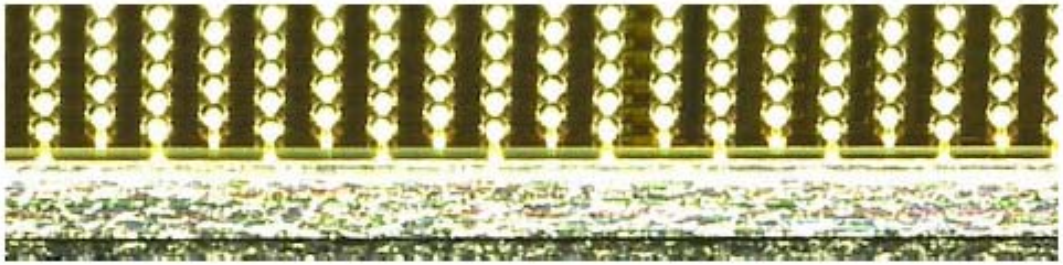
Q2: Have outside vendors been qualified?

Answer:

No. We rely on industrial quality of the provided chips.



Example:
bumped DCD chip
from UMC



Bonding (cont.)

Q3: The Switcher chip needs 150 µm bumps. Have bumps been placed on real chips and readout?

Answer:

The Switcher has to be bumped on chip level in-house (Uni Heidelberg). In this process the UBM is a (coined) Au stud on Al pads. On this UBM the solder bumps are placed using a solder jetting machine from PacTech.

Uni Heidelberg did the qualification of this procedure at the company itself and ordered this machine to have the process available within the collaboration.

Bonding (cont.)

Answer (cont.):

Bumps have not yet been placed on the 'final' Switcher-B, which has just arrived, but on several other chip designs manufactured in the same technology with similar pitch bumping has been successfully carried out.

There is no electronics under the pads, so the gold stud process is not expected to introduce any risk. Note that the need for in-house gold stud bumping for Switcher mainly comes from the fact that AMS/Europractice (as far as we have found out) are not providing bumped ASICs on a MPW basis.

Using a smaller pitch also helps to keep the chip small.

Bonding (cont.)

Q4: To accomplish the bumping, do PXD detectors have to be shipped from HLL to various vendors and collaborating universities?

Answer:
The UBM (landing pad) on the sensor substrate is an integral part of the sensor production and will be done at HLL. First tests with this process to check the compatibility with the sensor production have been done and show that there is so far no problem with the integration of the Cu layer into the sensor process flow.
The Flip-Chip connection between ASICs and sensor is again a standard procedure in the micro-electronics. The ASICs are bonded to the landing pads on the thick region outside the sensitive area (unlike ATLAS, CMS etc.), there is no pressure applied to the ASICs and the back side of the sensor is protected by the handle wafer throughout he entire procedure. The bump bonding (flip-chip) will be done at least two institutes (CNM Barcelona and Uni Heidelberg). The shipment of the ladders is planned to happen in dedicated transport and test fixtures.

Half-Ladder Joints

The half-ladders are joined through V-grooves and then glued. The V grooves are etched in the silicon.

Q1: Is the etching process such that it provides the reproducibility you are looking for each ladder?

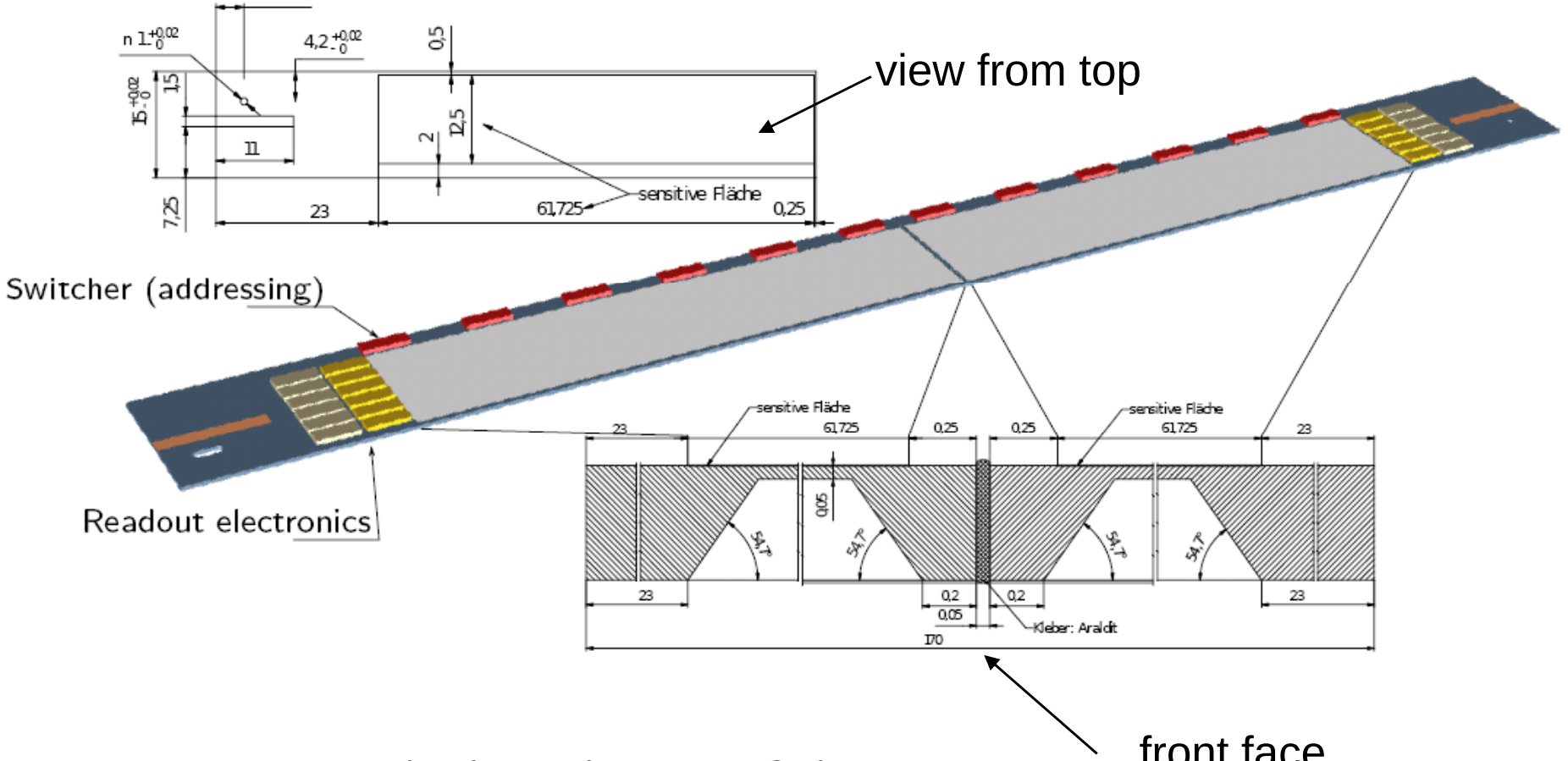
Answer:

The etching of the grooves is part of the back-thinning process. The reproducibility is given by the etching process itself and the single crystal structure of the handle wafer. The depth is given by the thickness of the top wafer. In this sense it is very well reproducible within a few microns.

Glueing Schemes for Half Ladders

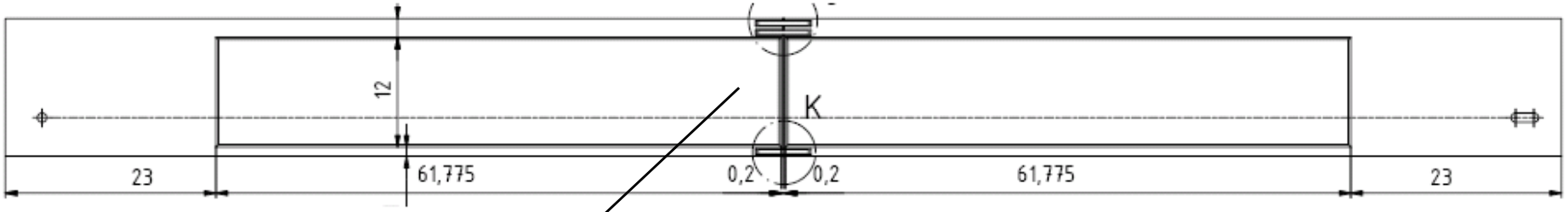
Simulation showed no significant impact of dividing both layers

➡ also inner layer will be divided to improve yield

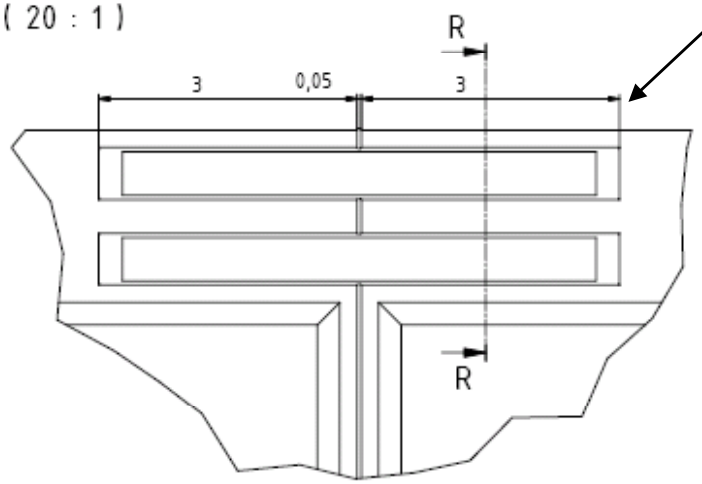


- $\sim 550\,\mu$m dead area because of glueing
- module length of 136 mm respective 170 mm
- fully covering acceptance now

Glueing Schemes for Half Ladders



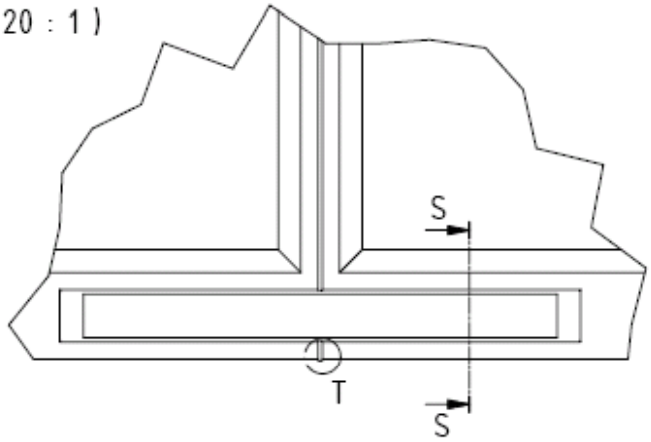
J (20 : 1)

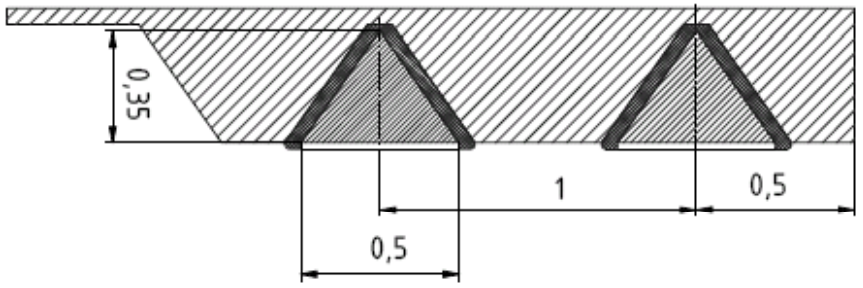


Design: Use front face glueing, reinforced using Al_2O_3 "prisms"

First batch of prisms have arrived, tests have been started with thick and thinned dummy ladders

K (20 : 1)





Tests done: pull OK up to 3 kg (thin dummies)
bowing OK up to 1 mm

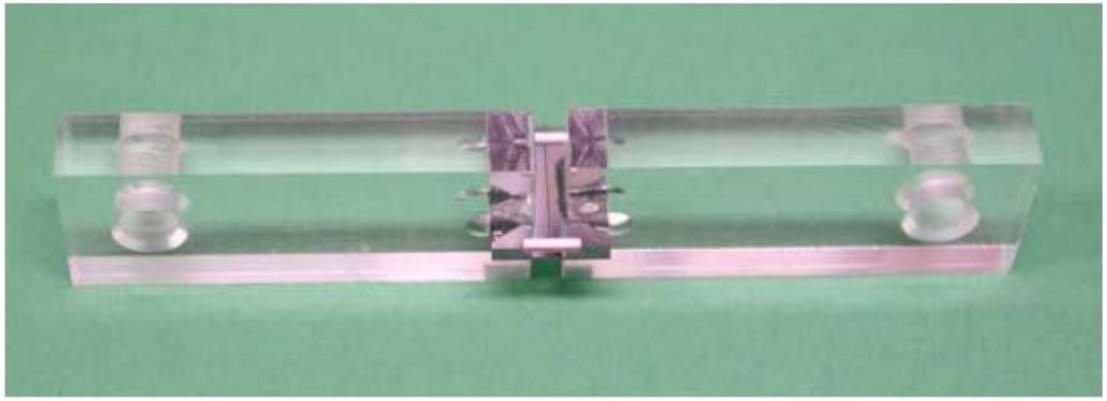
Half-Ladder Joints (cont.)

Q2: Most likely the ladders will not be perfectly flat but have a small “kink" to them. What is the maximum kink that is acceptable. What fixturing is foreseen to glue the ladders?

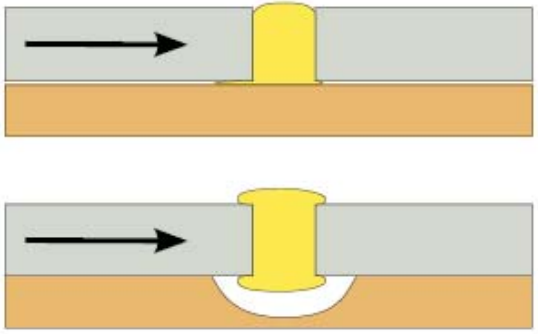
Answer:

We know that the ladders have an inherent bow in the order of 50 micron over 10 cm. This is elastic and will be corrected for during the joining of the half-ladders. The fixation will be done on dedicated gluing jigs with vacuum or mechanical clamps to the insensitive areas. This procedure has been tested on silicon samples and the results are excellent, giving us reassurance that the glueing is not the mechanically weakest part of the ladder

Details of Tensile Stress Tests



- undivided silicon tested with 7 kg
- glueing to be optimized: Ultimate strength varies between 4.5 kg and more than 6 kg

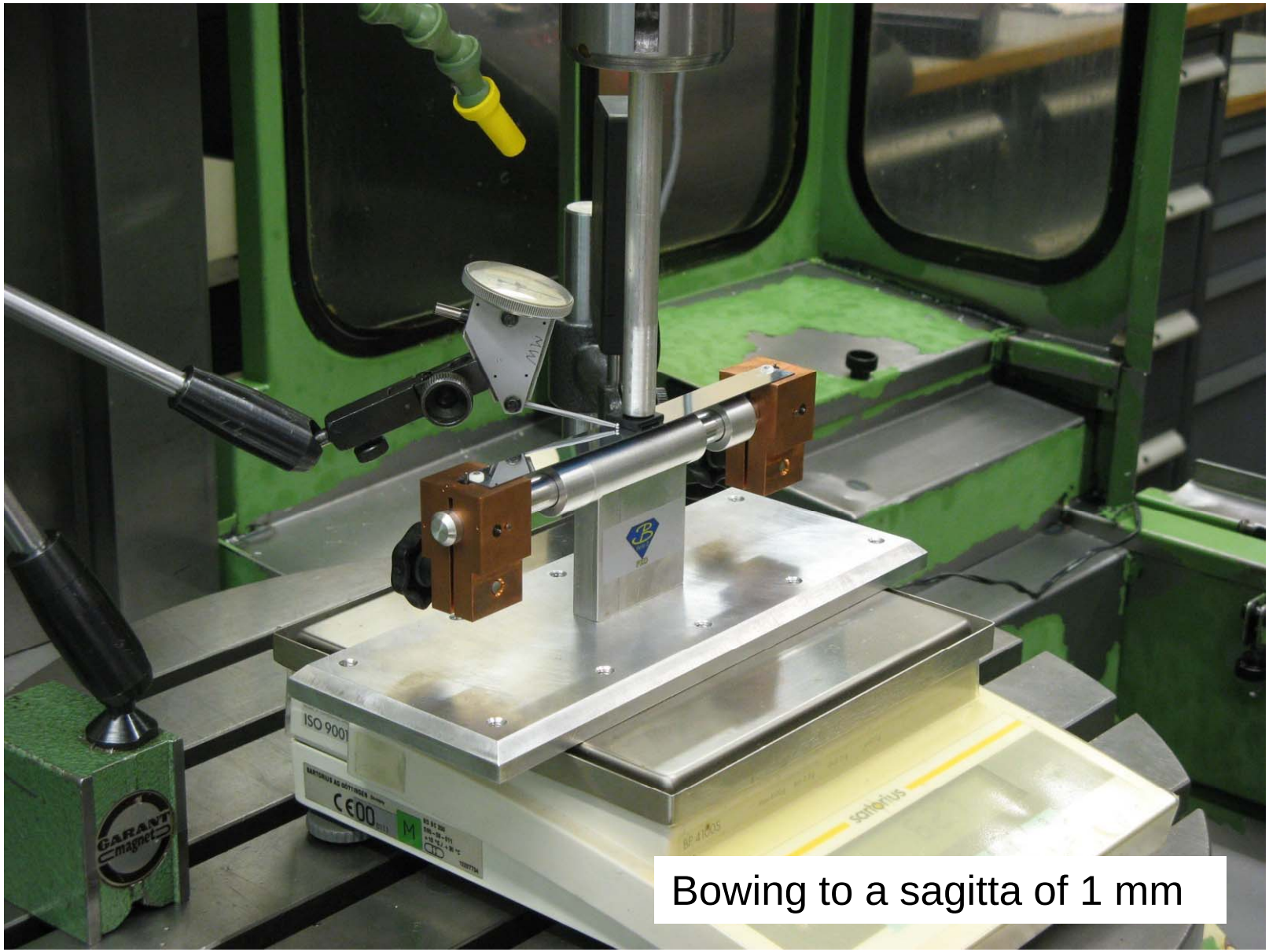


(MPI)

- No significant difference between reinforced and simple glue

… also done with thinned dummies now !

Details of Bowing Stress Tests



Bowing to a sagitta of 1 mm

Half-Ladder Joints (cont.)

Q3: Once the half-ladders are glued, what optical inspection is done to measure the flatness across the whole ladder. Also here, what is the maximum deviation across the ladder that can be tolerated?

Answer:

The optical inspection will be done with optical profilers available within the collaboration. A maximum kink is not yet defined. A hard boundary is the space between two ladders (about 0.42 mm), bowing and "kinks" within this range can be corrected for in the alignment procedure. However, we do not see any mechanism to generate such large sagittas, even when testing the glued ladders under extreme temperature variations.

ASICs and Irradiation Tests

Many ASICs are not yet available in their final design.

Q1: Are irradiation tests foreseen for all final designs?

Answer:
All final ASICs will be irradiated with X-rays. Prototypes of the ASICs have been radiated with X rays already to a level of 35 MRad. Further irradiation tests will be done in an electron beam both for the ASICs and the sensors.

Q2: How much time will that take?

Answer:
X-ray irradiation can be done in Karlsruhe with 0.5Mrad/h with a very short lead time. Switcher Irradiations have been carried out in 3 days. We therefore expect no delays from this at all.

Testing Components

It seems that an intermediate test of various parts will be carried out, that is to say, with not the final components and/or the final configuration. To retain the flexibility to exchange parts, we understand that that is required.

Q1: When does the schedule call for start of testing ladders in their final configuration?

Answer:

Testing of the final ASICs (available by March 2011) will happen well before the assembly of the final ladders and, if some problems are observed, there will be enough time to do resubmission and retesting. PXD6 will also allow testing of the final configuration on the half-ladders in a special test environment without the final ASICs.

Testing (cont.)

Q2: Is there enough contingency in the schedule to complete the project on time when an unexpected issue is uncovered?

Answer:

As far as we can see now, the only cause that could severely postpone the project would be problems in the PXD sensor production where the turnaround takes about 16 months.

Data Rate and Readout

The front-end data links can handle an occupancy rate of 2%. This, however, is an average occupancy rate. The backgrounds will most likely not be azimuthally symmetric.

Q1: Suppose the background rate in the horizontal plane reaches sometime 4%. How would this affect the pixel detector data? Would data be truncated?

Answer:

We have built in a factor of 2 safety in the DAQ system. So an occupancy of 4% could still be tolerated, if the readout is triggered with no more than 30 kHz. On the other hand, such a high occupancy would clearly create problems in the precise reconstruction of tracks using the PXD.

In addition, we are working on a data compression algo on the DHP

Data Rate and Readout (cont.)

Q2: The TDR describes three readout systems for the PXD. How and when will a decision be taken which ones to pursue?

Answer:

We have set up a working group to deal with the preparation of the decision process. All options are pursued at present, we foresee a date of decision by spring of next year, based mainly on performance (efficiency of finding the correct ROIs).

Ladder Assembly and Testing

The ladder assembly is preceded by extensive tests of the individual components. When the ladder assembly starts, a test is carried out after each component is mounted, such as the switcher chip or the DCD, etc.

Answer (short description of the procedure):

Once the ladders are produced, a pre-selection of matrices will take place using probe station measurements. The selected ladders will be shipped to the flip-chip facilities. We plan to do partial sequential tests during the ASICs assembly. For this we need the DHP chip for the DCD and SWITCHER operation.

Ladder Assembly and Testing (cont.)

Answer (short description of the procedure, cont.):

After the final reflow of the chips the final testing of a half-ladder can take place using a probe-card to establish contacts to the bond pads for the Kapton cable (before the cable is assembled).

The characterization of the ladder performance with a source and a laser will then take place. Selected half ladders are then glued together into the module and fixed onto the transportation jig on which also the final performance test is done. 2 weeks are planned for the characterization and module assembly. The ladder assembly is planned to be done in a parallel and interleaved manner.

Ladder Assembly and Testing (cont.)

Q1: What yield is assumed for each step?

Answer:

From past experience with devices of similar size and complexity (for high energy physics and astrophysical applications) we conservatively expect a yield for the DEPFET production of 50 %. In similar semiconductor devices the HLL routinely obtains a better than 80% yield. The expected yield of the flip chipping is high due to the relaxed pitch (standard procedure, see above) we have in our ASICs. The yield for the full ladder assembly is also assumed to be 50% (again conservative: for the ATLAS pixel detector a yield of 90% was reached in the assembly procedure). In total we count on a yield of working ladders of better than 25%. With this yield we will produce at least 40 complete and functioning ladders (20 are needed for the PXD detector).

Ladder Assembly and Testing (cont.)

Q2: What actions are envisioned when a step fails?

Answer:

The actions will depend on the nature of the failure. No show stopper is seen, a major delay will only occur if the DEPFET production runs into problems.

Q2: If the bump-bonding of one of the ASICs has a problem, is it possible to remove chips?

Answer:

In case of problems with the flip chip procedure, individual chips can be removed and new chips can be placed instead. This procedure has been tested successfully already in Heidelberg.

Ladder Assembly and Testing (cont.)

Q3: How much time is allocated to producing, testing and certifying a full ladder? Does the schedule assume ladders being produced in parallel?

Answer:
The estimated time for the assembly of the 2 half ladders (one module) is 1 week (including possible rework). This procedure will take place at the University of Heidelberg and probably at CNM Barcelona in parallel. After a successful test of the half ladder it is shipped back to Munich and the Kapton cable will be assembled and the final test of the half ladder performance will be done. Assuming the sensor production starts in April 2011 and finishes by June 2012 we will have less than a year to assemble all the ladders. Planning for parallel assembly and testing, we can have 40 modules tested in about 42 weeks (just on time for May 2013). In parallel to the testing of the ladders testing of the system readout can take place as soon as a certain number of ladders is produced and characterized.

Kapton Readout Cable

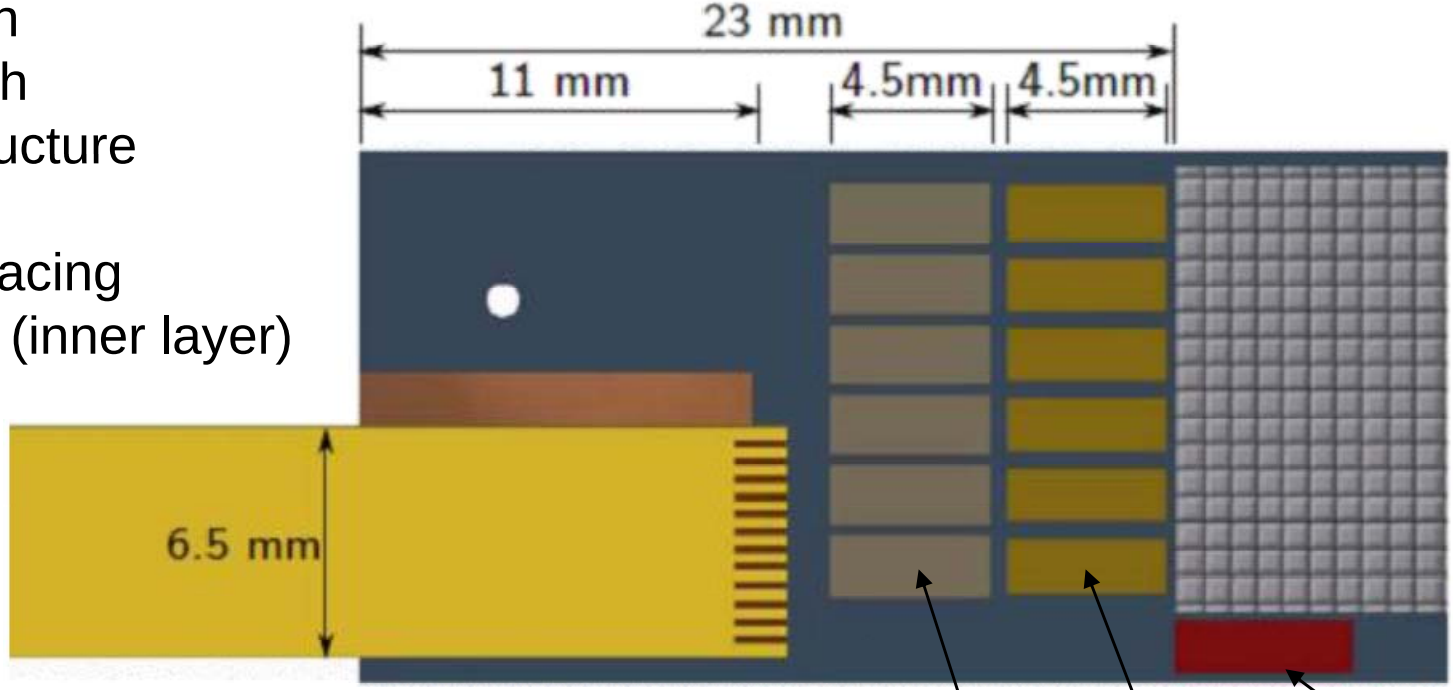
The TDR says almost nothing about the specifications of the kapton cable. Sometimes the information is conflicting: at one point it says that this is a 3-layer cable and at another point a 4-layer cable.

Answer:

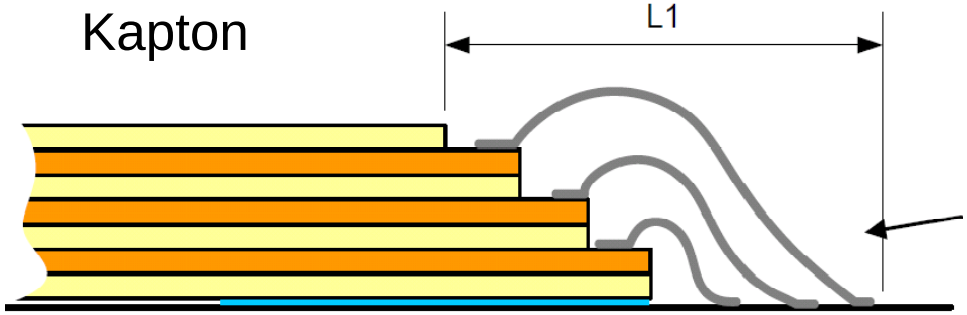
The Kapton cable is 3 layers. The "4-layer" cable is a misprint, sorry.

End-of-Stave Design

- Extended area for support/cooling
- Backside in contact with cooling structure
- front side facing beam pipe (inner layer)



Multilayer Kapton

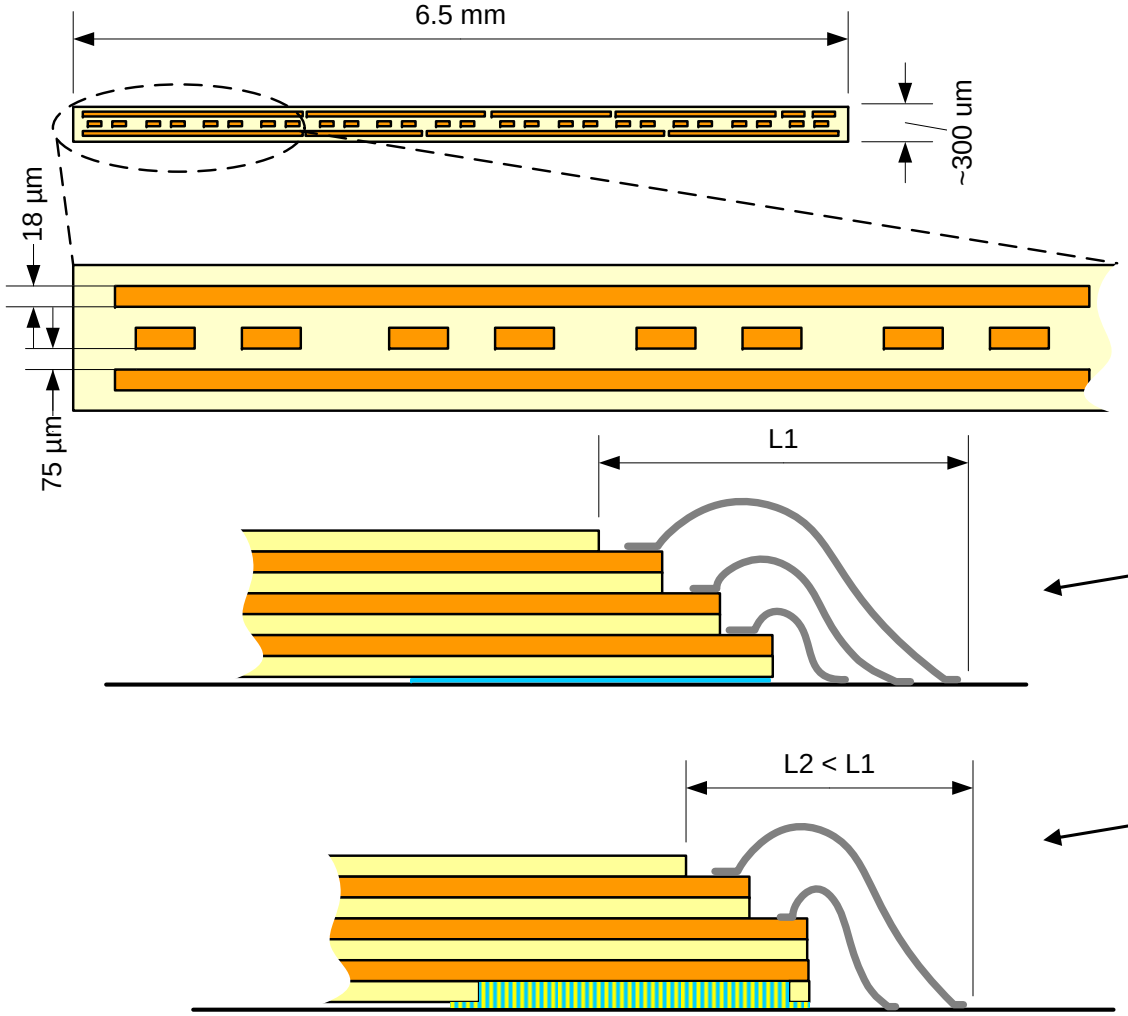


3 wire bond rows

(Data Handling Processor)

(Drain Current Digizer)

Kapton Readout Cable (cont.)



(split) power plane

differential strip lines

(split) ground plane

three wire bond rows, flex glued to substrate (electr. passive)

alternative option:

two wire bond rows for signal layer and top layer and z-axis glue (or solder or silver epoxy) for bottom layer

Kapton Readout Cable (cont.)

Q1: The cable seems to have 80 traces and a width of 7 mm and is 20-50 cm long. Can you provide us with some further cable specifications? What is the trace width, aimed trace resistance, capacitance, metallization for bondability?

Answer:

Baseline is a three layer kapton design with thick copper (35 µm) for the bottom and top layer carrying the power lines, and a thin (18 µm) inner layer for the impedance controlled differential signal lines. The impedance of these strip lines will be defined by the layer stack-up of the kapton and the line geometry to meet the default value of 100 Ohm.

Kapton Readout Cable (cont.)

Q1: These cables seems to be non-trivial. Has a vendor been qualified to manufacture these cables? Should a second vendor be qualified?

Answer:

We are in contact with a vendor and have ordered a prototype of the cable for testing. Since the necessarily small line width is critical, a qualification of different vendors is planned.

Next: Mechanics

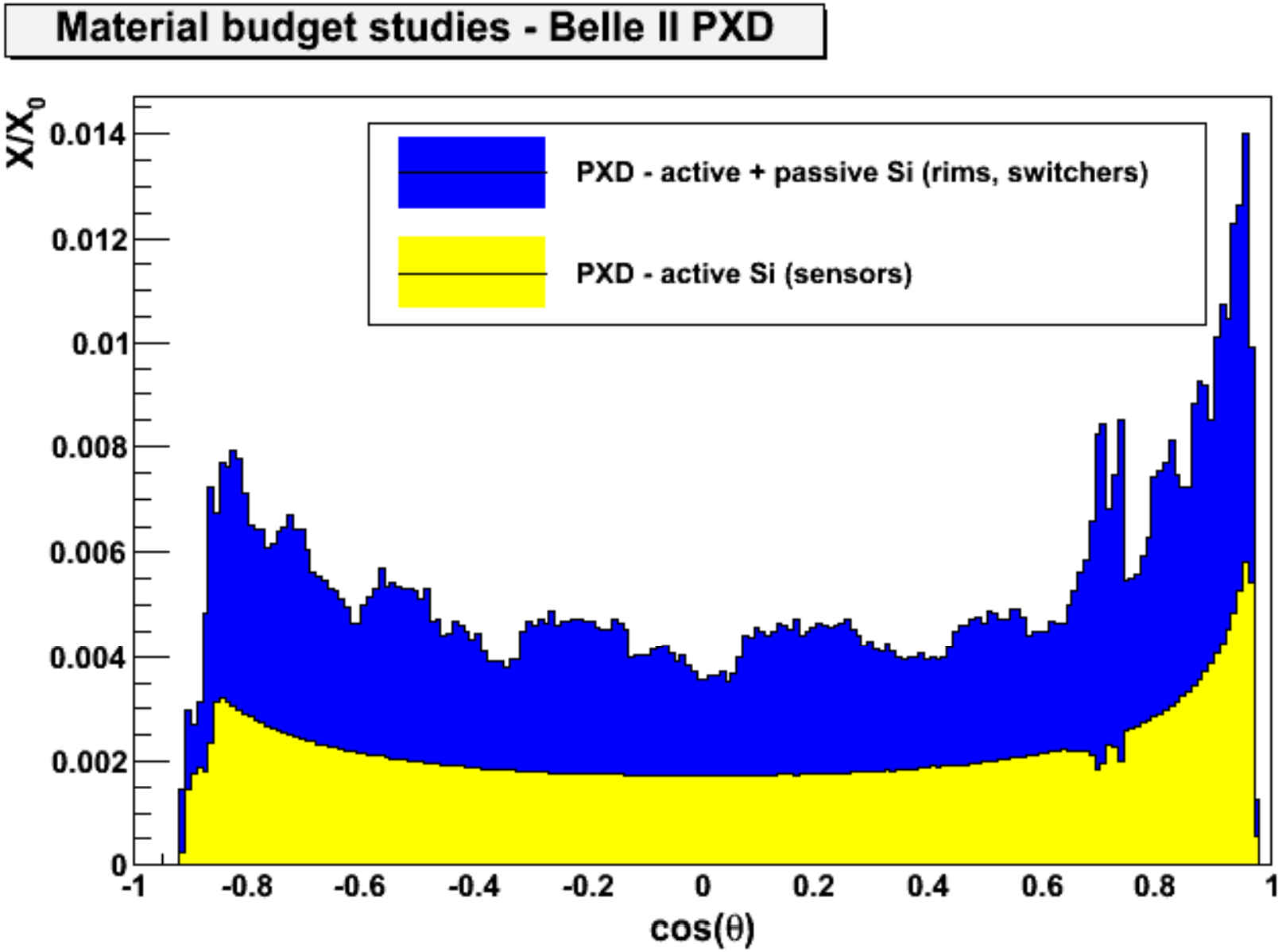
Mechanics

Comment by Panel:

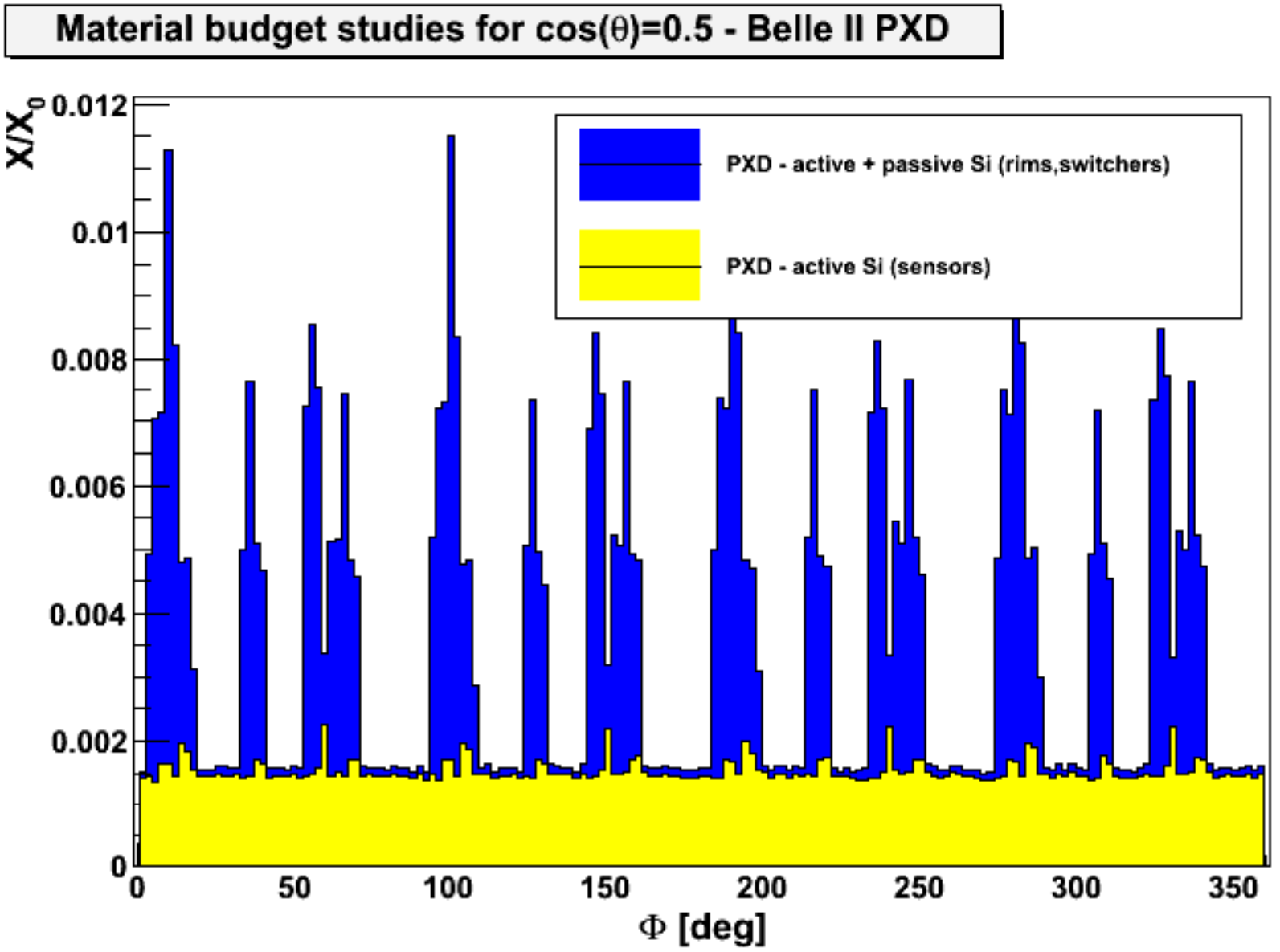
It would be nice to see a ray traced plot of radiation length as function of azimuthal angle, including all dead material such as gold traces, bumps and ASICs. Also, it would be nice to see the number of hits per track as function of azimuthal angle for tracks with infinite momentum and for tracks with momentum of say 40 MeV. The latter is aimed at understanding if there is a momentum bite where a particle could sail through the PXD without leaving any hits. (By the way, does Belle reverse the polarity of the magnetic field?)

Answer:
Detailed simulations have been done and the requested plots are available and will be shown in the presentation.

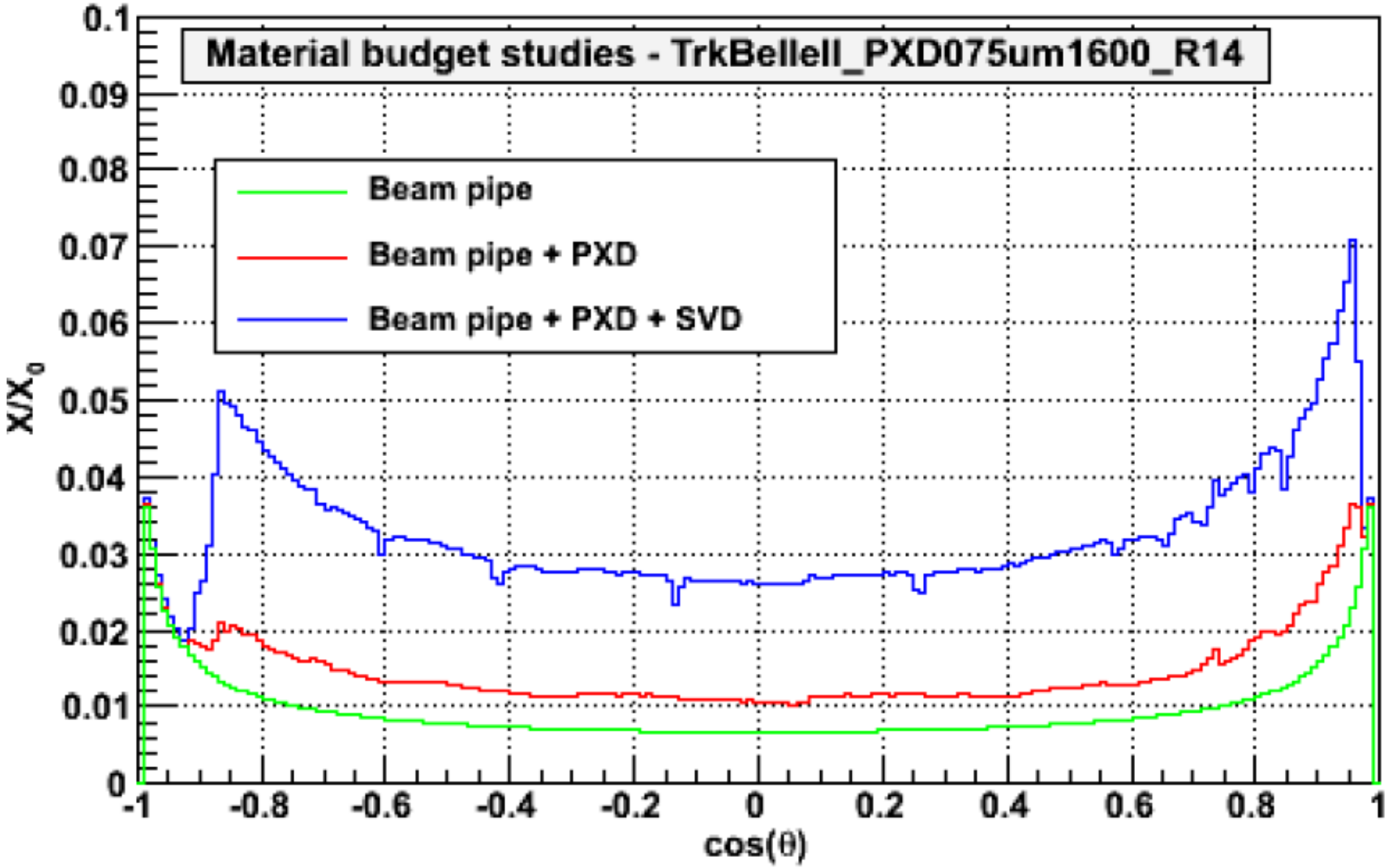
Materialbudget of the PXD



Materialbudget of the PXD



Materialbudget of Si-Tracking System



Mechanics (cont.)

Q1: The ladders are mounted to the support structure through grooves. What is the target mechanical accuracy for mounting the ladders and how reproducible is the mounting?

Answer:

Our engineers are confident that a 20 micron mechanical accuracy (controlled optically) for the mounting of the ladders (relative to each other) can be achieved.

The detector will be mounted on the beampipe, where the absolute position will not be so easily defined and verified.

The final point accuracy in the experiment is expected to be better than 10 microns since alignment with particles will be done.

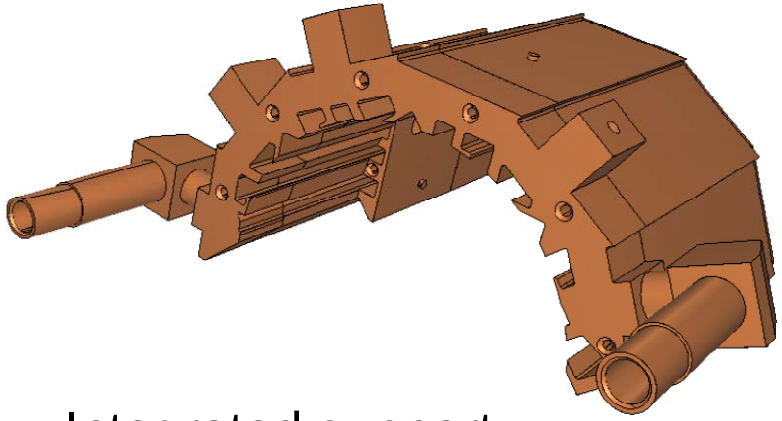
Mechanics (cont.)

Q2: The TDR is rather thin on the details of the mechanical design, although it is a critical aspect for this detector. It is my understanding that the support structure is made out of copper, which clamps onto the beam pipe. The ladders are screwed into the copper. Is the support structure not electrically isolated from the beam pipe? What is the grounding scheme exactly and what possible ground loops and noise sources have been considered?

Answer:

The grounding scheme is under discussion. It is clear that the PXD should be isolated from the beampipe. A first idea for the grounding is to connect each end of the ladder to the common inner aluminum shell of the CDC. Such a scheme would avoid ground loops and resulting current flowing though the ladders.

PXD Mechanics, Outer Layer



Integrated support
and cooling structure

ladders are
self-supporting
(>140 mm)

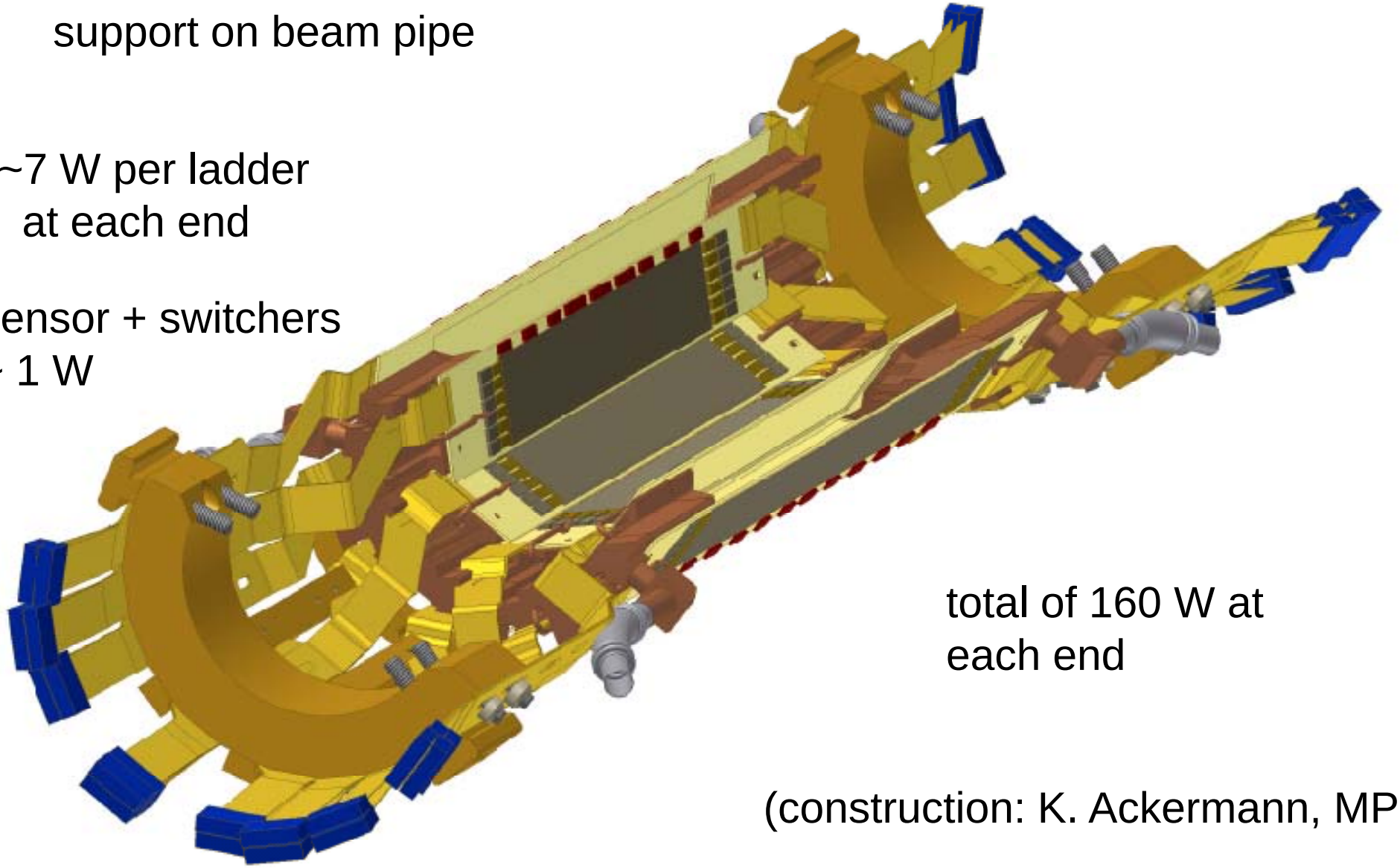
(construction: K. Ackermann, MPI)

PXD Mechanics, Inner Layer

support on beam pipe

~7 W per ladder
at each end

sensor + switchers
~ 1 W



total of 160 W at
each end

(construction: K. Ackermann, MPI)

Mechanics (cont.)

Q3: Two cooling options are discussed that are at almost opposite sides of the spectrum: liquid water- glycol cooling and evaporative CO2 cooling. The design implications are significant which option is chosen. What is the time scale for a decision between these two options?

Answer:

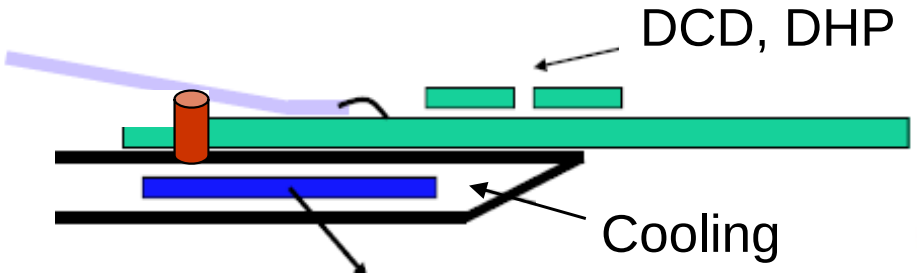
Recently, we have made a decision to opt for CO2 cooling due to its larger safety margin. We have an integrated mechanical construction for support and cooling of the ladder ends (end of stave), carrying the power-consuming electronics, which can be equipped with CO2 cooling pipes.

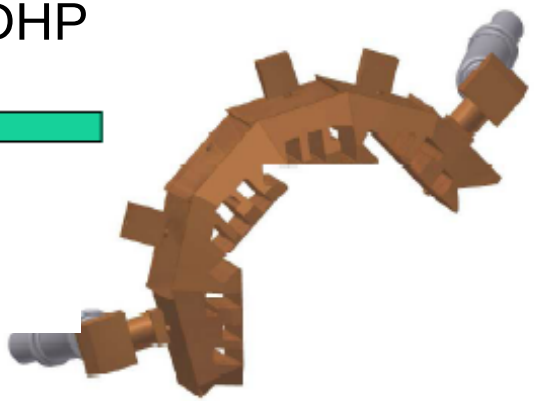
Because of the complex design, 3D prototyping (instead of standard machining) can be used, and stainless steel (less preferred because of its thermal properties, but better for high pressures and precise mechanics) will be used instead copper.

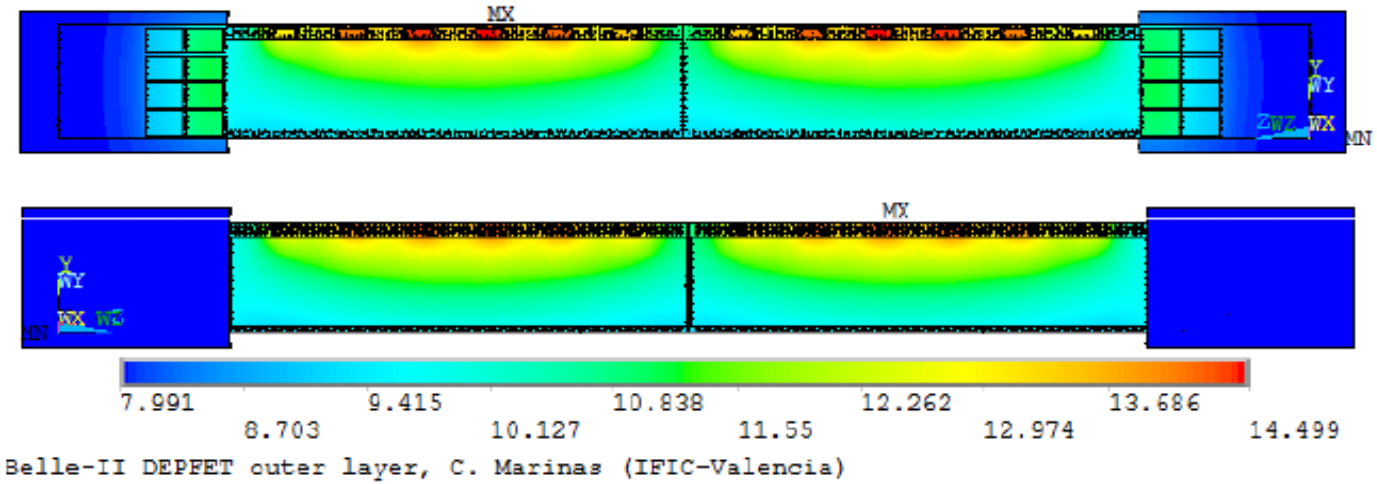
Cooling (Simulations)

Coolant most likely CO_2
(copy LHCb system)

Single Phase Fluid as backup
Additional air cooling
mandatory (1 m/s)







(Valencia)

ambient T (dry air)
~ -10° favored

required:
T(sensor) < 30 deg
T(ASIC) < 60 deg

Mechanics (cont.)

Q4: It is proposed to cool the DEPFET itself through air flow at a flow rate of 1 m/s. Although the flow rate is modest, the volume for the flow rate is very small. With very thin devices there is a clear possibility of vibrations. Has a vibrational study been carried out?

Answer:

Two air cooling solutions are under study and a test stand is being prepared for testing with real ladders. Although the sensitive area is very thin, the stability will be provided by the thick frame around the sensor. A thicker sensor (75 microns) will also help and the ladder will be more robust. The vibrations are strongly dependent on the air cooling option, so the studies are on the way, but we have no results yet.

Mechanics (cont.)

Q5: At what flow rate does the flow become turbulent?

Answer:
In order to know the fluid regime (laminar or turbulent), the Reynolds number has to be calculated; at this time, is very hard to establish that number, since the geometry and the boundary conditions are not finished. Parameters like the geometries of the module and the support structure, the temperature distributions and the mechanism to put the air in and out of the volume should be known before. A realistic mockup with sensor dummies is being prepared to study these questions in detail.

Mechanics (cont.)

Q6: How is the air brought into and taken out of the detector volume ensuring both layers are adequately cooled.

Answer:
In our present design of the 2-layer PXD we plan to bring in the air by pipes, blowing cold air between the two layers. The outer layer will be cooled by the common cold gas volume of the SVD.

Mechanics (cont.)

Q8: What is the margin built in for the cooling system? The same cold air flow is also used for the SVD. How are the two coupled to ensure adequate air flow to the PXD and that an air temperature of -5° C is really achieved at the entrance to the PXD?

Answer:

The proposed cooling solution (environmental temp = -5ºC, temperature at the cooling support = +8ºC) assumes a reasonable set of environment conditions.. CO2 can go down to -40ºC (with a pressure of 10 bar, that could also be beneficial to our support structures) and a temperature of -15ºC for the air is easily achievable.

Mechanics (cont.)

Q9: It would be nice to have a thorough overview of the mechanical issues at the review with a discussion of what mechanical engineering support is available for this project and what their experience is in building low-mass, small scale, high-precision silicon detectors?

Answer:

We will bring a real-size model of the PXD with cooling and support structure to explain the concept. The MPI engineering department has broad experience in building various types of particle detectors, including Si vertex detectors (e.g. ALEPH and ATLAS). There is also strong support from our collaborating institutions in Bonn, Karlsruhe and Valencia, who have acquired vast experience within the ATLAS/CMS experiments.

Mechanics (cont.)

Q10: Also, going over the actual installation process, and removal of the detector when the detector needs to be replaced, would be good (though it may be a bit early at this stage for details).

Answer:

This is a very important discussion and we are in close collaboration with the Interaction Region and the SVD.

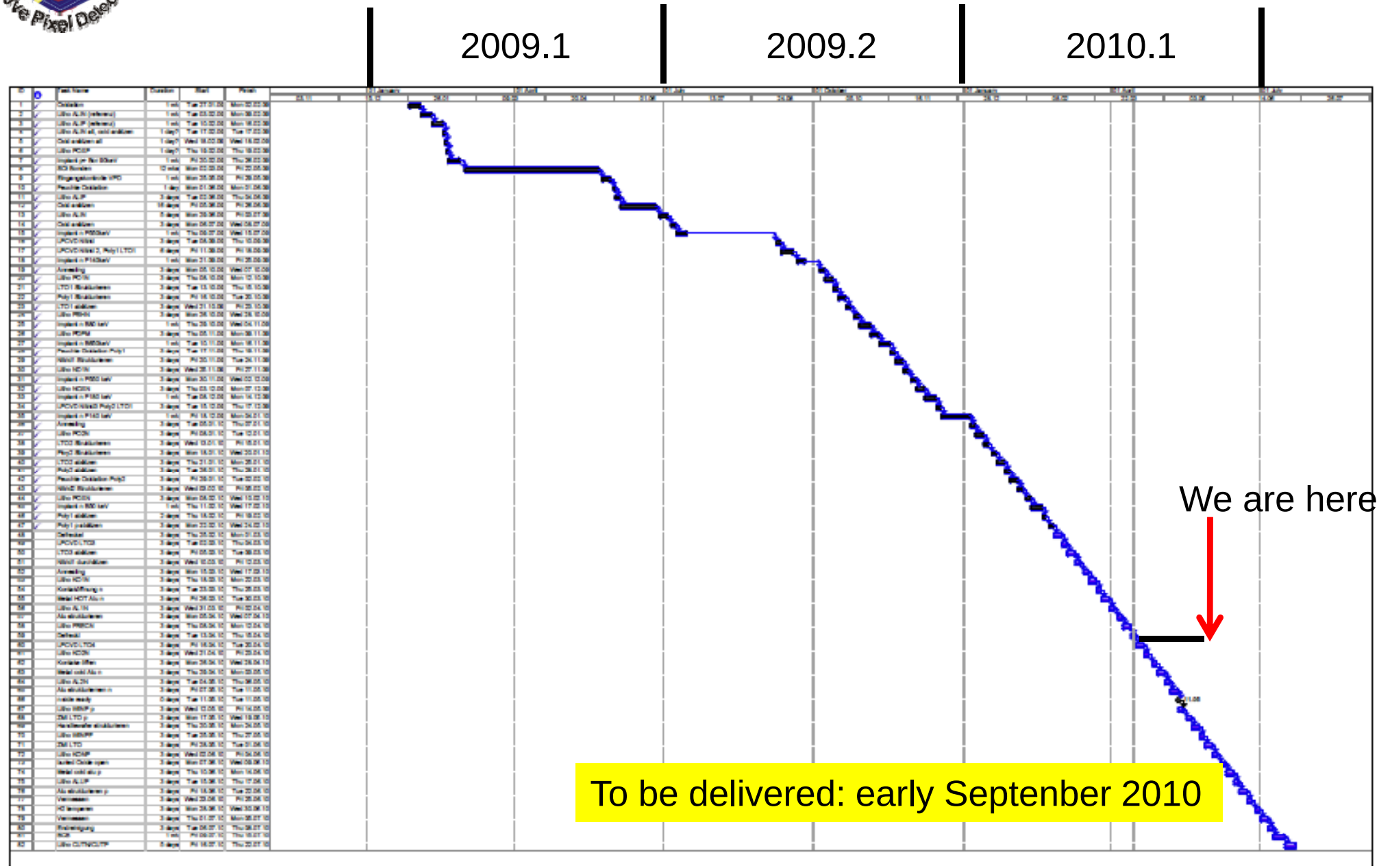
Schedule

Often, for highly complex detectors, a prototype phase and a preproduction phase is scheduled. Does Belle II intend to adopt a similar schedule?

Answer:

Time constraints do not allow for an extended prototyping phase for the PXD.

Production Plan for the PXD6 Sensors



Schedule (cont.)

Q1: The schedule calls for PDX7 preproduction. What are the goals of the preproduction run? Will the preproduction run settle on the final design parameters? The preproduction run is only 3 months long with no time allocated to testing. How will the final PXD7 wafer processing, which is to start in January 2011, benefit from this run?

Answer:

There is a misunderstanding here: The "preproduction" is not a "prototyping", it is the preparation of the SOI wafers, which cannot be produced (bonded) in the MPI Semiconductor Laboratory (HLL). The SOI wafers are a prerequisite to build the DEPFET sensors. Sorry for the misleading formulation.

Schedule (cont.)

Q2: Testing of the final PXD7 sensors and of the final production modules is missing from the schedule. Is that an oversight? What are the plans for a slice test, that is, a test of the full detector and readout chain? I believe this to be absolutely critical for the success of the detector.

Answer:

As detailed above, there is an extensive period envisaged of testing the sensors in many ways before it is assembled into the PXD proper. After assembly, a complete system test (powering, cooling, readout) will be performed, before the detector is packed up and sent to Japan. This final test will most likely take place in the Munich area, followed by an extensive testing and commissioning period at KEK, prior to the installation in Belle II .

Schedule (cont.)

Q7: If the thin-oxide/nitride program to make the sensors more radiation hard does not work out in time, the effects have to be compensated for by running at higher voltages which implies higher heat load.

Answer:

We consider the thin oxide as our baseline for the final production. We do not see any major obstacle to realize this feature (see above). Our expected heat load is determined from the simulations employing the "thick" oxide layer. On the other hand, the power consumption depends only on the voltage difference, not on the absolute value of the threshold voltage. Furthermore, the CO2 option will give us enough margin to cool to the desired level.

Specific Questions

p81, 4.2.2 How are the thinning runs going? What is the yield? MPI does all this processing 'as research' even for the PXD production? Doesn't sound commercially viable (9 processing steps, applying Cu in same foundry, ultra thin (4 µm or less) lines etc.). Almost sounds like there are 2 or 3 development steps over-and-above what was already being done for ILC.

Answer:

We have shown a few slides making it clear that the Semiconductor Laboratory of the Max-Planck-Society is a highly professional foundry for producing first class sensors for particle and astrophysics.

Specific Questions (cont.)

p82, 4.2.3 Choosing designs based on laser tests? To what extent have something close to the final design been validated with MIPs?

Answer:

Lasers (laboratory measurements) are very useful for testing the basic performance parameters of the DEPFET (and other semiconductor) sensors. ILC design DEPFETs from the PXD4 and PXD5 production have been submitted to exhaustive scrutiny in beam tests in the CERN SPS. Comparison with the laboratory measurements has allowed to validate the less involved source and laser measurements for some aspects of the characterization (i.e. we know the gQ measurement with a X ray source yields the same result as the same measurement with MIPs). PXD6 sensors will be tested in a high-energy pion beam in November 2010 if delivered on schedule. The fall-back solutions include a DESY beam test in January/February 2011 or an SPS beam test in May 2011.

Specific Questions (cont.)

p88, 4.3.4 The DHP *will be implemented* in 0.09 µm technology". So it is not even started yet?

Answer:

The DHP development has started beginning 2009. Submission of a first test chip with almost full functionality (but half the size of the final chip) was done in Feb 2010.

It is expected back for first tests by the summer.

Specific Questions (cont.)

p102, Fig 4.21 5 x 5 signal clusters? How big are the pads (50 x 50 or 50 x 75 µmm right)? Are laser pulses really representative of MIPs? Surely MIPs don't hit five x five pads?

Answer:

These measurements are performed on ILC-design matrices with small pixels (20x20 and 24 x 32 µm). The expected number of pixels with a signal over 2.6 sigma is 4.5 for perpendicularly incident MIPs (i.e. typically nearly all signal is well-contained in a 3x3 fixed-frame cluster). A well-focused 1060 nm laser yields similar results if used at MIP intensity and with excellent control of the incidence angle. Even so, for very large laser intensity the Gaussian intensity profile may leave a significant signal outside the 3x3 area.

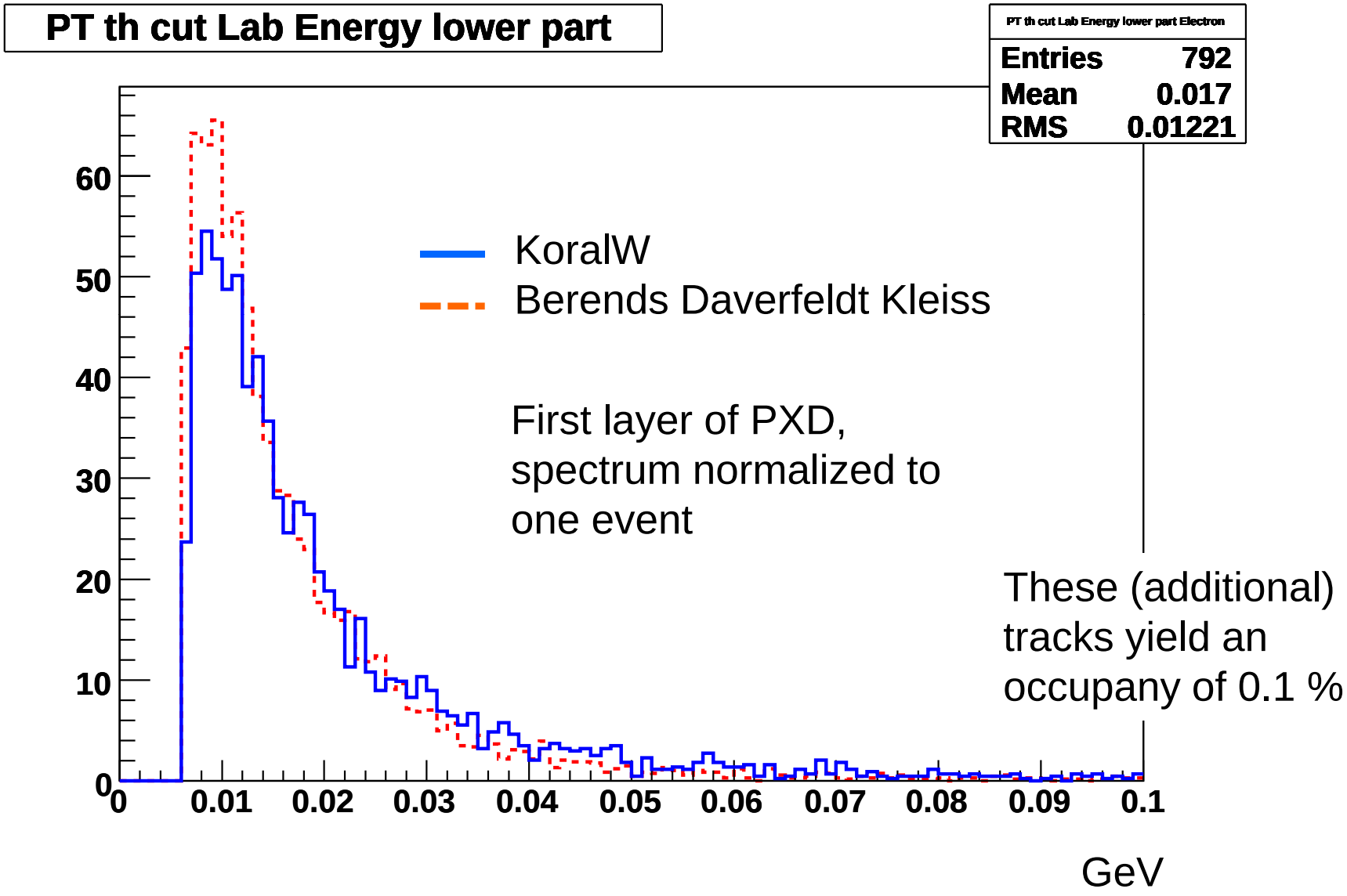
Specific Questions (cont.)

p105, 4.7.3 I guess I didn't follow all of the assumptions in the data-rate calculation. Are these two-pixel clusters just coming from MIPs produced in e+e- collisions? If so I assume it is at 8x10^35 luminosity? Right? What about backgrounds from Toushek electrons (or beam gas)? Are they included in this 1% (or 2%) background estimate?

Answer:

We assume a luminosity of 10^36 for our calculations. For the rate calculations we assume a 2% occupancy of the PXD, with a safety factor of 3. The 1% number comes for a very pessimistic assumption on the QED (mainly 2 gamma) background only. We have, unfortunately, not yet access to estimates of the machine background, which would come on top.

QED spectrum: KW and BDK



Specific Questions (cont.)

p106-108 I don't understand the division of responsibilities, as embodied by the blue lines in figure 4.25 that seem to move CDC and SVD data to the PXD higher level readout. I understand the ROI-finding will be done by the PXD team to allow removal of non-physics hits from the PXD data-stream, but has the splitting of SVD/CDC signals been agreed, tested, planned? Who is responsible for checking / understanding the integrity of this information as it used to filter PXD hits?

Answer:

We have set up a common working group for the PXD data reduction and data acquisition, with members from PXD, SVD, and DAQ. We consider the data integrity and the data reduction and acquisition as a common project. A representative from each subgroup is defined.

Specific Questions (cont.)

p112, 4.8.1 “overlaps in phi to eliminate dead areas". What about active overlap to facilitate alignment, will there by any of this?

Answer:

The overlap has been deliberately chosen to cover 8-10 pixel columns, so that a meaningful alignment can be done.

p112, 4.8.2 “thinned over active area". But the frames must run beside the active pixels (overlap in phi region) too, no?

Answer:

No, also the unthinned frame is covered with active pixels (except, of course, for the side where the switchers are located).

Specific Questions (cont.)

p123 30 x 30 micron pixels see charge in 4-5 pixels on average (so a 2 x 2 square I assume). I know the Belle ones will be larger. Have/will you do(ne) test beams with those to understand pixel cluster shapes there?

Answer:

The small-pixel test beam (TB) results are obtained with a thick sensor. For 75 micron thickness the signal cloud is much smaller. Some control is moreover possible by increasing/decreasing the bias voltage. The collection of electrons from a depleted and biased silicon wafer is well-understood. All TB measurements indeed yield results that are as expected.

Specific Questions (cont.)

Answer (cont.):

The good agreement between the digitizer model and TB results

- in cluster size and seed fraction vs. incidence angle and voltage and the eta distribution

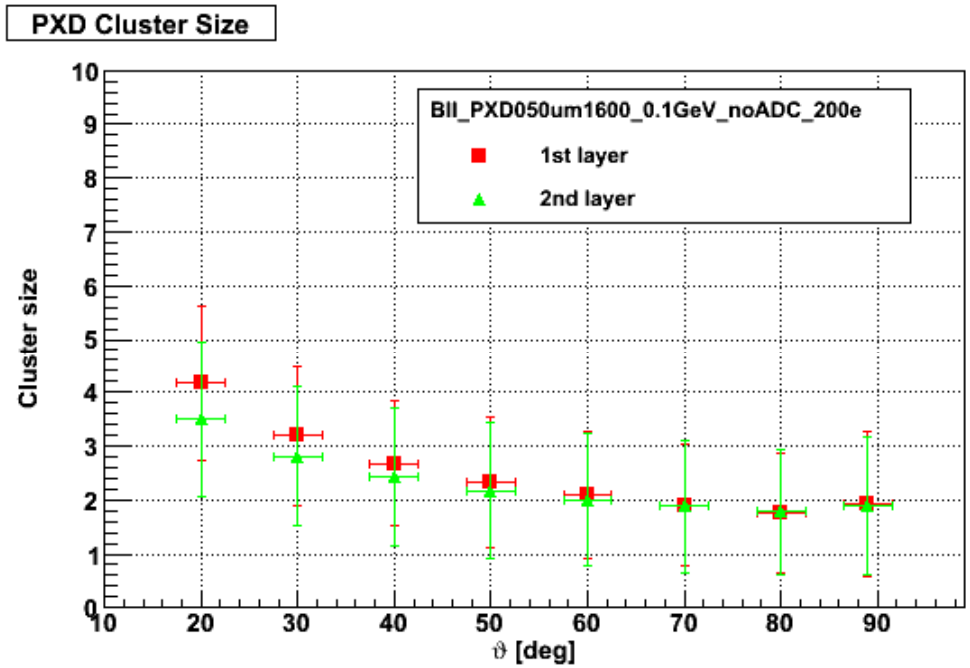
- further increases the confidence that our model of what happens inside the wafer is correct. Moreover, in the experiment charge sharing is predominantly due to the inclination of the tracks. This is modeled by pure geometry.

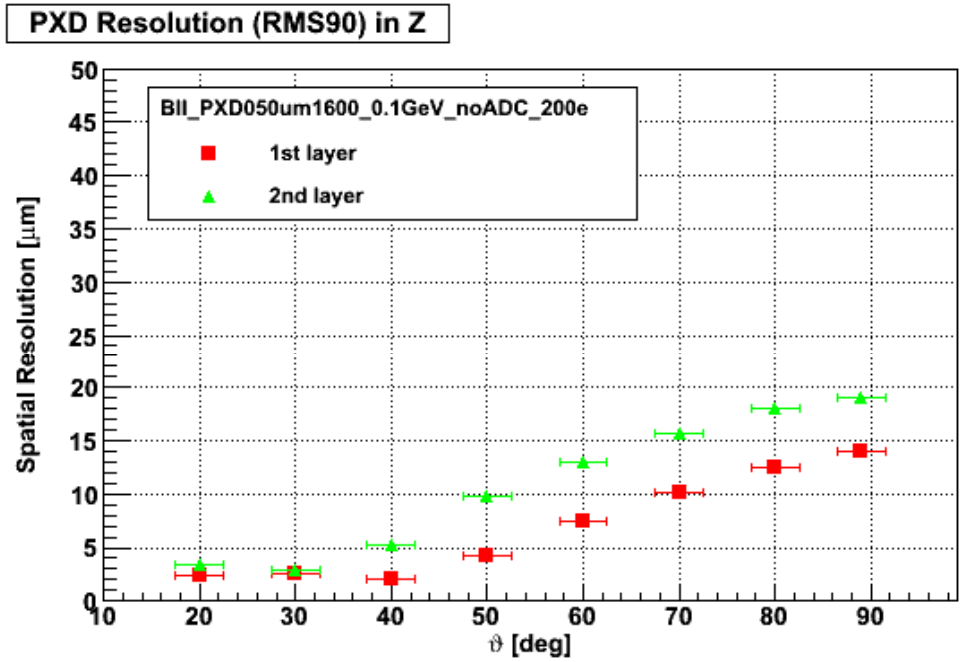
All that said: beam tests of PXD6 Belle-II design sensors will indeed be performed as soon as possible (see discussion above).

Sensor Thickness

„thinner“ sensors: low multiple scattering, low occupancy

„thicker“ sensors: larger S/N (> 20 desired), better mechanical stability, less risk



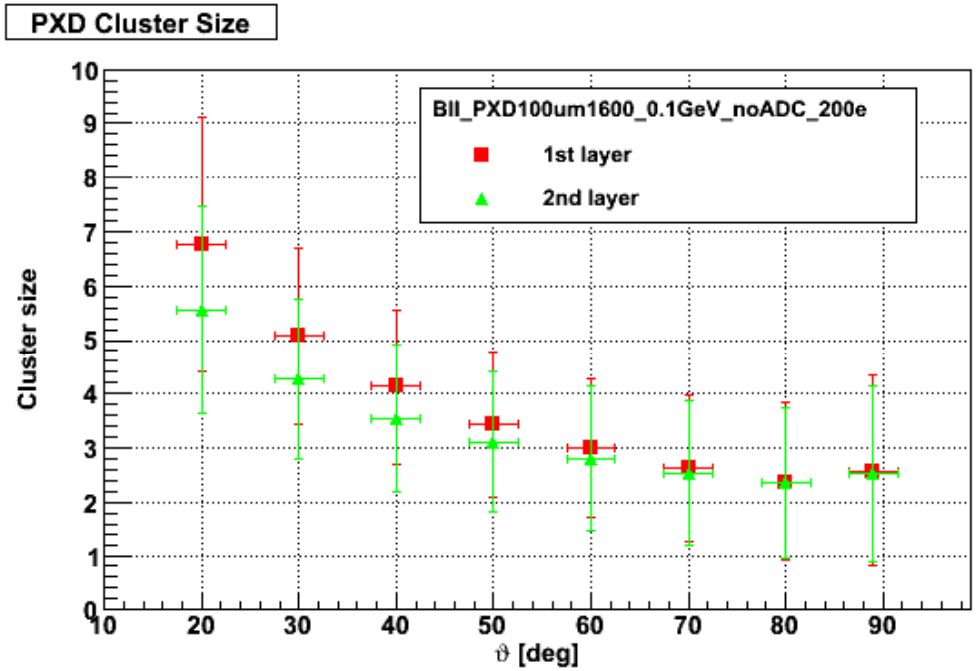


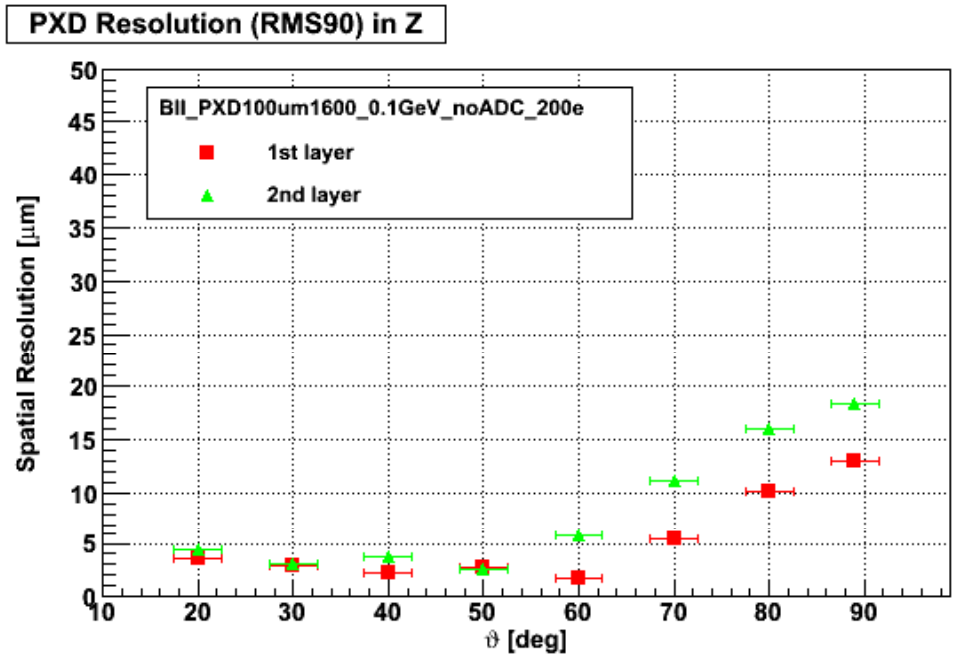
DEPFET thinned down to 50 μm

Sensor Thickness (cont.)

„thinner“ sensors: low multiple scattering, low occupancy

„thicker“ sensors: larger S/N (> 20 desired), better mechanical stability, less risk





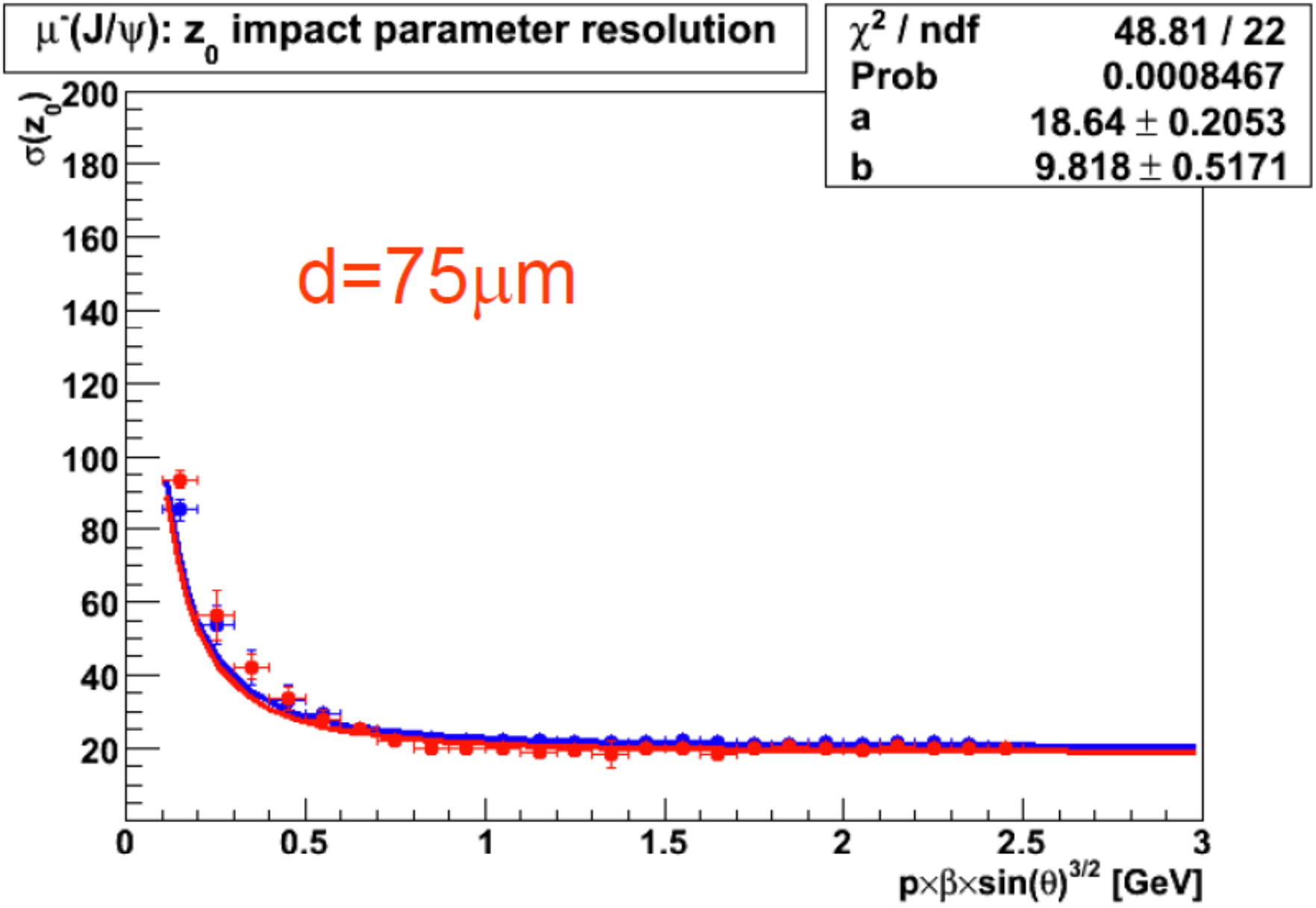
DEPFET thinned down to 100 µm

Monte Carlo calculations ongoing …

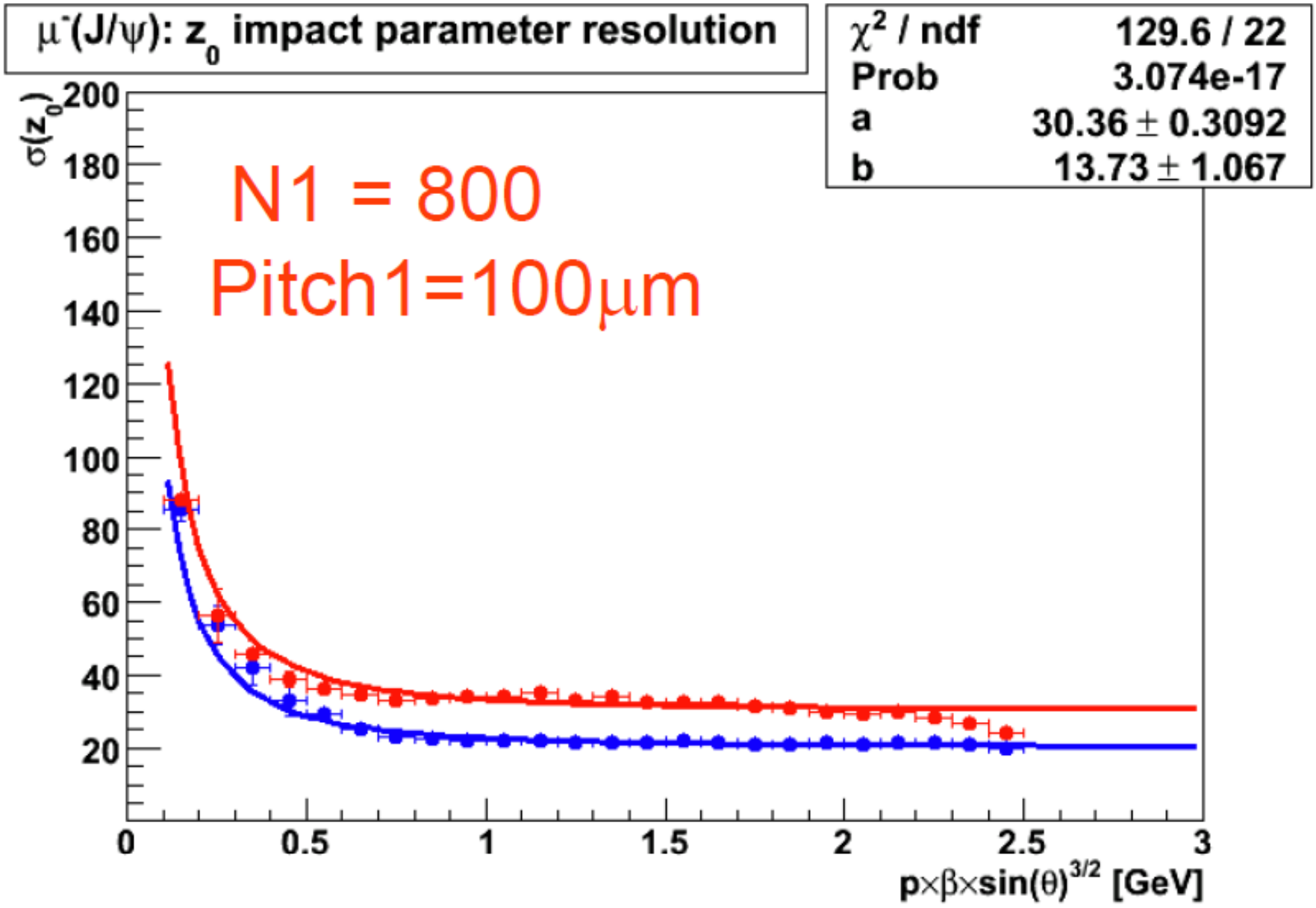
Specific Questions (cont.)

p128, 4.11.5 From the variants you conclude that 75 micron thick is no worse than 50 microns, for reasons of extra signal giving better intrinsic hit resolution winning out (or keeping up with at least) multiple scattering. If that is the case why are you still going to 50 micron thick? That must be lower yield and potentially more risking mechanically after installation etc. There is a big difference between 30-50 micron thick silicon and 75-100 micron thick, in terms of mechanical stability. Why not go with the slightly more rigid/conservative sensor thicknesses? Even the reduction from 1600 to 800 pixel rows { the most dramatic change doesn't seem like it would change the physics all that much. Instead halving the readout time would give another factor of two reduction in occupancy, no? That might be *very* important given some of the uncertainties involved in estimating the backgrounds at this stage. No?

Thickness: 75 µm vs 50 µm



Pixelsize: 800 vs 1600 pixel rows



Specific Questions (cont.)

Answer:

We have decided recently on the basis of physics performance to go for 75 µm as our new baseline.

With these simulations we have also verified that the first layer must have at least 1600 pixel rows. With only 800 rows our vertex resolution is significantly worse.

The occupancy does not change, to first order, by halving the readout time, since the pixel area is doubled. However, the resolution is strongly affected.

Specific Questions (cont.)

p132, fig 4.40 I don't understand the time line around PXD6 production and testing, final sensor design and PXD7 production. It seems PXD7 production starts (or preproduction I guess) before the final sensor design is finished. There can be good reasons for this, but I didn't see an explanation in the text.

What production yield of DEPFET is assumed in the schedule? On what performance criteria is assumed in the production yield? What experience do you have with such criteria/yield assumptions?

Specific Questions (cont.)

Answer:

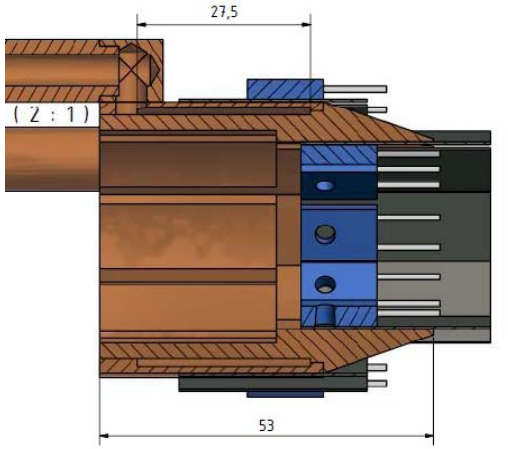
We have laid out the production schedule above. We are sorry again for the misleading term “preproduction”.

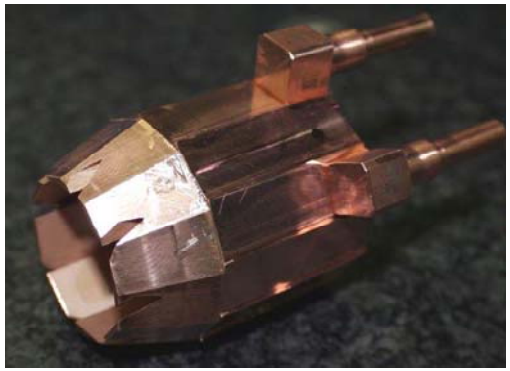
Concerning the production yields etc, we have answered above: The Semiconductor Laboratory (HLL) of the Max-Planck-Society has an excellent record since many years of producing high-quality sensors for various fields of fundamental science, such as for particle and astrophysics, and recently also for photon science.

End of Questions

Backup

Cooling (Mockup)



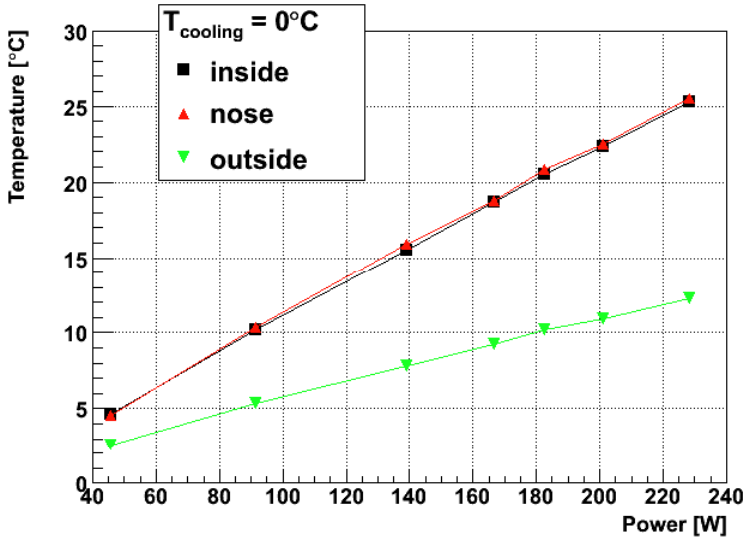


Test with copper block

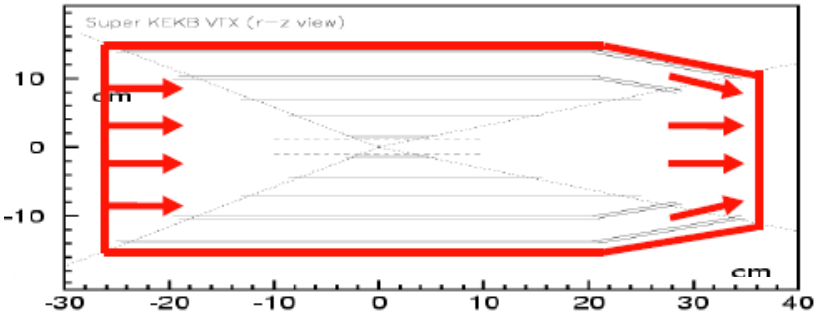
coolant; FC-77

Large ΔT between coolant and block surface
Even larger for inner modules (20º)

(Karlsruhe)



Air cooling: common cold volume with SVD,
needs to be engineered,
thermal insulation from CDC

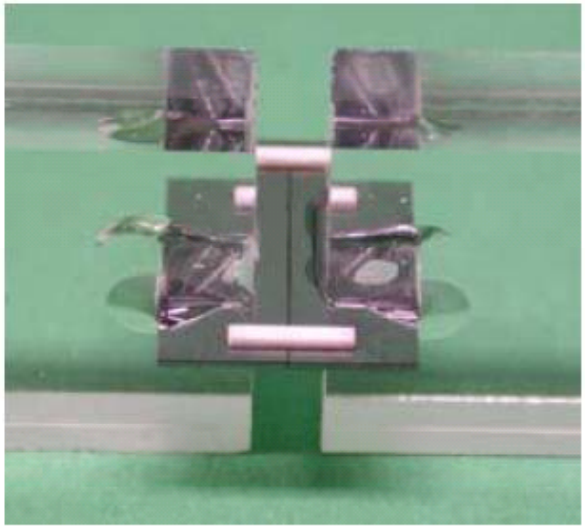


Various Tests of Glueing Schemes

First tests of the module joint glueing were carried out:

- tensile strength
- bowing strength

(MPI)



Both tests were carried out with different configurations:

1. plain, 450 μm silicon (no glue)
2. 450 μm silicon, front face glueing
3. as 2, but with two additional Al_2O_3 pieces as reinforcement glued on the silicon

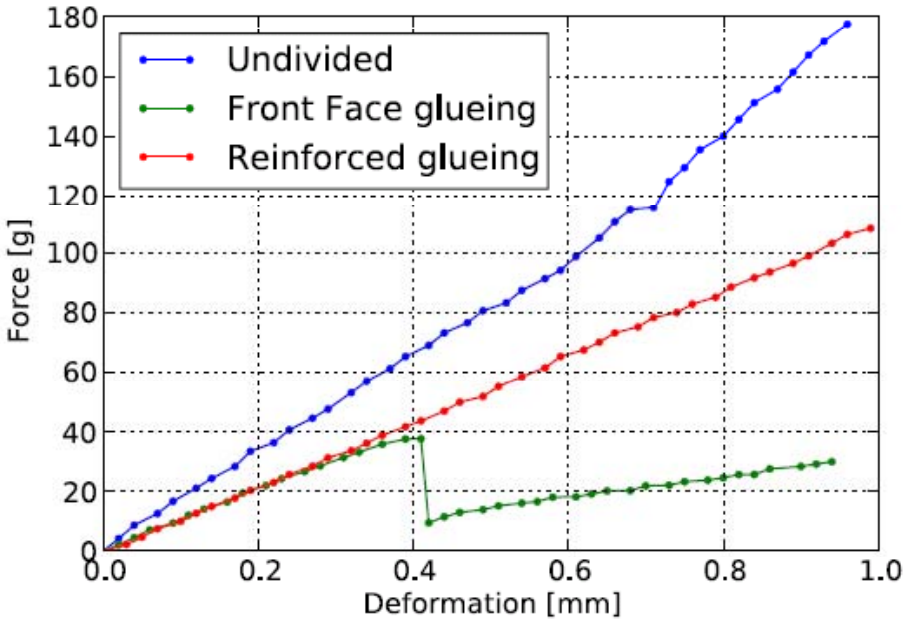
Things to keep in mind:

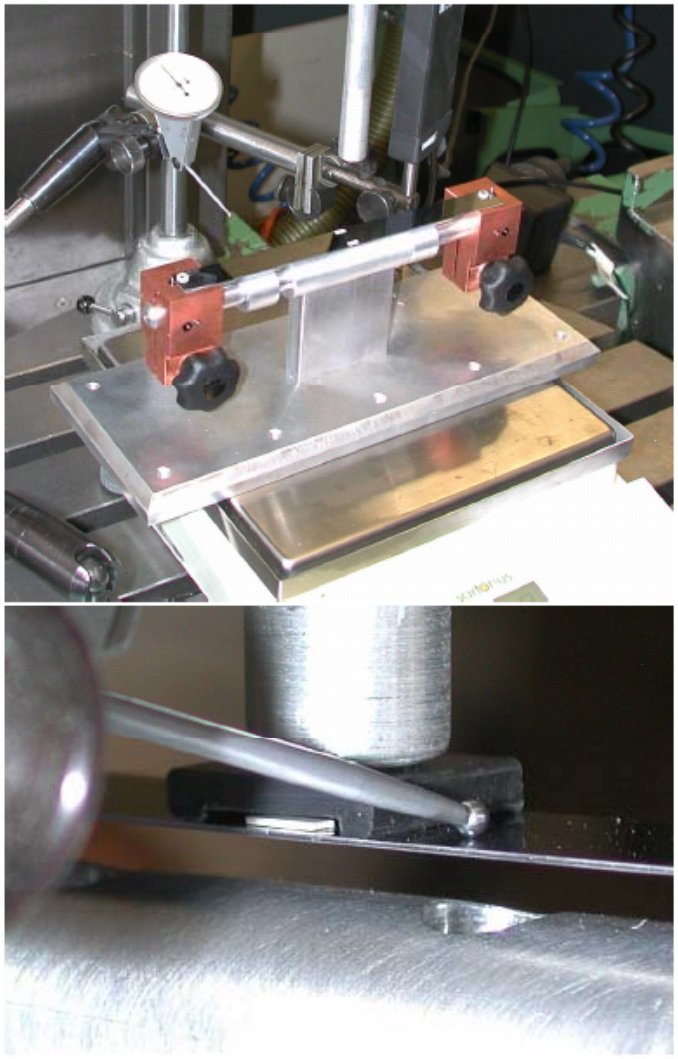
- reinforcement different: glued on top of Si, larger dimensions
- modules not thinned down

Details of Bowing Stress Tests

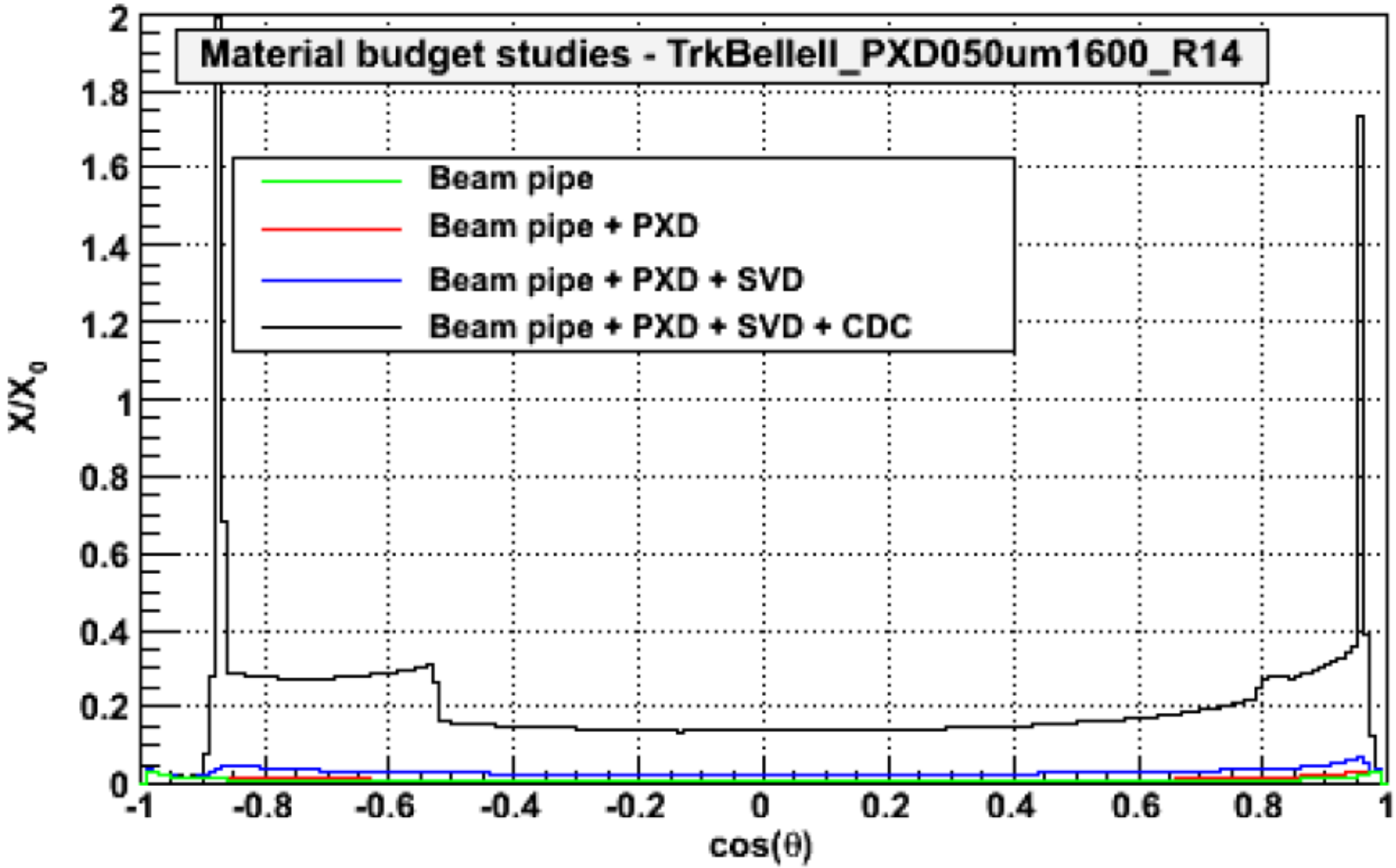
(MPI)

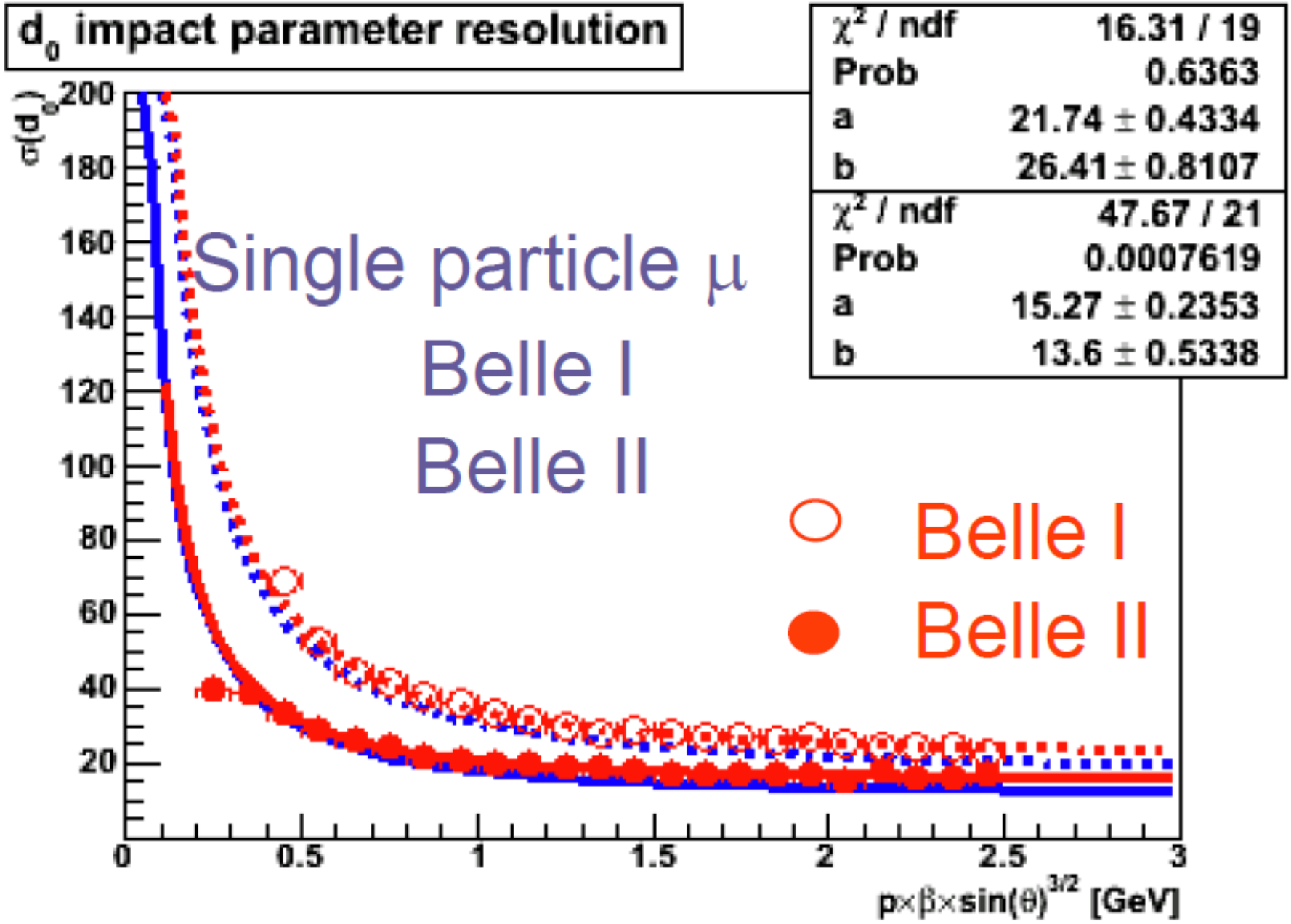
1. undivided, inner layer dummy broke at deformation of 1.445 mm (Force of 316 g)
2. front face glued outer layer module:
   - glueing broke at 0.4 mm deformation (37.7 g)
   - half modules remained in good order
   - tested to 1 mm deformation ($\sim$ 30 g)
3. reinforced glueing successfully tested up to 1 mm deformation (108 g)





… next round with thinned dummies


Material budget studies - TrkBelleII_PXD050um1600_R14
Beam pipe
Beam pipe + PXD
Beam pipe + PXD + SVD
Beam pipe + PXD + SVD + CDC
X/X0
cos(θ)
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-1
-0.8
-0.6
-0.4
-0.2
0
0.2
0.4
0.6
0.8
1


d0 impact parameter resolution
χ2 / ndf 16.31 / 19
Prob 0.6363
a 21.74 ± 0.4334
b 26.41 ± 0.8107
χ2 / ndf 47.67 / 21
Prob 0.0007619
a 15.27 ± 0.2353
b 13.6 ± 0.5338
σ(d0) [μm]
Single particle μ
Belle I
Belle II
Belle I
Belle II
p×β×sin(θ)3/2 [GeV]

Schedule and Near Future Milestones

Phases of the PXD@Belle II Project

Design	Prototypes	Tests	Production	Integration.	Comm.
2009 +	2010.9	2010.10-	2011.5 – 2012.6	-2013.3	-2013.9

Workpackages, reponsibilities, overall schedules are defined

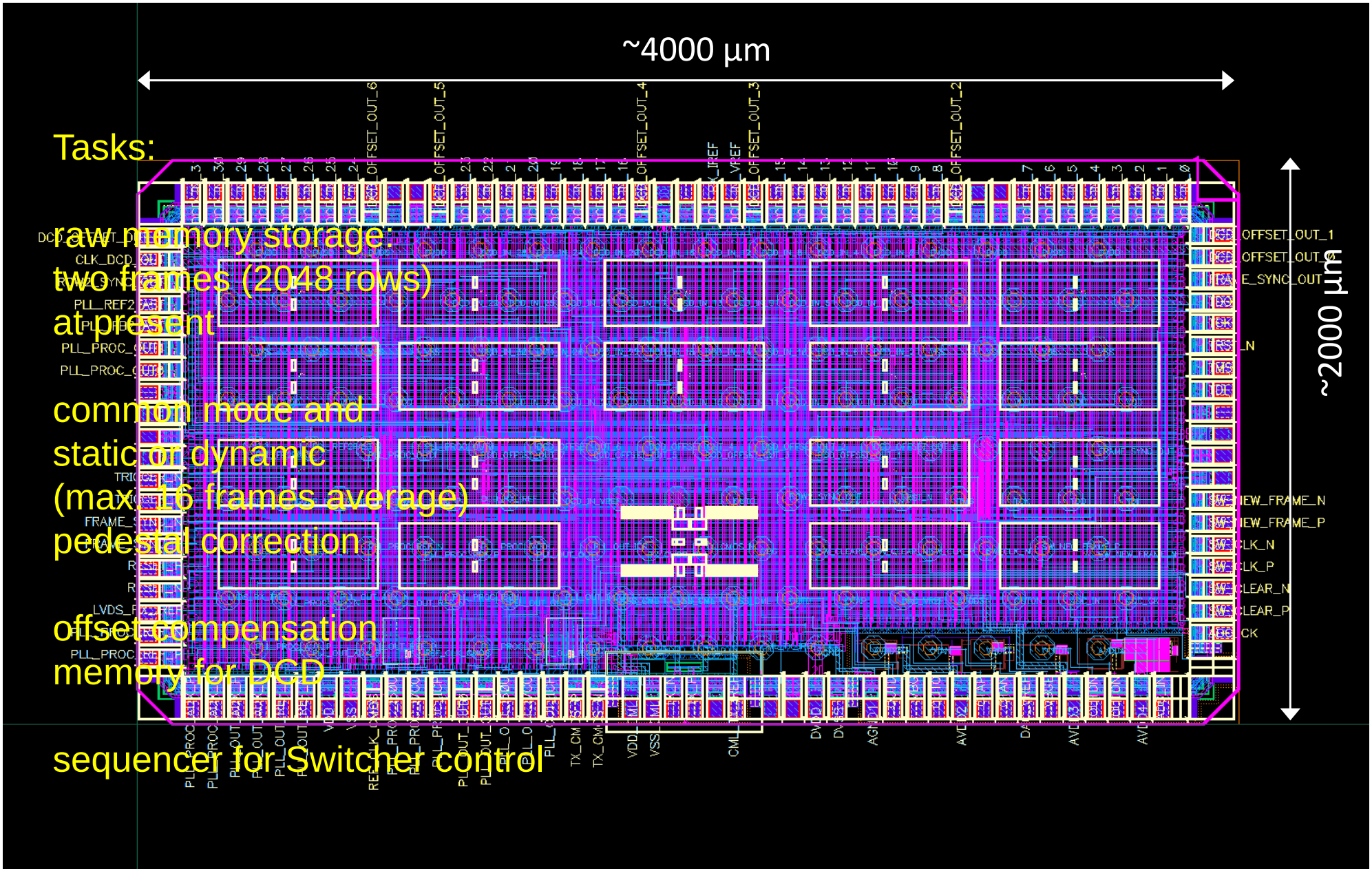
2010: We enter now a phase where concrete planning is mandatory:

- define MOST technical details;
- make technological decisions
- and establish firm schedules and procedures

→ Immediate milestones:

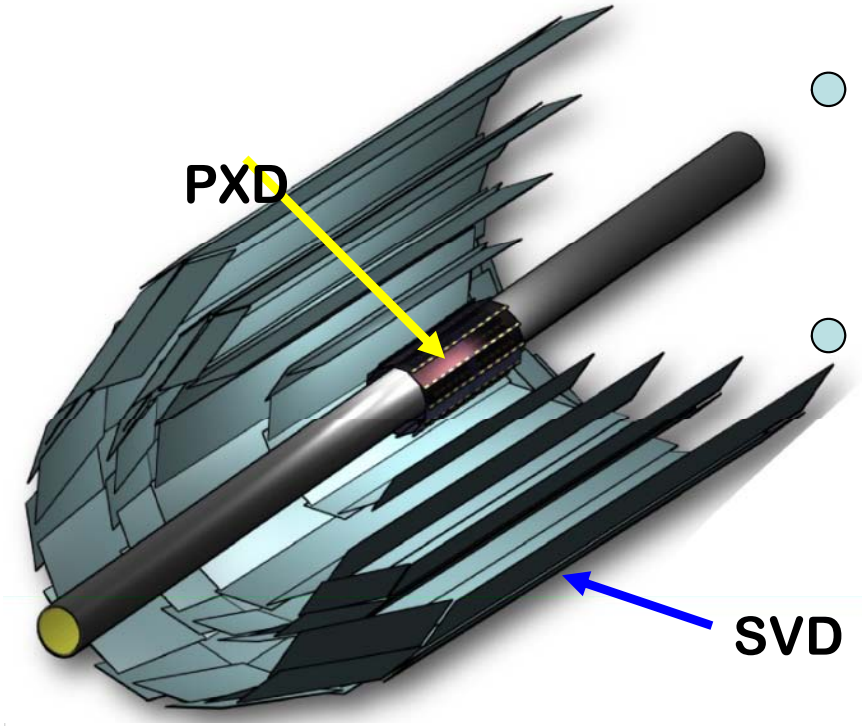
- Machine parameters (beam pipe) defined soon (when ?)
- Techncial Design Report (delivered by 2010.3)

Status of DHP



Expected Performance with PXD

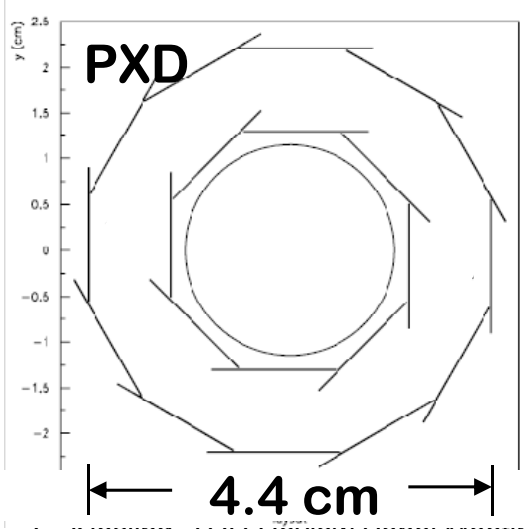
Nano beam option: 1 cm radius of beam pipe



„PXD“

- 2 layer Si pixel detector (DEPFET technology) monolithic sensor
  (R = 1.4, 2.2 cm)
  thickness 50 µm (!), pixel size ~50 x 50 µm²
- 4 layer Si strip detector (DSSD) „SVD“
  (R = 3.8, 8.0, 11.5, 14.0 cm)

Significant improvement in z-vertex resolution

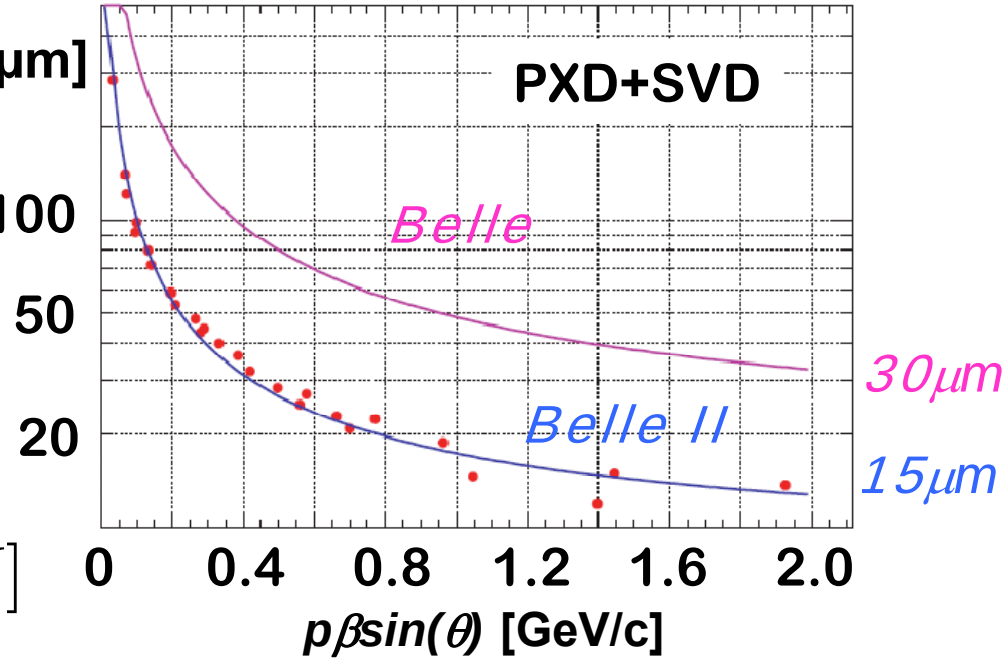


$$\sigma = a + \frac{b}{p\beta \sin^{5/2}\theta}$$

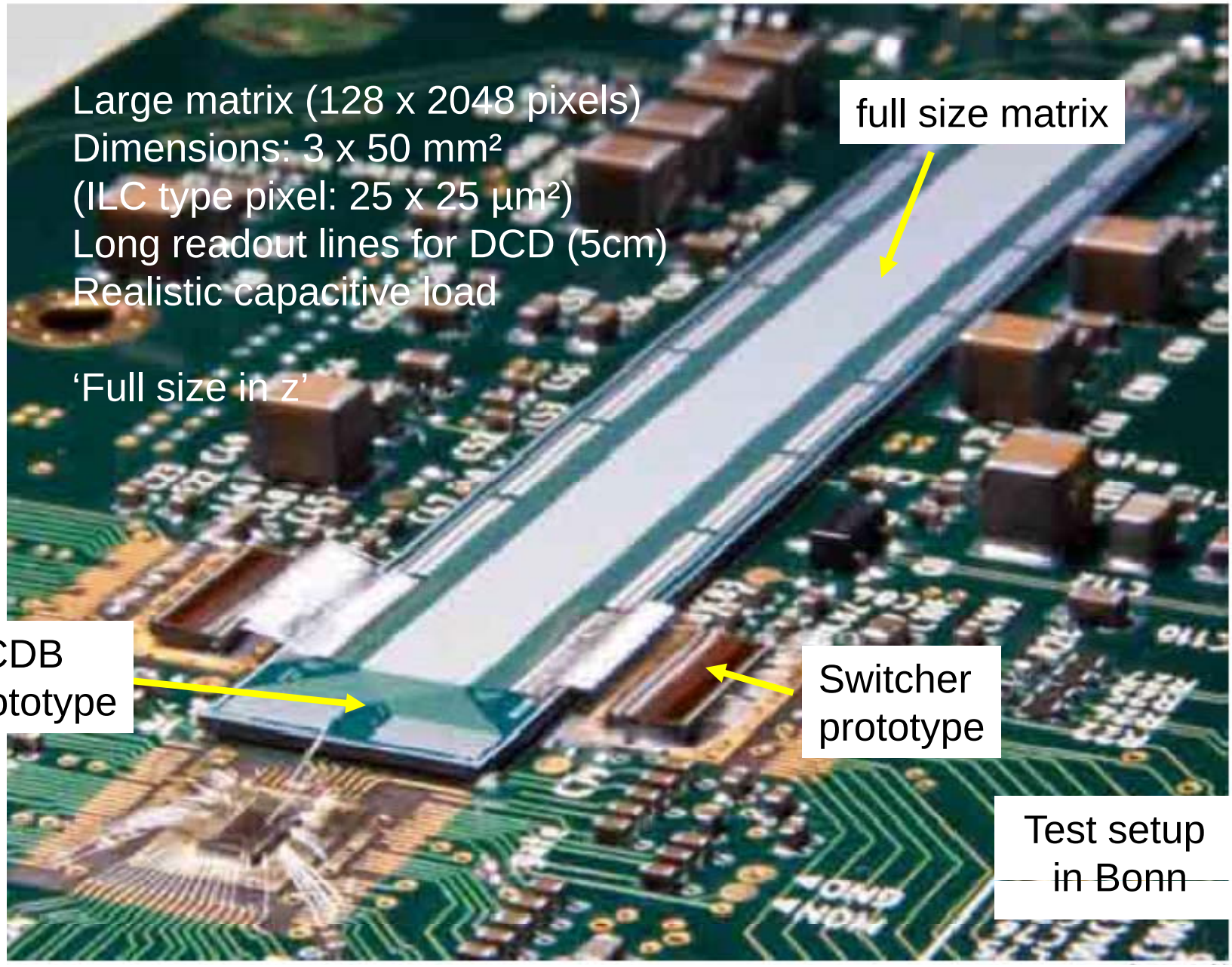
Belle II:

$$a = 8.5\,[\mu m]$$

$$b = 9.6\,[\mu m\,\mathrm{GeV}]$$



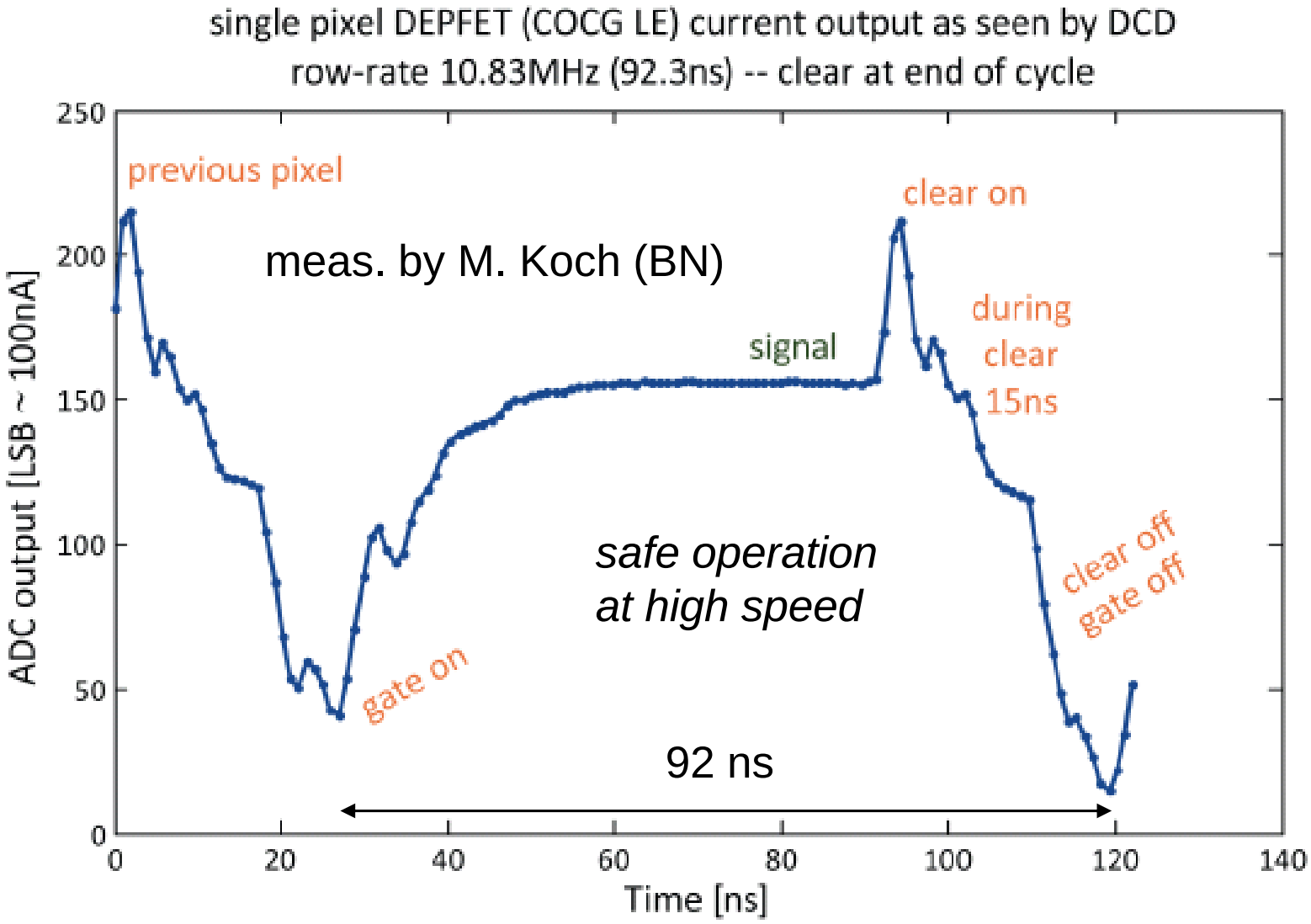
Tests on Readout Speed



Tests on Readout Speed (cont.)

single sampling with common mode rejection

DCDB prepared for doing single and double correlated sampling



Full speed readout demonstrated