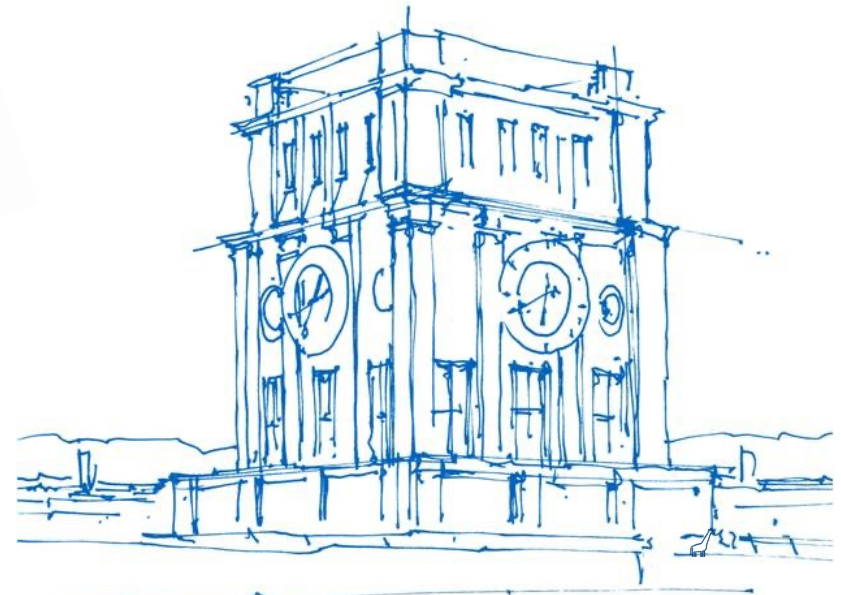
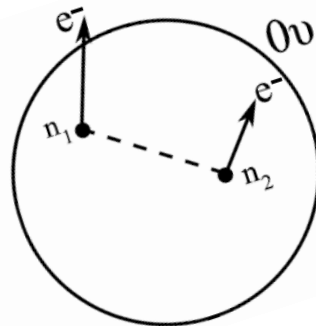
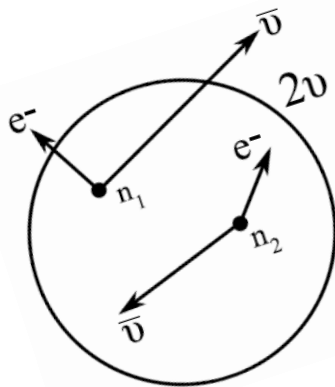


# ASIC based readout electronics for high-purity Germanium detectors in LEGEND 1000

DPG Heidelberg 2022

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24/03/2022



Uhrenturm der TUM



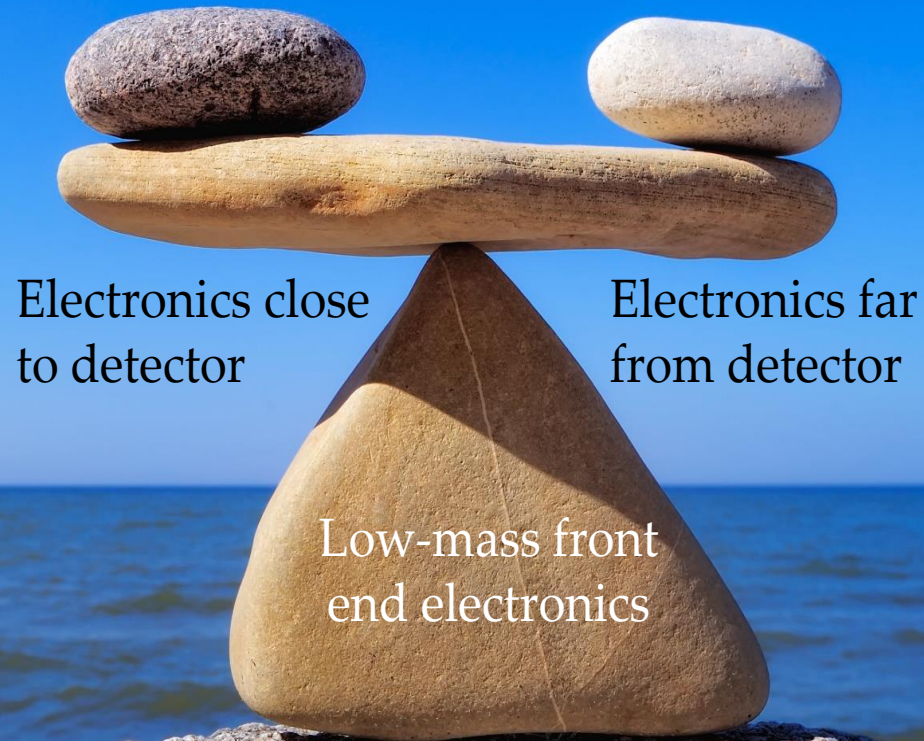
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1. Motivation – Signal Readout electronics in LEGEND
2. Charge Sensitive Amplifier (CSA) in LEGEND
3. LEGEND-1000 Berkeley ASIC
4. Summary and Outlook

# Motivation – Readout Electronics for $0\nu\beta\beta$ Experiments

Low electronic noise

Low background

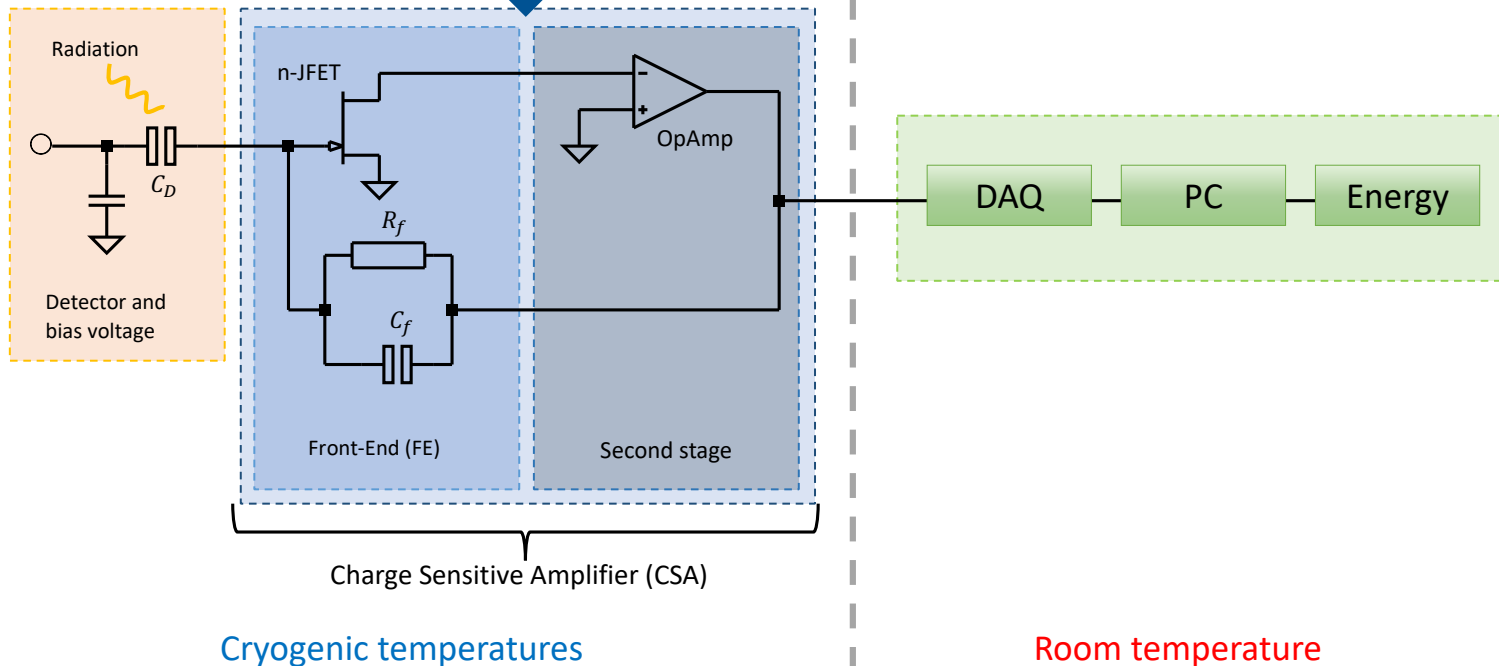


## LEGEND-200



### Readout chain

- HPGe detector with HV reverse bias voltage
- $p^+$  contact connected to Charge Sensitive Amplifier (CSA), typically:
  - First stage close to the detector
  - Second stage further away



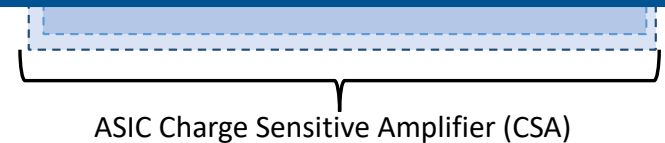
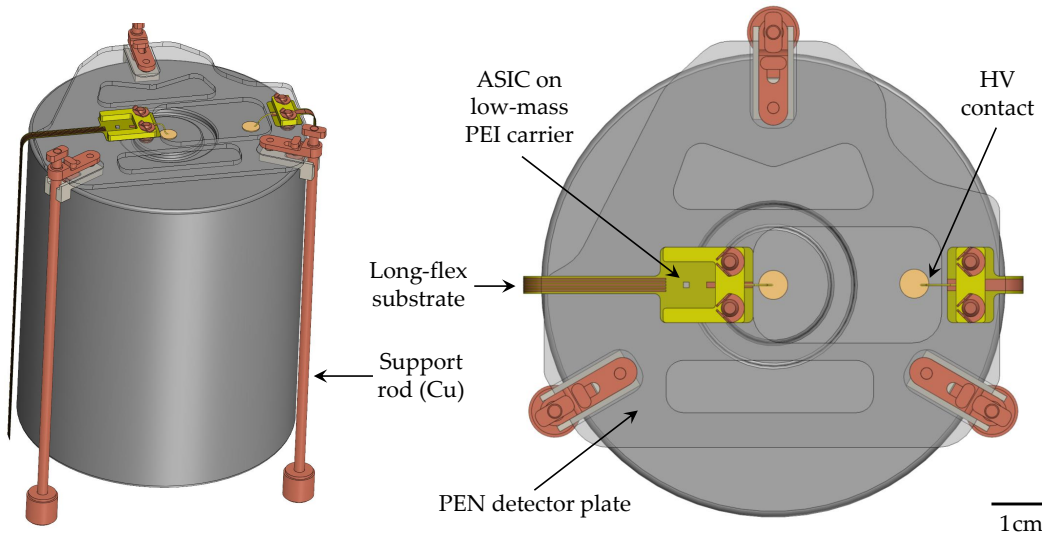
## LEGEND-1000 Electronics

### Application-Specific Integrated Circuit (ASIC) technology

- Combine all CSA components into low-mass chip → ASIC technology
- Enables excellent noise performance

## CSA Requirements for LEGEND-1000

- **Very low electronic noise**
- Large dynamic range (up to 10 MeV) and high linearity
- Important constraint radiopurity (ASIC + everything supporting the chip!)
- **Continuous (exponential) reset, decay time  $\geq \mathcal{O}(100\mu s)$**
- Fast rise times:  $\mathcal{O}(10\text{ ns})$ , bandwidth 50MHz



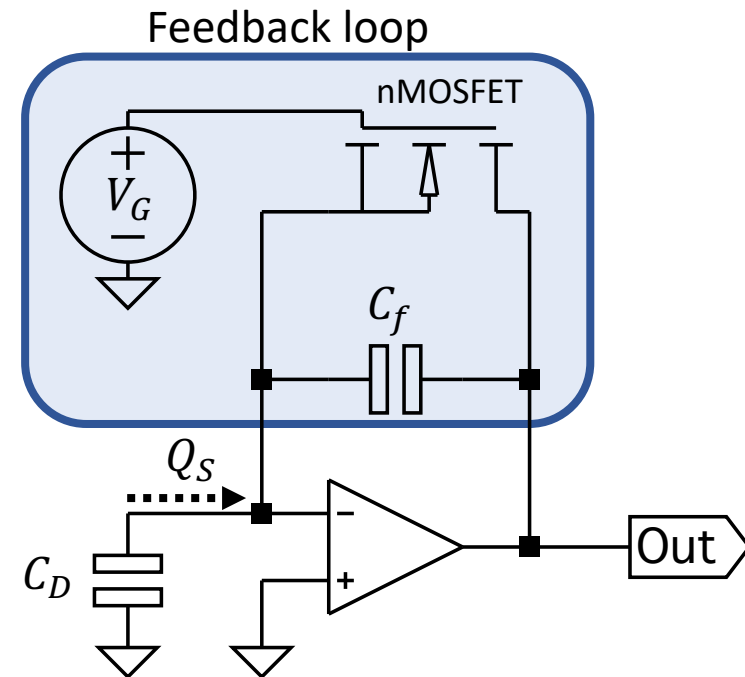
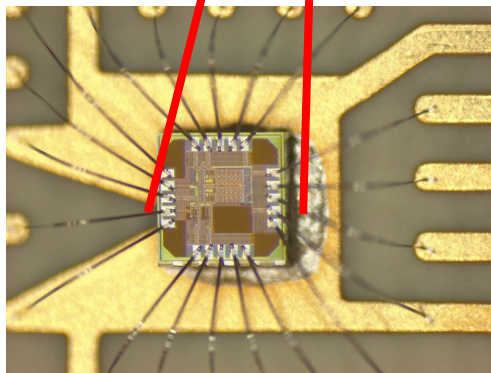
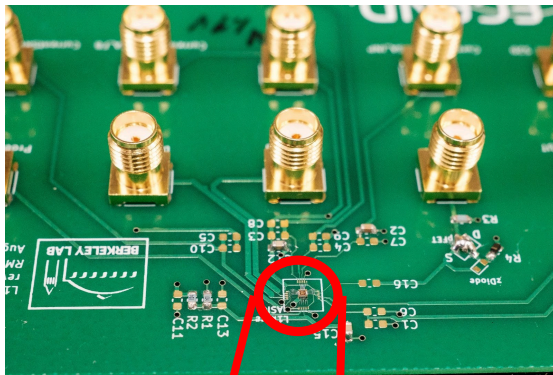
Cryogenic temperatures

# The L1k Berkeley ASIC (LBNL ASIC)

## L1k preliminary ASIC

ASIC built by Berkeley lab in 2020 and tested @ TUM

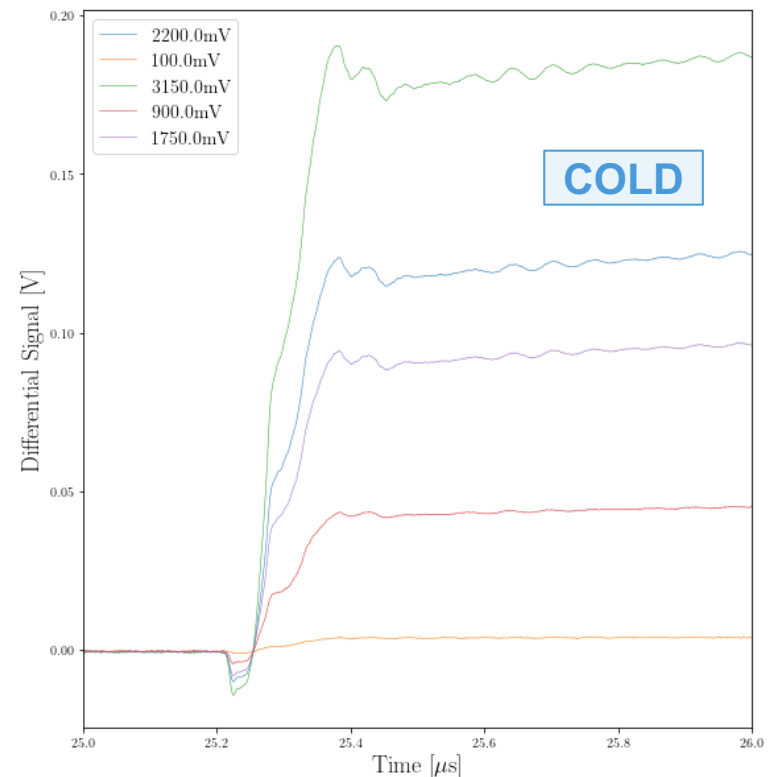
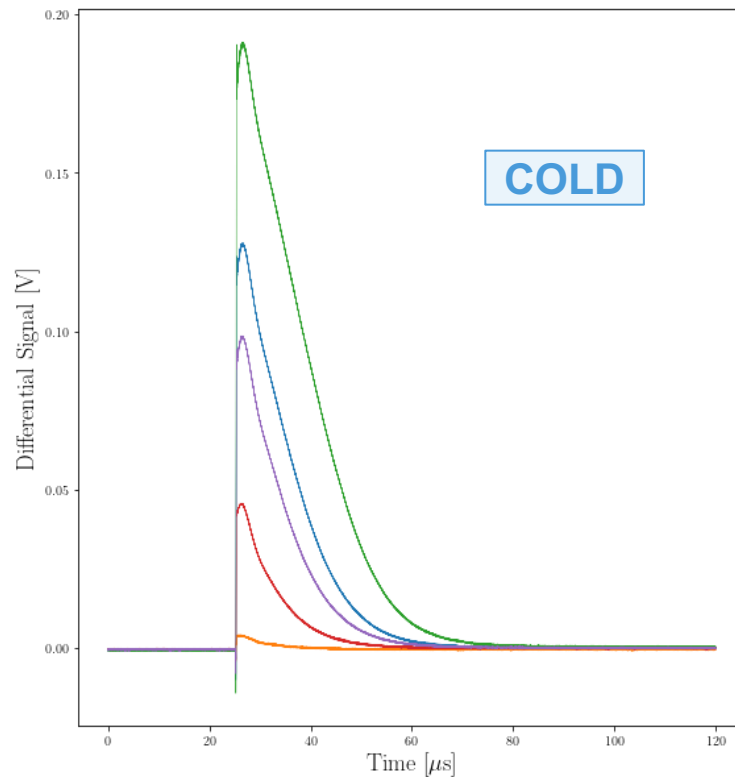
- Internal, continuous reset with semiconductor technology
- Differential output
- Detector load:  $\sim 1 - 5 \text{ pF}$
- $C_F = 500 \text{ fF}$
- Feedback loop: effectively a capacitor and a transistor (*n-MOSFET*) in parallel



# The L1k Berkeley ASIC (LBNL ASIC)

## L1k preliminary ASIC

- Two different regions in the decay tail
  - “Linear” region in the beginning of the tail
  - “Exponential” region in the end of the tail
- Good linearity
- Cold and warm almost similar
- ➔ Under- and overshoot in the rise unclear

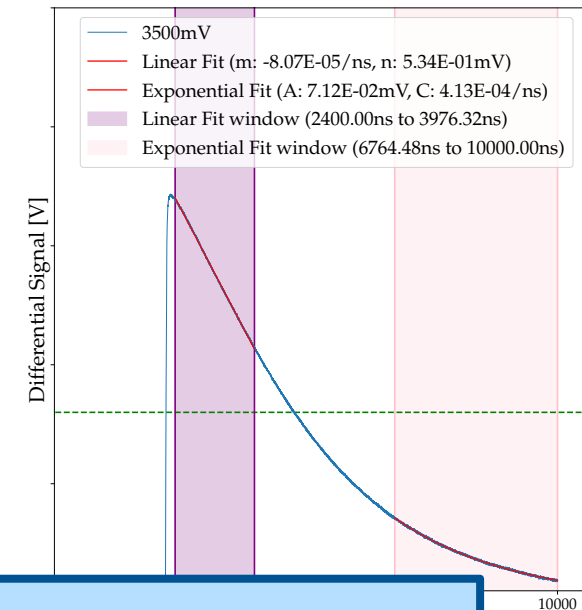
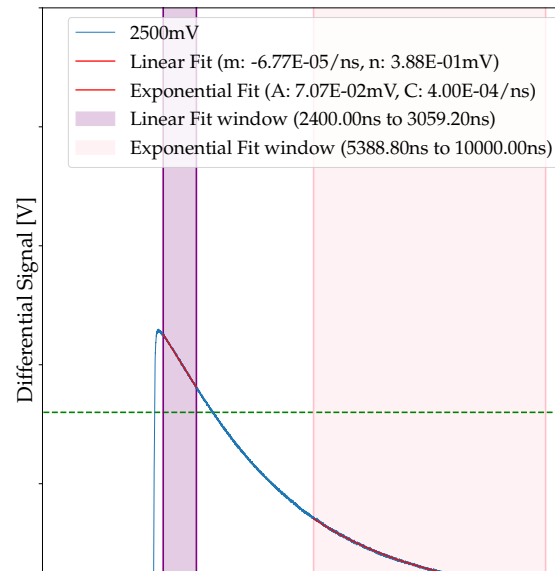
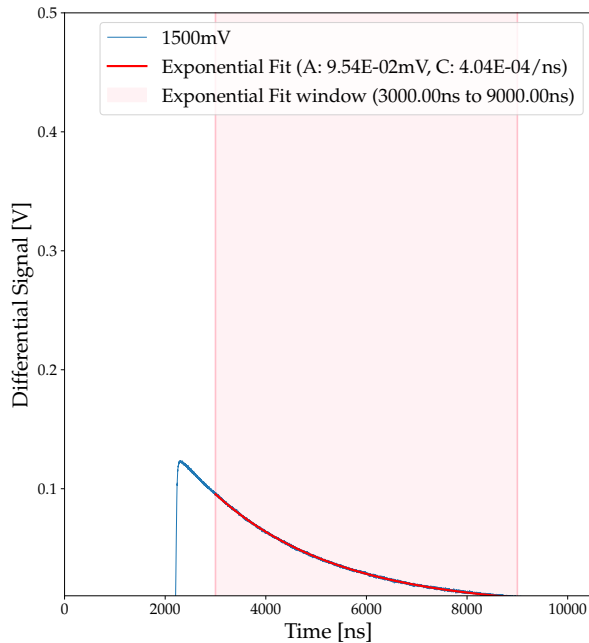
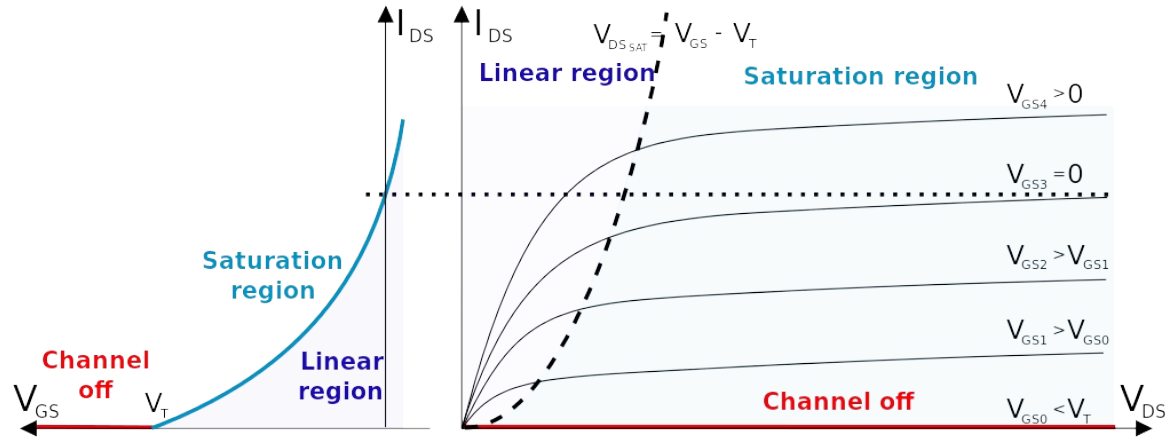
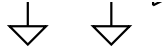


# The L1k Berkeley ASIC (LBNL ASIC)

Feedback loop

“Saturated region” ( $V_{DS} > V_{sat}$ )

- $i_D \approx \text{const}$   
 $\Rightarrow$  “ $R_{equiv.}$ ”  $\approx k \cdot V_{DS}$
- $h(t) \approx m \cdot t + n$



## Problems:

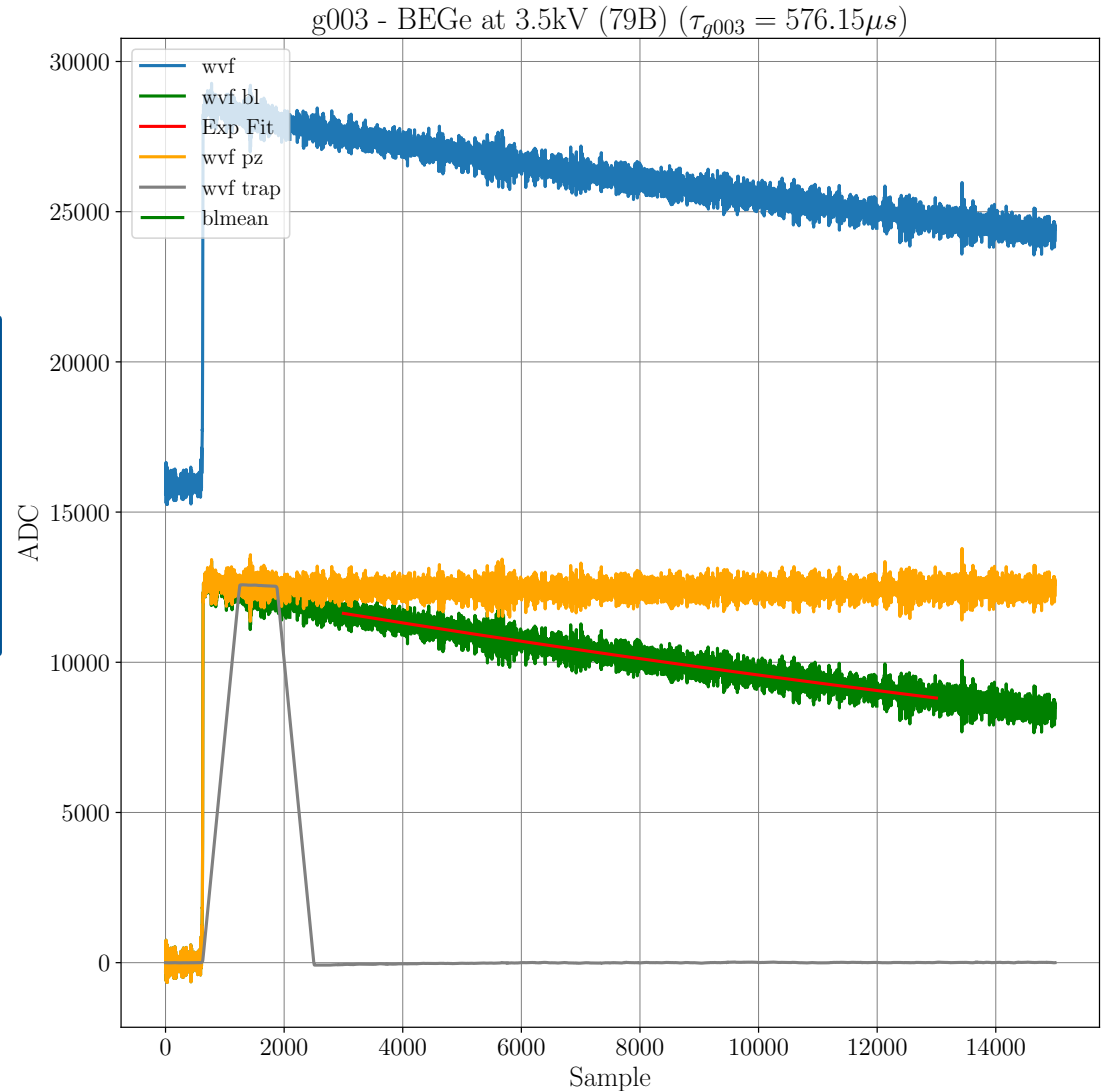
- Regions in the *beginning*, *between* and *end* of the tail?
- Pulse shape is energy dependent (!)



## LEGEND DSP

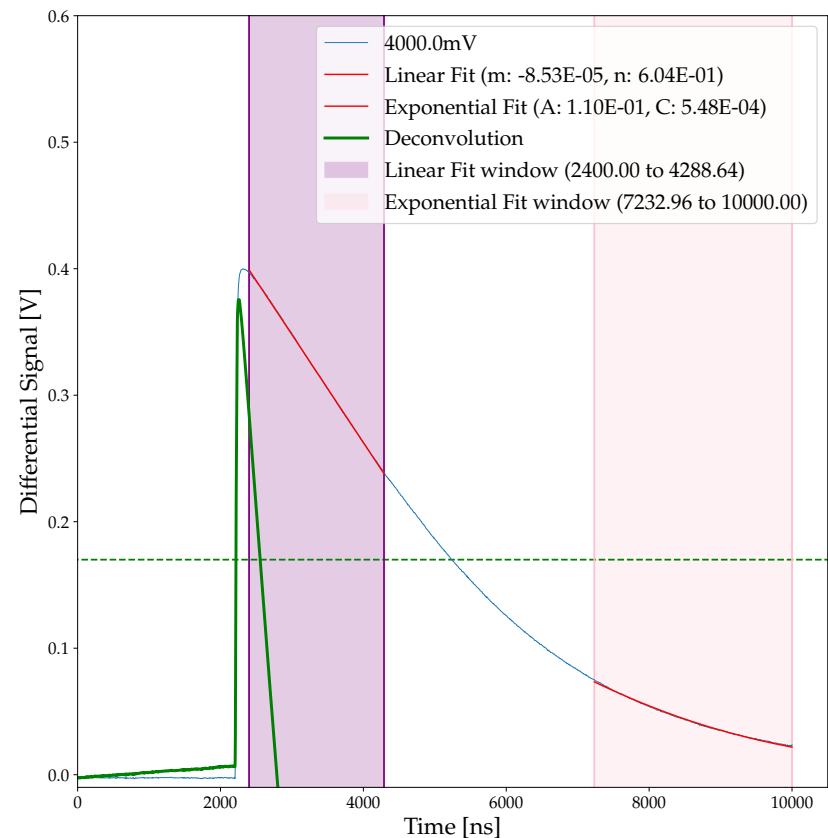
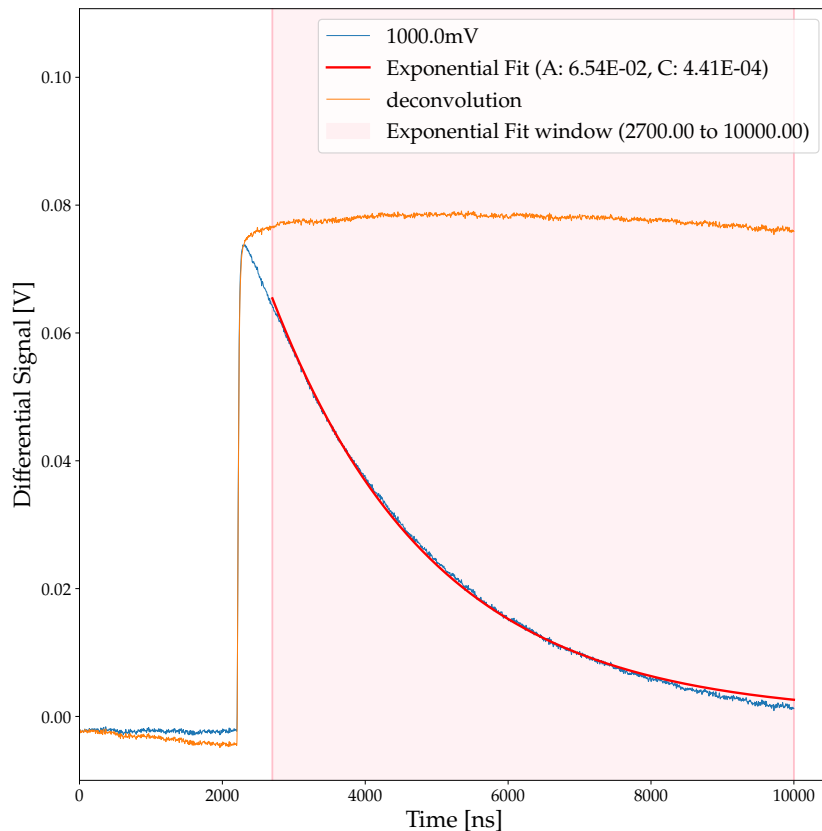
Most important steps for raw data

- Baseline subtraction
- Exponential fit
- Deconvolution
- Trapezoidal filtering



## L1k preliminary ASIC – Deconvolution

- No full analytical  $h(t)$  for the MOSFET feedback of the ASIC
  - ➡ every energy  $\Rightarrow$  different shape
  - ➡ higher rates: circuit not fully discharged  $\Rightarrow$  different shape
  - ➡ For pulses only in the "linear" region  $\Rightarrow$  model also not precise enough



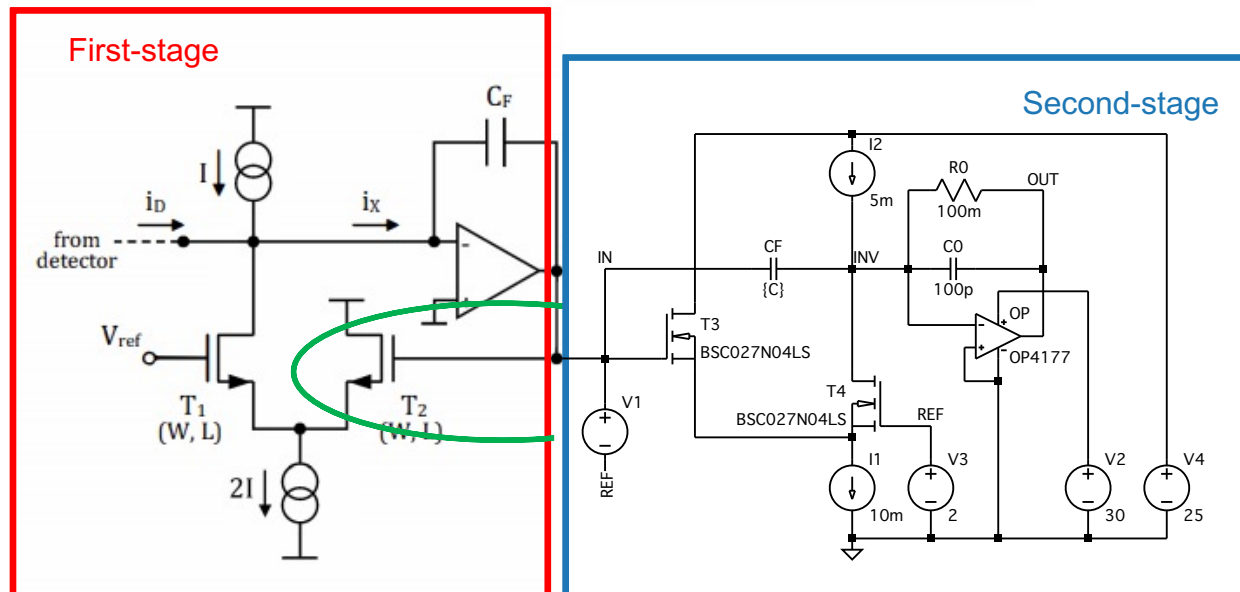
# The L1k Berkeley ASIC (LBNL ASIC)

## L1k preliminary ASIC – What can be done?

- Current ASIC setup **NOT** suitable for DSP
- One possible approach:

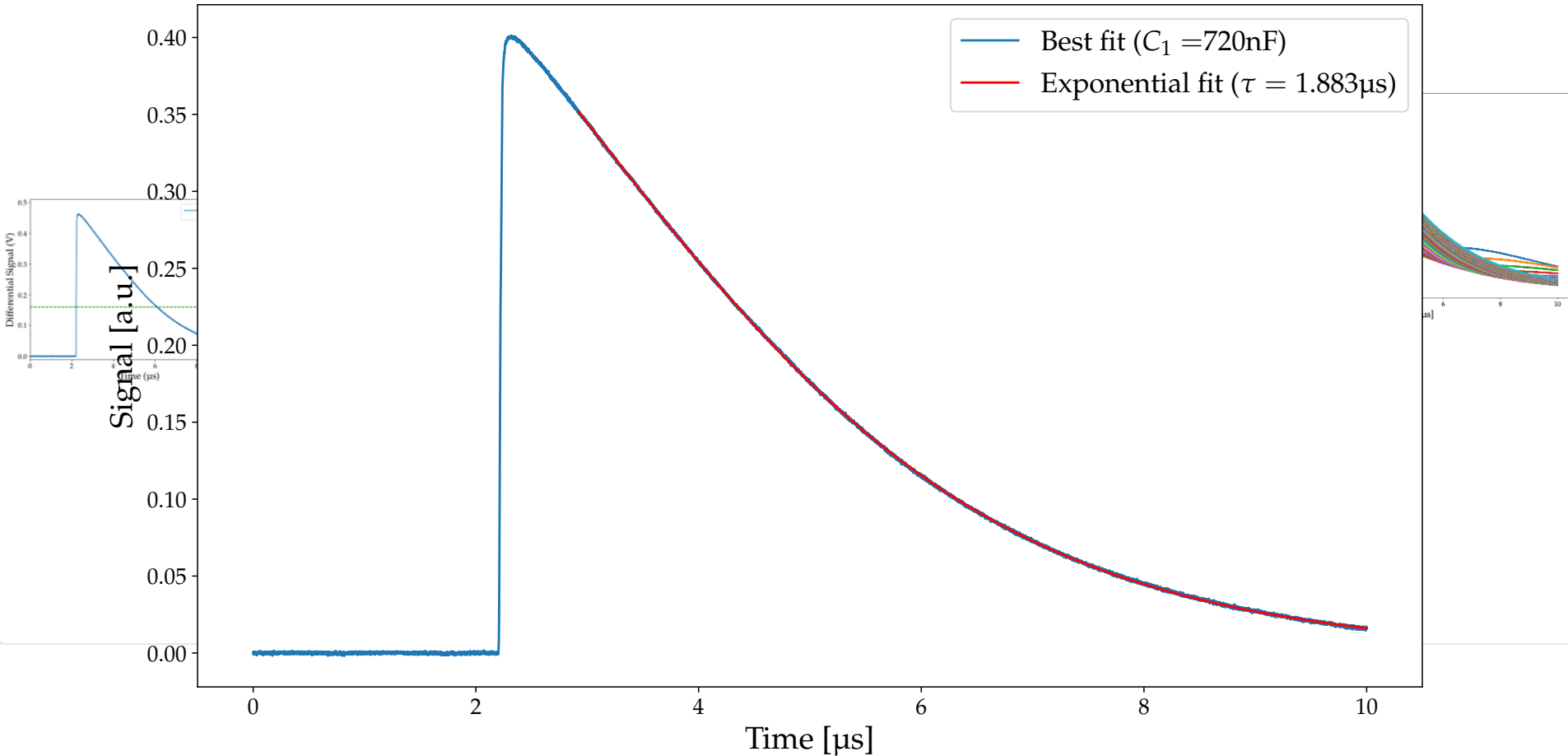
*Second stage circuit* according to Pullia et.al. Paper (DOI: [10.1109/NSSMIC.2012.6551066](https://doi.org/10.1109/NSSMIC.2012.6551066) )

- On-chip *second-stage circuits* to cancel "non-linear behavior" by **coupling** a second MOSFET to the **first stage circuit**
- Tested with LTSpice simulation for *second-stage circuit* and real data for the **first stage circuit**



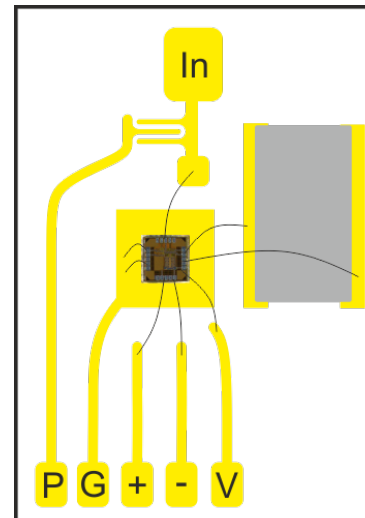
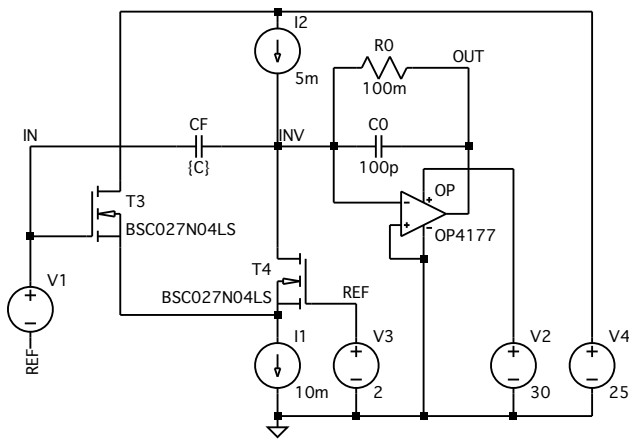
# The L1k Berkeley ASIC (LBNL ASIC)

## L1k preliminary ASIC – Second stage circuit



## L1k ASIC - Outlook

- What comes next?
    - Collaboration with *LBNL*
    - Collaboration with *Politecnico di Milano* (Prof. Carlo Fiorini) → **TUM ASIC**
      - New design with second-stage circuit approach or/and
      - New design with external aGe resistor
- ➔ Most important: Evaluation of physics performance in LAr with ICPC



**Thanks for the  
attention!**

# BACKUP

# L1k ASIC – Summary Table

	XGLab	LBNL	Future TUM ASIC
<b>External components</b>	<b>Too many</b>	<b>Only one supply voltage</b> (but filter capacitor needed!)	<b>Low drop-out regulator</b> <b>Clean external capacitors</b>
<b>Reset mode</b>	<b>Pulsed reset</b>	<b>Continuous reset</b> (but non-uniform waveforms)	<ul style="list-style-type: none"><li>• <b>Second stage</b></li><li>• <b>Int. high-ohm feedback</b></li><li>• <b>External resistor</b></li></ul>
<b>Suitable for long cables</b>	<b>no</b>	<b>yes</b>	<b>yes</b>
<b>Detector capacitance</b>	<b>Only up to 3 pF</b>	<b>Up to 5 pF</b>	<b>Up to 10 pF</b>

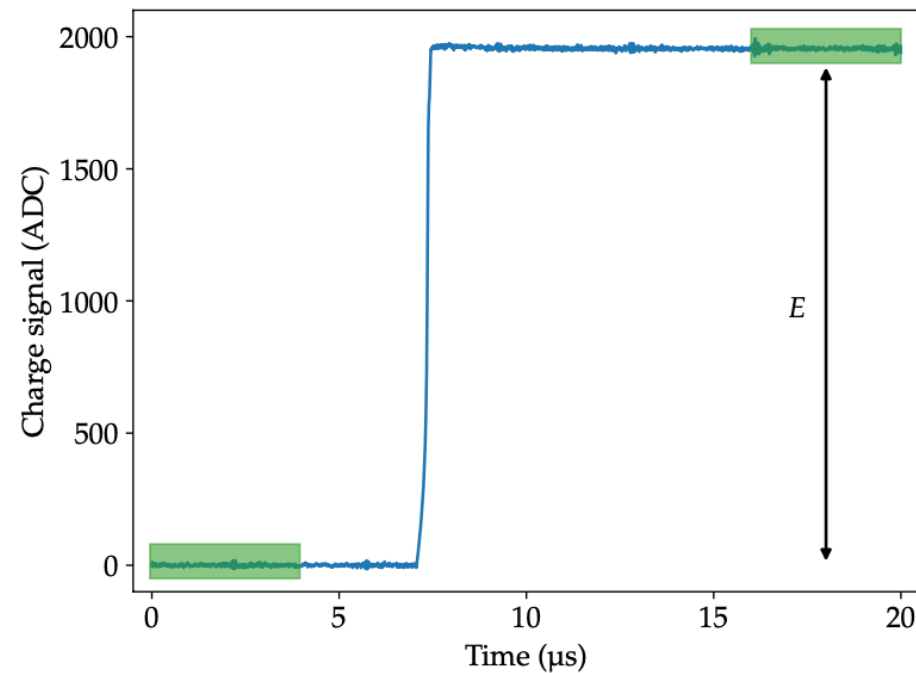


## CSA Requirements for LEGEND

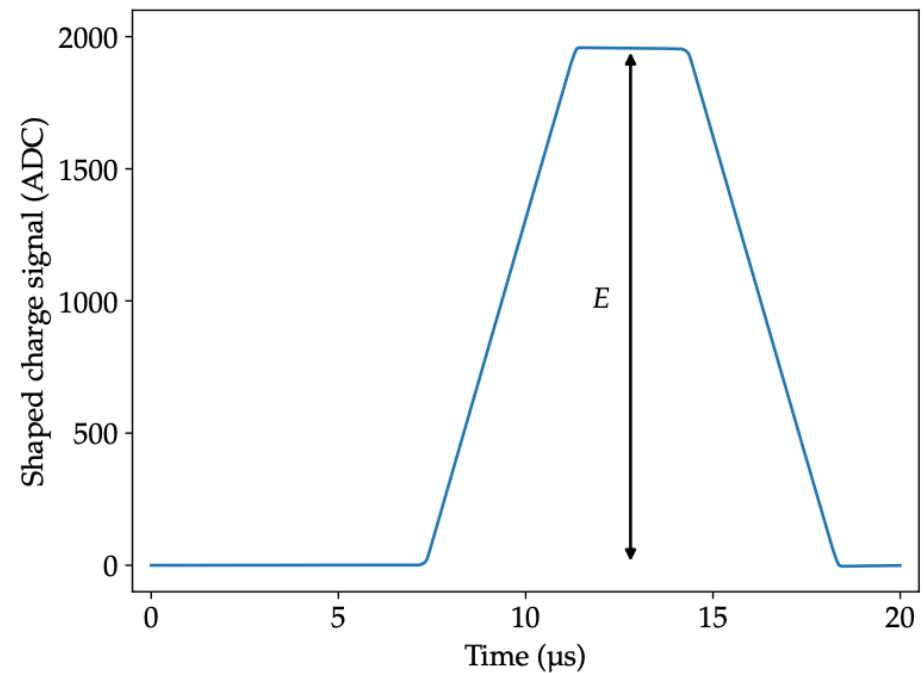
- Very low electronic noise:  $< 1$  keV FWHM pulser  $\approx 10e^-$  RMS
- Large dynamic range (up to 10 MeV) and high linearity
- Primary constraint  $\rightarrow$  radiopurity (ASIC + everything supporting the chip!)
  - Small volume ( $\lesssim 0.4\text{mm}^3$ ), bare die, wire-bondable
  - No external components: single power supply, no (close) bypass capacitors, on-chip LDO
  - Ideally no external feedback components
- Continuous (exponential) reset, decay time  $\geq \mathcal{O}(100\mu\text{s})$
- Fast rise times:  $\mathcal{O}(10\text{ ns})$ , bandwidth 50MHz
- Suited for detector capacitances in range  $\sim 1 - 10\text{ pF}$
- Operational in liquid argon at 87 K
- Low power consumption (avoid bubbling of cryostatic liquid)
- Driving differential signal over distance of  $\sim 10\text{ m}$
- Robustness to electrostatic discharges (ESD protection VS noise)

## Digital Signal Processing – Why we need certain decay shape?

- DSP for LEGEND:
  - Baseline correction
  - Waveform smoothing
  - Pole-Zero correction
  - Signal shaping (trapezoidal)
  - Energy reconstruction
  - Further analysis:
    - Pulse-Shape Analysis, Drift-Time correction etc.



(a) Charge signal.



(b) Shaped charge signal (trapezoid).

# Deconvolution

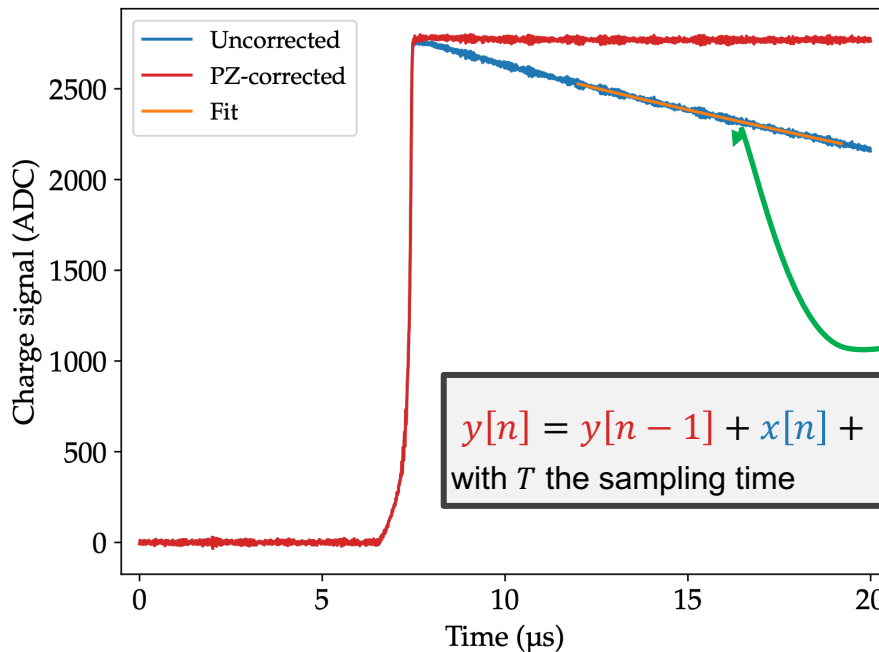
## Digital Signal Processing – Deconvolution

### Convolution

Every waveform = convolution of the charge input signal coming from the detector with the response function of the RC-feedback (and gained according to the CSA properties).

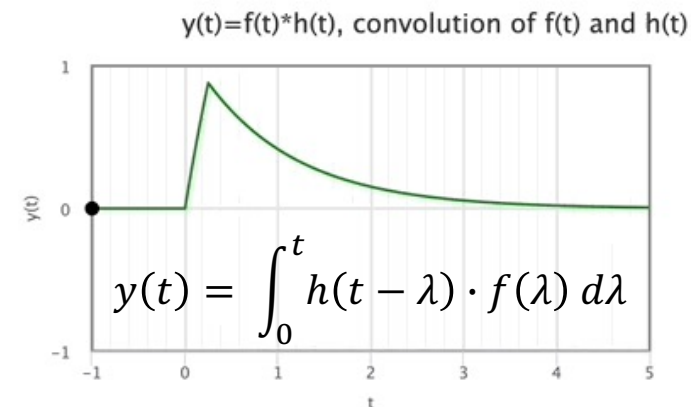
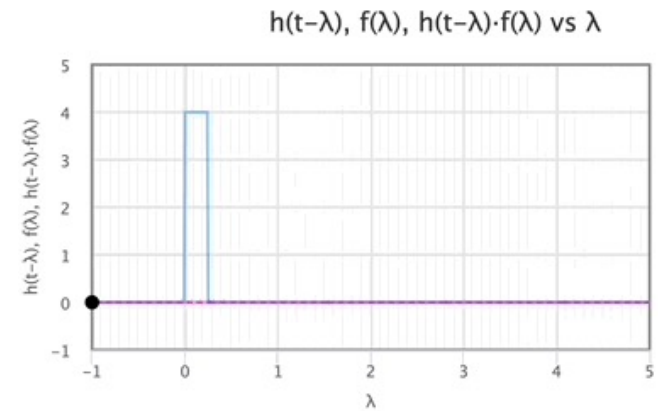
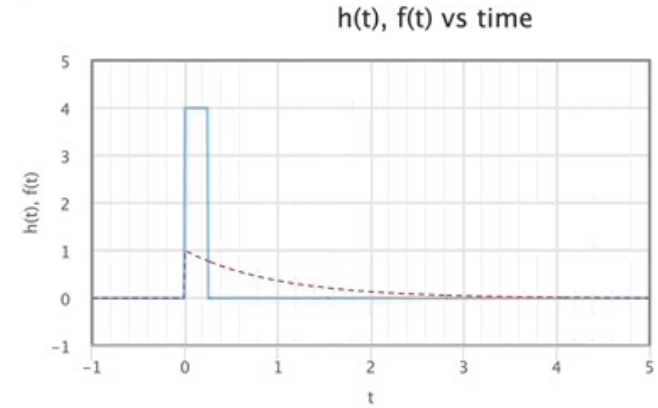
### Deconvolution

Infinite-Impulse-Response Filter (IIR) which corresponds to the inverse transfer function of the CSA while only require the decay time  $\tau = RC$



$$y[n] = y[n - 1] + x[n] + e^{-\frac{T}{\tau}} \cdot x[n]$$

with  $T$  the sampling time



## Simple CSA

Consists of:

- Feedback capacity combined with Operational Amplifier ("Integrator")
- Input voltage:  $V_{in} = \frac{Q_s}{C_{det} + C_i}$

1. Output voltage of amplifier:  $v_o = -Av_i$
2. „Node rule

$$v_i = v_f + v_o$$

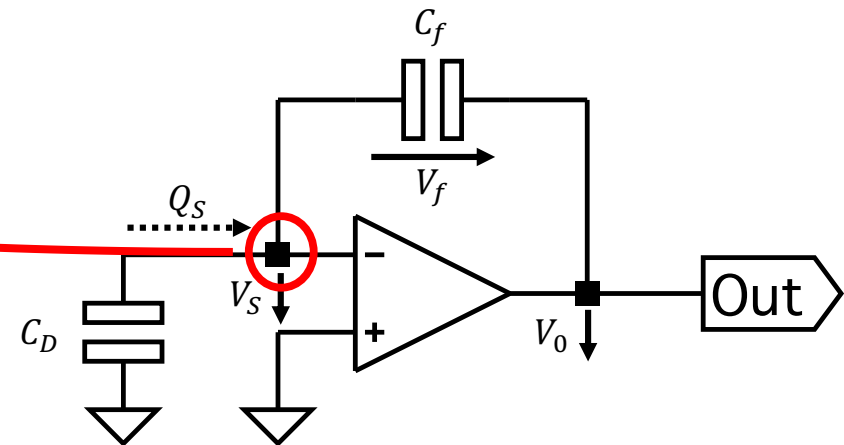
$$\Rightarrow v_f = (A + 1) \cdot v_i$$

3. "Ideal no current in OpAmp":

$$Q_i (= Q_f) = C_f v_f = C_f (A + 1) \cdot v_i$$

$$\Rightarrow v_o = \frac{-A}{C_f \cdot (A + 1)} Q_i$$

$$\Rightarrow v_o \approx \frac{Q_i}{C_f}$$

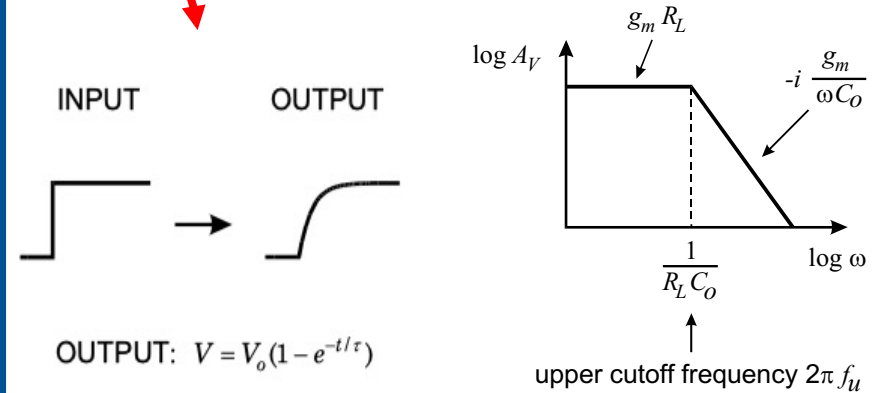
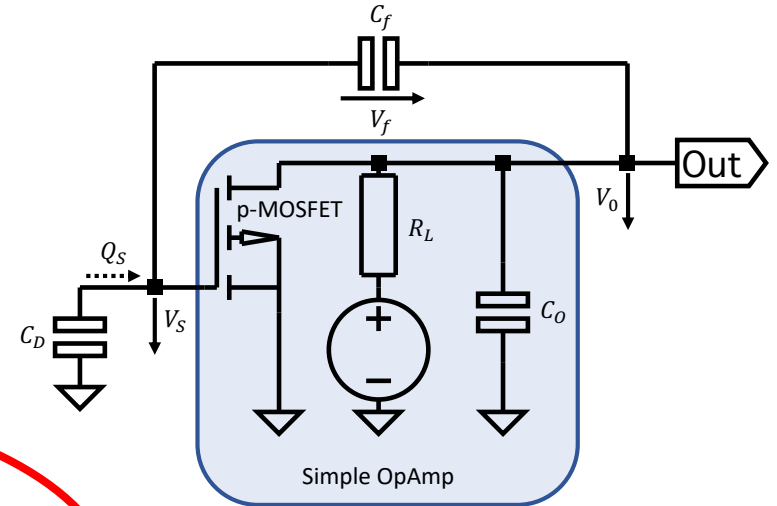


# Charge Sensitive Amplifier (CSA)

## What is the problem?

Realistic CSAs are frequency dependent:

- $A_\omega = g_m \left( \frac{1}{R_L} + i\omega C_0 \right)^{-1}$ 
  - $A_\omega$ : gain
  - $g_m$ : transconductance
  - $R_L$ : series resistance
  - $C_0$ : parallel capacity
- For low frequencies: gain constant
- For high frequencies: drops off linearly  
First need to “load the capacitance”
- A JFET before the OpAmp cancels this out
  - At high frequencies:
    - ➡ JFET holds voltage “constant” while following the current coming from the detector
    - ➡ Acts as a “current source” for OpAmp
    - ➡ Lowest shot noise of all available components

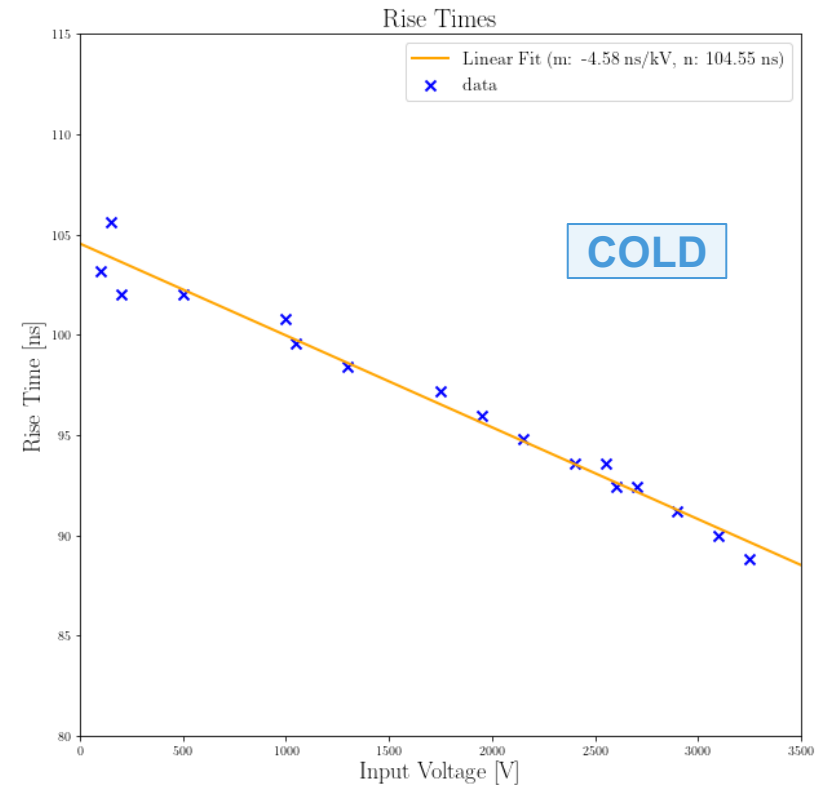
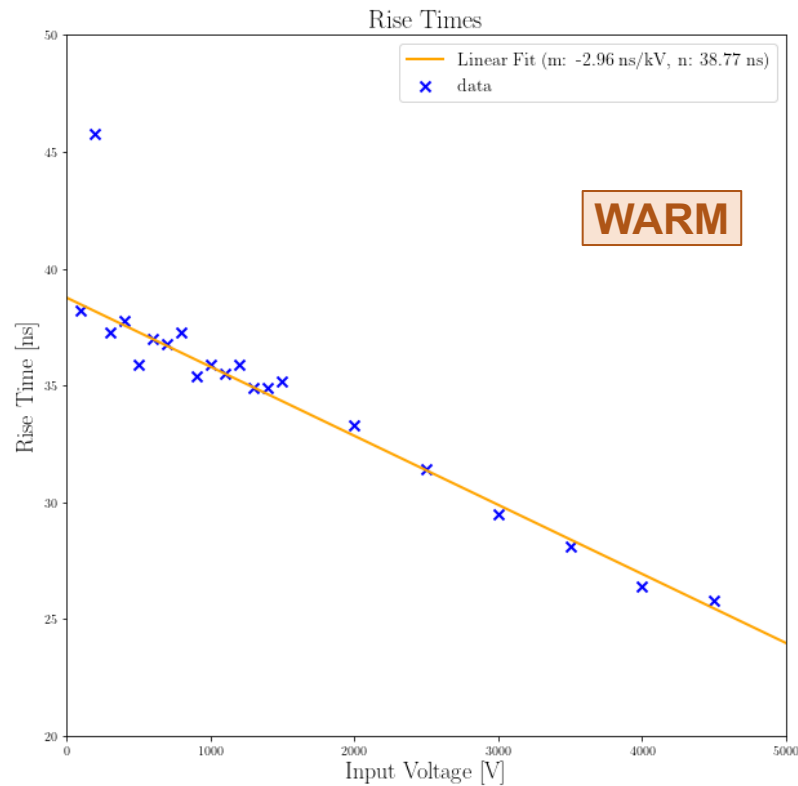


$$\left( \frac{S}{N} \right)^2 = \left( \frac{S}{N_1} \right)^2 \frac{1}{1 + \left( \frac{N_2}{A_1 N_1} \right)^2}$$

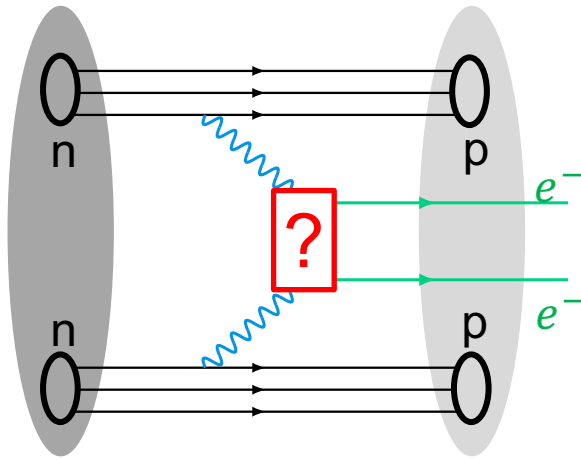
$$\text{ENC}^2 = \underbrace{\alpha \frac{1}{\tau_s} \frac{2k_B T}{g_m} C_{tot}^2}_{\text{series: ENC}_p^2} + \underbrace{\beta A_f C_{tot}^2}_{1/f: \text{ENC}_s^2} + \underbrace{\gamma \left( e I_{tot} + \frac{k_B T}{R_F} \right) \tau_s}_{\text{parallel: ENC}_{1/f}^2}$$

## L1k preliminary ASIC – Rise Times

- Rise Times (10%-90%) in the desired range (< 100ns) for the **warm** and the **cold** setup
- Rise Time depends linear on the input voltage ( $\sim$  energy)



# Neutrinoless double beta ( $0\nu\beta\beta$ ) decay



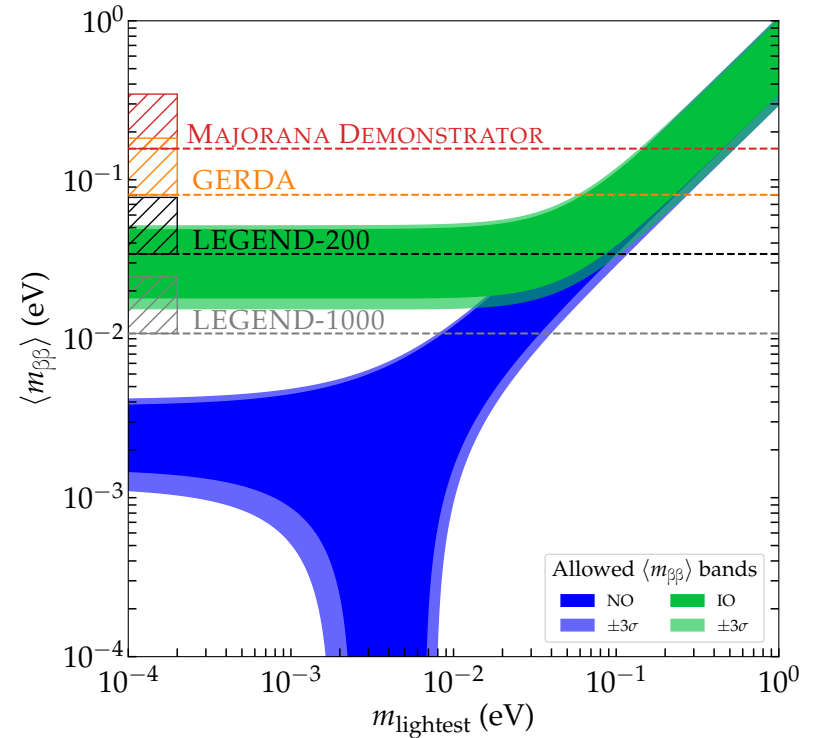
$$\langle m_{\beta\beta} \rangle \propto \frac{1}{g_A^2 |M^{0\nu}|} \sqrt{\frac{1}{T_{1/2}^{0\nu} G^{0\nu}}}$$

$\langle m_{\beta\beta} \rangle$ : Effective Majorana mass  
 $T_{1/2}^{0\nu}$ : Decay half-life  
 $M^{0\nu}$ : Nuclear matrix element  
 $G^{0\nu}$ : Phase space factor

$$\begin{aligned} \langle m_{\beta\beta} \rangle &= \left| \sum_i U_{ij}^2 m_i \right| \\ &= \left| \cos^2 \theta_{12} \cos^2 \theta_{13} m_1 + e^{2i\alpha} \sin^2 \theta_{12} \cos^2 \theta_{13} m_2 + e^{2i\beta} \sin^2 \theta_{13} m_3 \right| \end{aligned}$$

## Neutrinoless double-beta decay

Double beta decay without emission of two anti-neutrinos  
 → Neutrinoless double beta decay ( $0\nu\beta\beta$  decay)



# LEGEND Sensitivity

$$T_{1/2}^{0\nu}(3\sigma \text{ DS}) \propto \begin{cases} f_{\text{enr}} \cdot \epsilon_{\text{det}} \cdot \sqrt{\frac{M \cdot t}{BI \cdot \Delta E}} & \text{with background} \\ f_{\text{enr}} \cdot \epsilon_{\text{det}} \cdot M \cdot t & \text{background - free} \end{cases}$$

