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Module Link Issues

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Constraints

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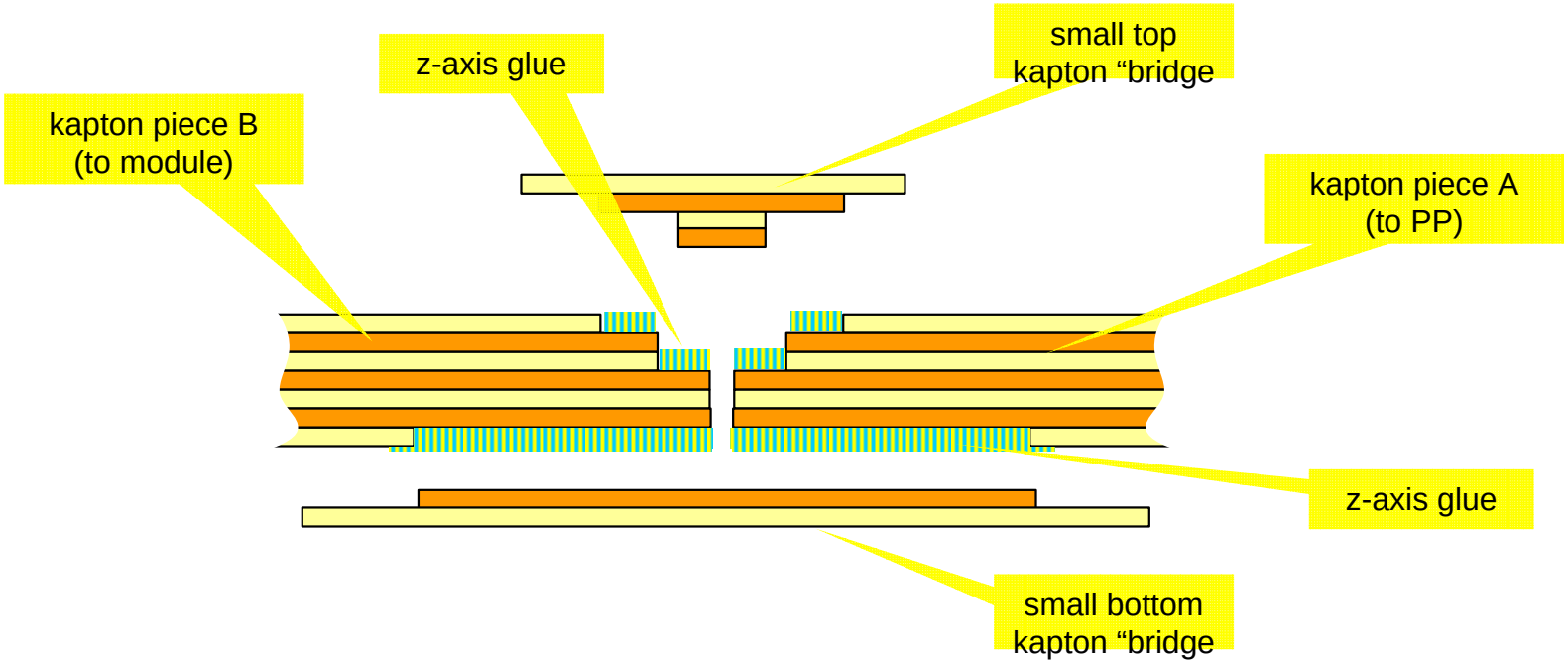
- need to cover 12-15m between module and DHH with combination of kapton and TWP cables
- active repeater circuits not recommended (radiation hardness, space, power consumption)
- no bulky connection between kapton and TWP/power cables
- make kapton part as short as possible
  - signal integrity issues with kapton flex: dielectric loss of the polyimide, resistive loss of the narrow signal traces
  - standard S/FTP (shielded foil twisted pair cable, Cat-6) dose not degrade the signal transmission too much

Constraints

- make the connection outside of the shield
  - better handling during installation
  - more space for patch panel

  ➔ may have to stitch two kapton parts to extend the length > 40cm (min. length to have the PP just outside the shield)



Connection between Kapton and TWP / Power Cables

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Option 1: flex cable with rigid end to mount connectors for data & power cables

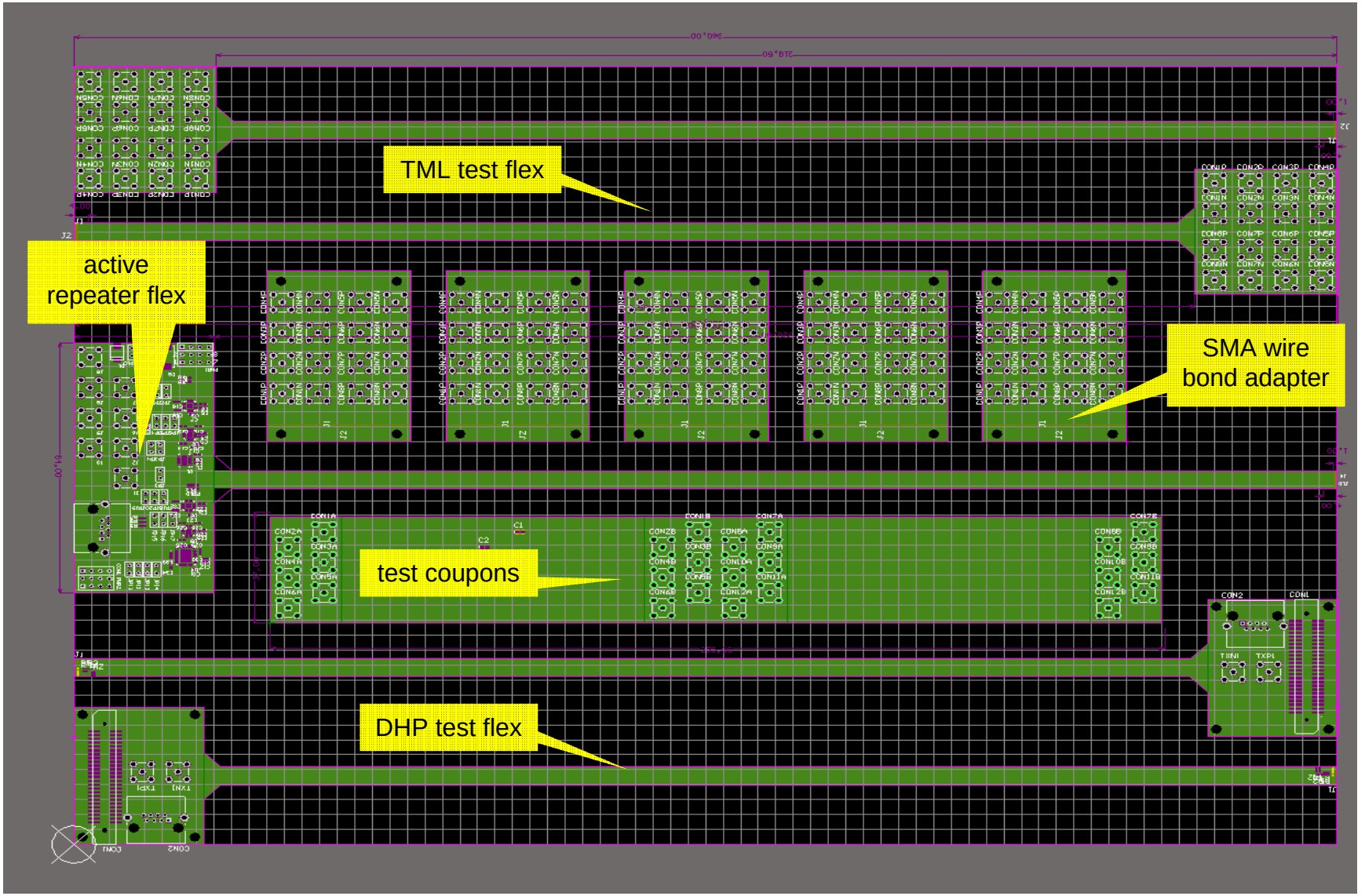
- preferred solution for S.I and mechanical handling
- but to connectors would be to bulky

Option 2: flex cable without rigid part (no PP). The TWP and power cables would be soldered to a small PCB which in return would have a small flex connector

- could be much smaller
- flex connector for three layer flex not so easy to implement

Option 3: like 2 but have a small rigid part on the flex end and mount a high density (non-flex) connector on it which mates with the connector on the cable PCB

Flex Test Designs



Test system Status

- Flex test
  - test structures ordered (I.V. Schaltungen)
  - second vendor contacted (Cicorel, may have HF base material available)
- DHP test system
  - PCBs (Hybrid PCB + FPGA board piggy board) ➔ expected end of the week
  - FPGA card programming (XUPV5 board) ➔ ongoing (Sergey, Tomek)
  - waiting for wire bond adapter

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backup

Signal & Power lines

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- Digital signals between DHH and DEPFET module (DHP)

Signal name	Type	Description	Comment
GCK	LVDS in	system clock = 1/8 rowClk (~100 MHz)	generated from RF clock F0 adjusted by additional factor on the DHH
FCK	LVDS in	99.2 kHz frame clock	synchronous to the beam gap
TRG	LVDS in	trigger	10-30 kHz
TMS	LVDS in	JTAG mode select	
TCK	LVDS in	JTAG clock	
TDI	LVDS in	JTAG data in	
TDO	LVDS out	JTAG data out	
RST	LVDS in	reset	for all chips? polarity?!
DO[3:0]	CML out	DHP data out	one per chip

1.25 Gbps

- Power lines
  - DCD (3x analog + digital)
  - DHP (digital IO + core)
  - Switcher (4x analog + digital)
  - DEPFET bias (5x)

Power / bias lines

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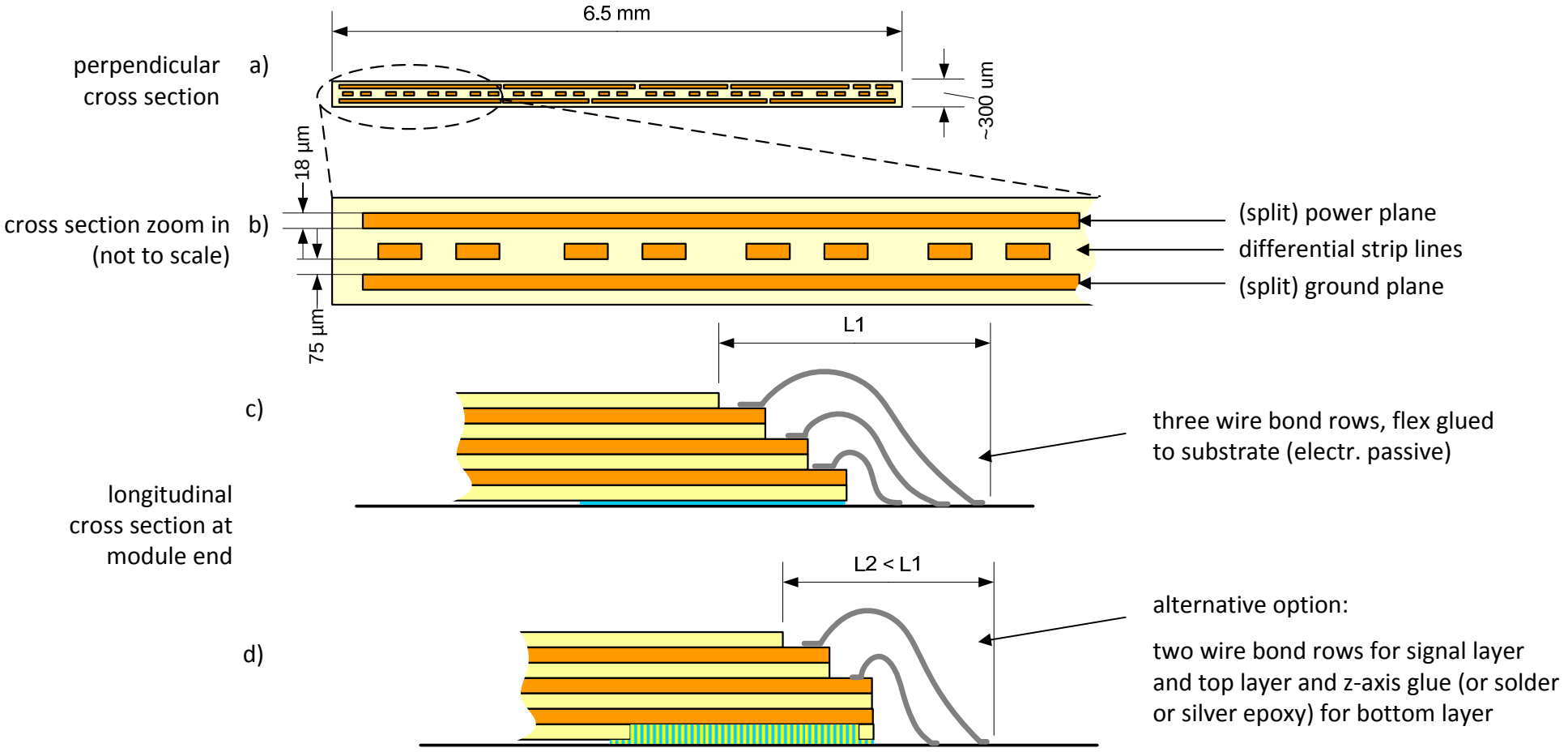
	name	type	voltage [V]	current [mA]	comment	cable	twin	coax	width [mm]	voltage drop [V]
power supplies	VDDA	DCD analog	1,8	2300	sense line		1	6	3,48	0,35
DCD	VDDD	DCD digital	1,8	800	sense line				1,21	0,35
	REFIN	DCD analog ref	1,1	100	sense line		1	2	0,15	0,35
	DGND	commor digital ground	0	800	common					
	AGND	analog ground	0	2300	sense line		1	6	3,48	0,35
	AMPLOW		0,35	1500	sense line		1	4	2,27	0,35
DHP	VDDIO	DHP IO rail	1,8	100	sense line		1	2	0,15	0,35
	VDDC	DHP core	1,2	500	sense line		1	5	0,76	0,35
	DGND	digital ground	0	600	common					
SWITCHER	VDDS	digital supply	3,3	4				1	0,01	0,35
	DGND	digital ground	0	4	common					
	V.TAG	JTAG IO rail	1,8	4	common					
common	VDDIO	commor IO rail + DCD digital	1,8	904	sense line		1	4	1,37	0,35
	DGND	digital ground	0	1404	sense line		1	6	2,12	0,35
bias voltages	Vclear_on	clear on	~17	30			1			
	Vclear_off	clear off	~8	30			1			
	Vgate_on	gate on	~1	30			1			
	Vgate_off	gate off	~13	30			1			
	Vsource	source	7	100			1	1		
	Vceg	commor clear gate	~7	0			1			
	Vbulk	bulk	~17	0			1			
	Vguard	gurad ring (edge)	?	0			1			
	Vbias	backplane	-20	0			1			
					signal pins:	24	17	37		
		power current		4896	total sum:			78	15.00	

- min. copper width (17µm copper) for ΔU < 0.4 V (10A, 50 cm length): 15 mm
- total flex width (including digital, bias and sense lines): ~24 mm ➔ 3 layer flex, 6 mm wide
- still some safety factor if 35µm instead of 18µm copper for power layers would be used

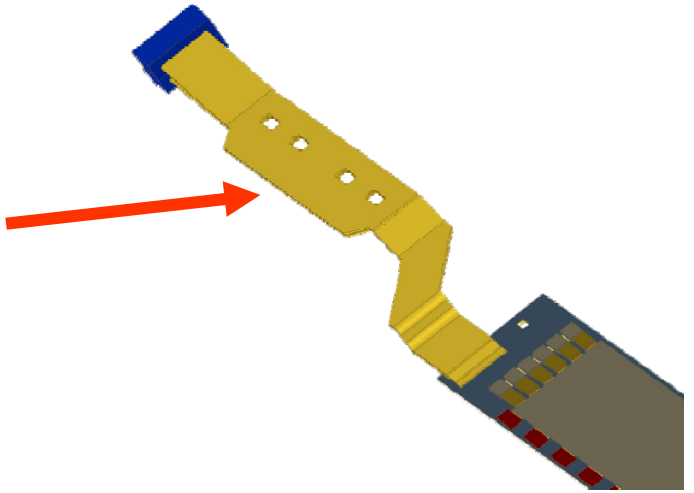
Proposed layer stackup



Signal integrity simulation - outlook

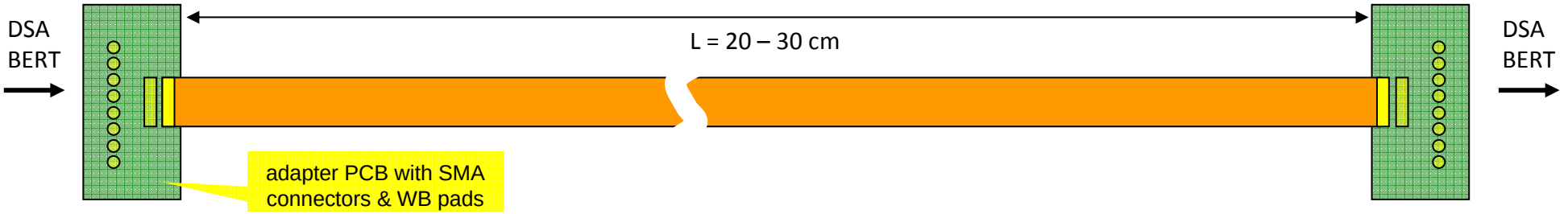
work in progress:

- define simulation model for DHP CML driver
- layer stackup for routing on silicon substrate (2 or 3 metal layers)
- simulate different receiver components
  - repeater ICs
  - TWP or coax cables (for passive patch panel option)
- board level simulation
  - import flex design and re-simulate
  - will be important for designs with complex flex outline



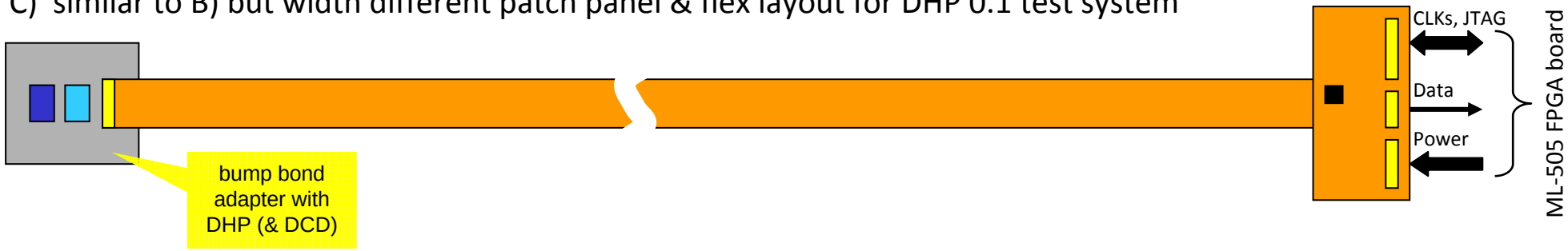
Prototype flex designs variants

A) diff. TML pairs with line width / spacing variations, WB balcony on both ends

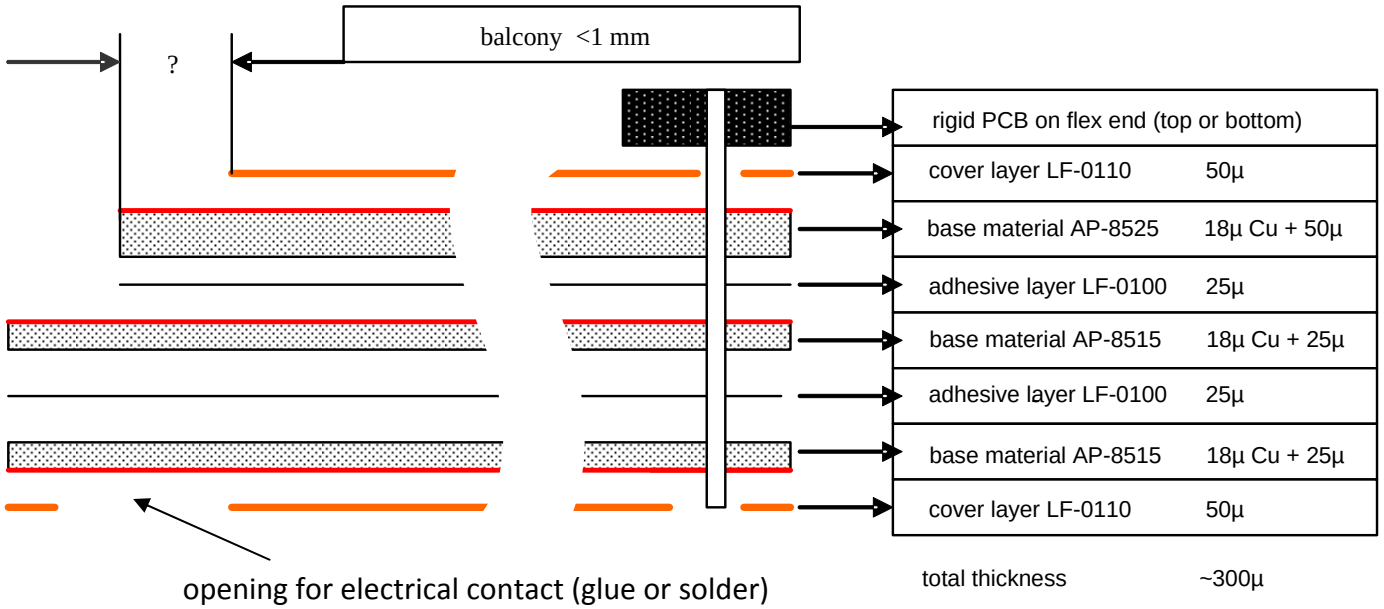


B) diff. TML pairs, patch panel on one side with different board equalizer ICs (repeaters) + connectors

C) similar to B) but width different patch panel & flex layout for DHP 0.1 test system



Layer stackup for test flex



- design rules (for 18µm copper):
  - 100µm line width & spacing (80µ line width?)
  - 200µm/400µm via hole/outer ring diameter
  - dielectric constant: 3.4 – 3.6 for all isolation layers
- 75µm dielectric above and below the (inner) signal layer
- bottom layer “upside-down” for glue attach area