

The International Linear Collider Project

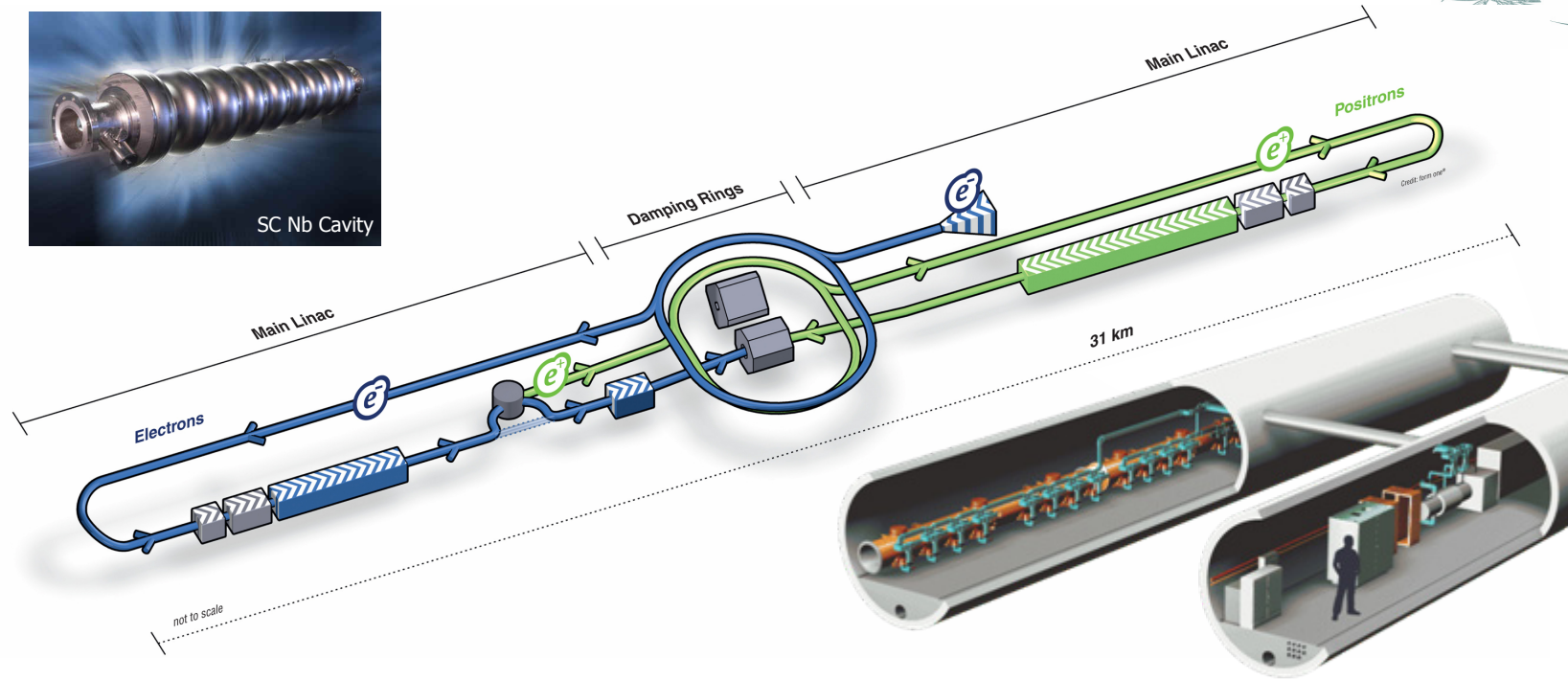
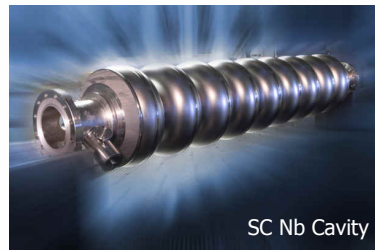
-: Introduction, General Overview

-: MPI Involvements

-: Software Developments/Simulation

-: Status of the DEPFET VTX Project

● The International Linear Collider (RDR, 2/2007)

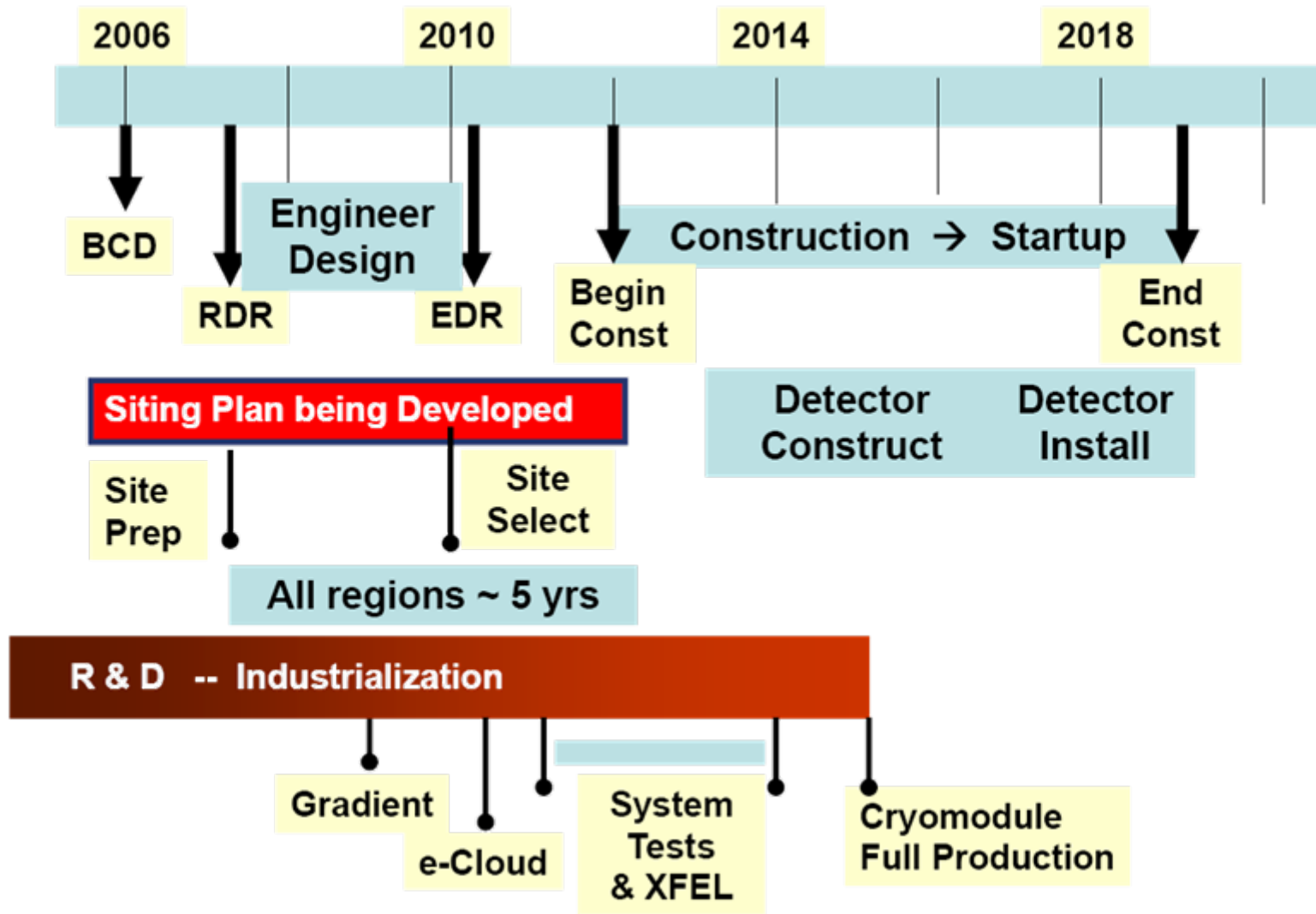


- e⁻-e⁺ collider: two 11 km SC linacs at 31.5 MV/m
- Dual tunnel configuration (safety and accessibility)
- Single IR, crossing angle 14 mrad, two detectors in push-pull operation

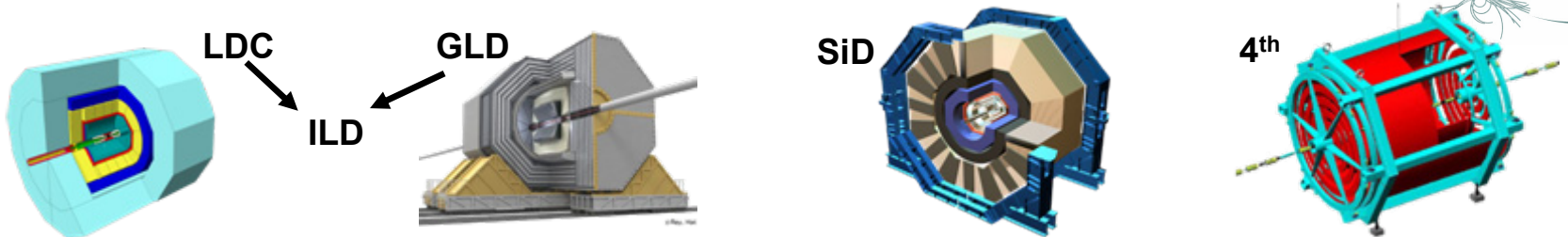
Parameters:

- $\sqrt{s} = 500 \text{ GeV}$, tunable from 200 to 500 GeV, upgradeable to 1 TeV
- $\int L dt = 500 \text{ fb}^{-1}$ in 4 years (peak luminosity $2 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1}$)

● Technically Driven Timeline (GDE)



● The ILC Detector Concepts



Detector	Premise	Vertex Detector	Tracking	EM calorimeter	Hadron calorimeter	Sole-noid	Muon System
LDC ILD GLD	PFA	5-layer pixels barrel only	TPC Gaseous	Silicon-Tungsten	Analog- scintillator	4 Tesla	Instrumented flux return
	PFA	6-layer pixels 1 discs	TPC Gaseous	Scintillator-Tungsten	Digital/Analog Pb-scintillator	3 Tesla	Instrumented flux return
SiD	PFA	5-layer pixels 4 discs	Silicon strips	Silicon-Tungsten	Digital Steel - RPC	5 Tesla	Instrumented flux return
4 th	Dual Readout	5-layer pixels	TPC Gaseous	2/3-readouts Crystal	2/3-readouts Tungsten-fiber	3.5 Tesla	Iron free dual solenoid

Requirements: Impact parameter resolution: $\sigma_{r\phi} \approx \sigma_{rz} \approx 5 \oplus 10 / (p \sin^{3/2} \theta)$
 Momentum resolution: $\sigma(1/p_T) = 5 \times 10^{-5} (GeV^{-1})$
 Jet energy resolution: $\sigma_E / E = (3-4)\%$

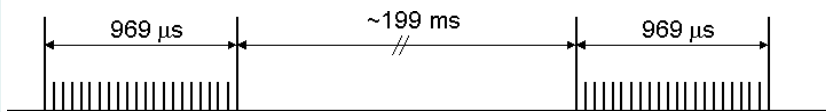
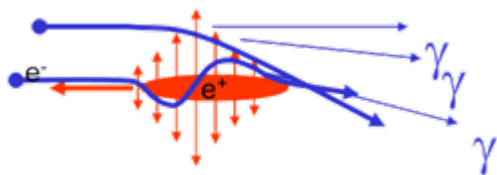
Call for Letters of Intent October 2007, due October 2008
 → first step towards the formation of 2 proto-collaborations! Produce EDRs by ~ 2010

● LHC \leftrightarrow ILC Environment



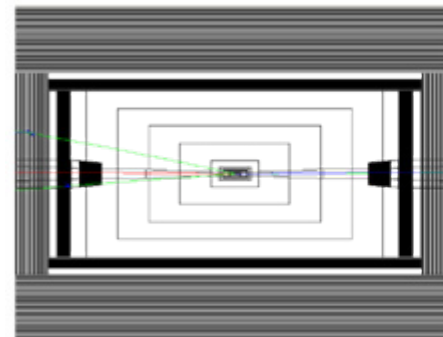
	LHC	ILC
Event rates:	1GHz	1kHz
beam structure (BX):	25ns, cont.	~ 370 ns, 0.5% Duty Factor
Triggering:		
L1&L2	40MHz \rightarrow 1kHz	no hardware trigger
L3 (software)	100 Hz	15kHz \rightarrow 100Hz
Radiation Field:	$\sim 10..50$ Mrad/year	$\sim 10..50$ krad/year

But there is another challenge at the ILC \rightarrow background due to beamstrahlung!

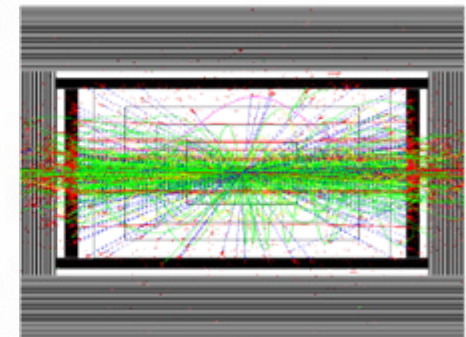


time structure: 5 trains with 2625 bunches per sec

1 BX



150 BX

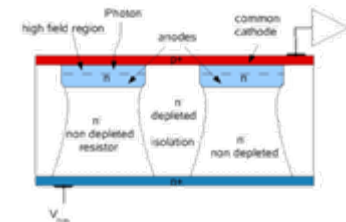
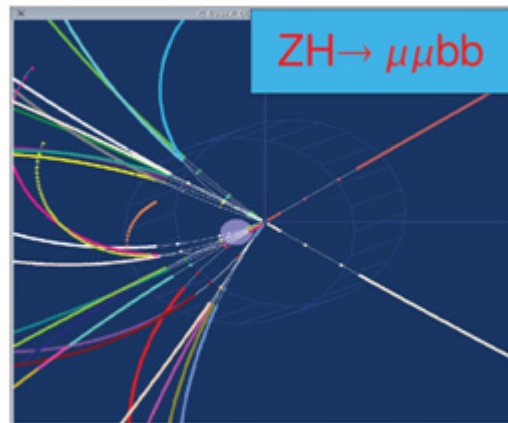
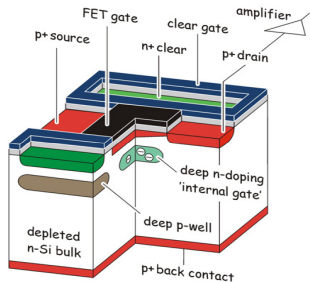


e^-e^+ pairs, μ and hadronic events in the SiD Detector

MPI Activities within the ILC Project



- Development of a **DEPFET based VXD** → DEPFET Collaboration
 - part of the EUDET Program
- Development of **software tools** for
 - simulation of the DEPFET VXD
 - track reconstruction and their application in detector optimization studies
- Coordination of TPC tracking activities within the **LCTPC Collaboration**
- Since summer 2007 member of the **CALICE Collaboration** (Calorimetry, see Frank's talk tomorrow)
 - Participation at the test beam summer 2007
 - Development of Geiger-mode APD arrays ("SiPM") suitable for large scale production

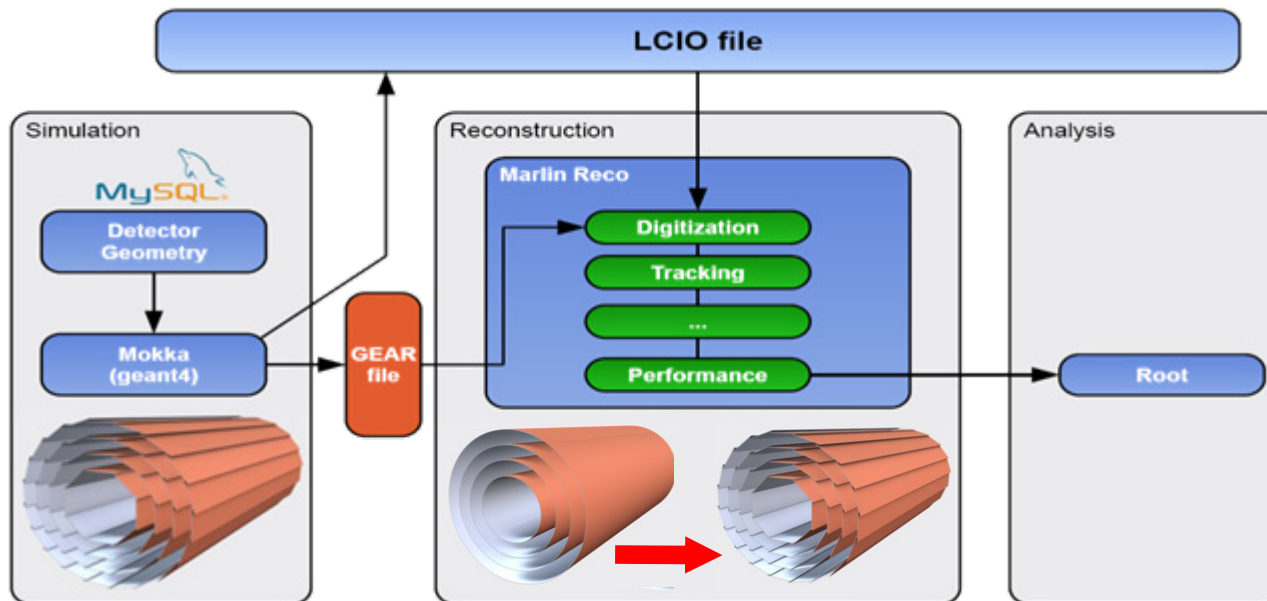
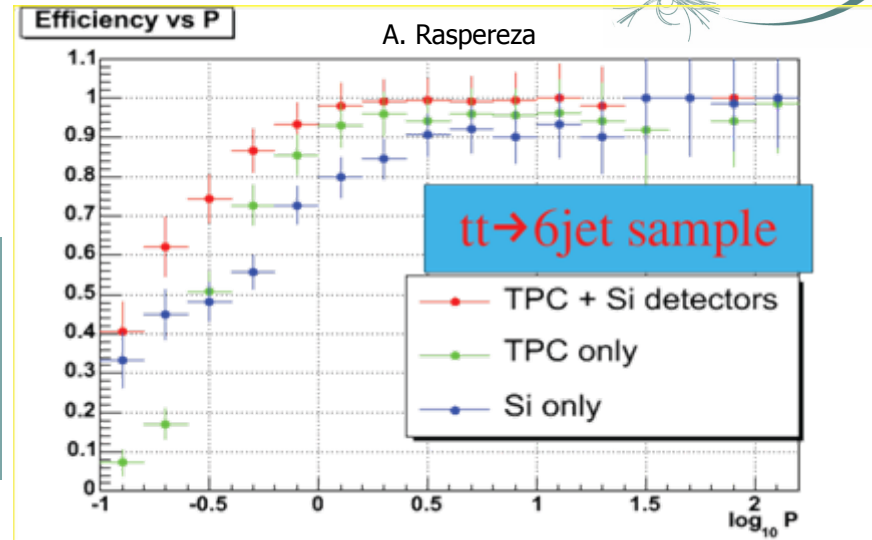


● Software Tools: Full tracking for the LDC

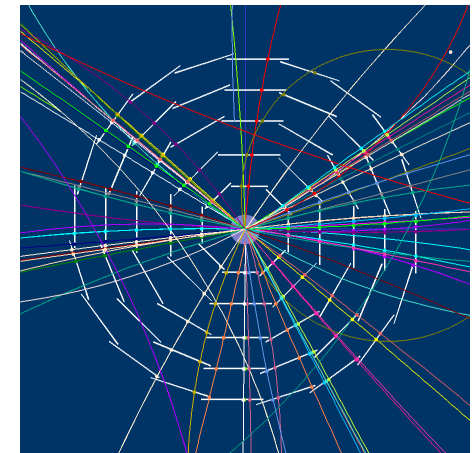
- Tracking extended to forward and intermediate silicon detectors
- Linked to TPC tracks
- Realistic full tracking for LDC detector

New:

Implementation of VXD ladders in the reconstruction



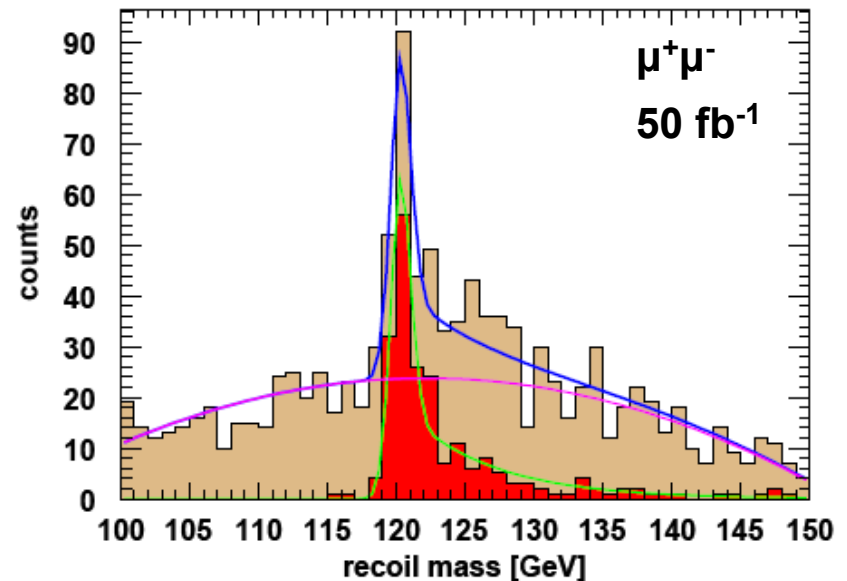
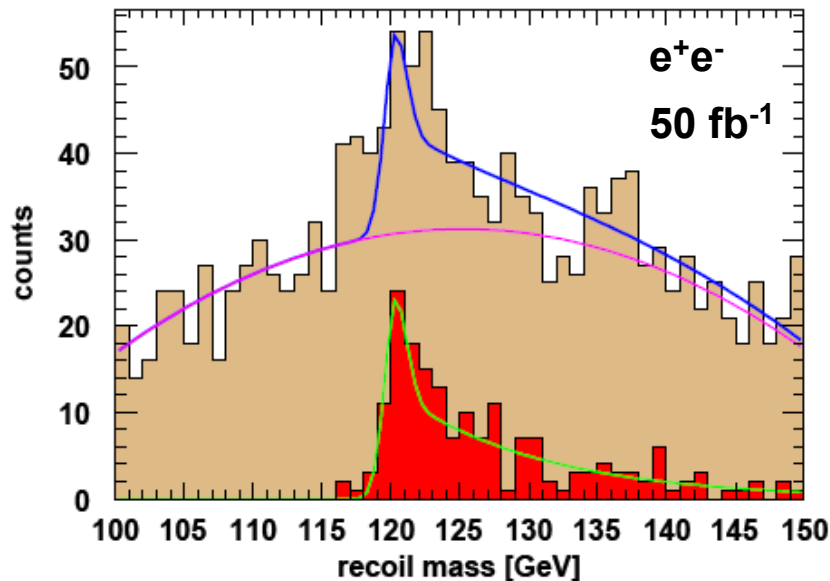
$e^+e^- \rightarrow t \bar{t}$



A. Moll

● Software Tools: Application to Higgs analysis

- Reconstruct recoil mass for Higgs $Z \rightarrow e^+e^-, \mu^+\mu^-$
- Model independent, Benchmark process for tracking at ILC, $m_H = 120$ GeV assumed
- Goal: Find optimal \sqrt{s} for mass and Xsect measurement \Rightarrow Result: 250 GeV
- $\Delta m = 120$ MeV and $\Delta\sigma/\sigma = 9\%$ for only 50 fb^{-1}

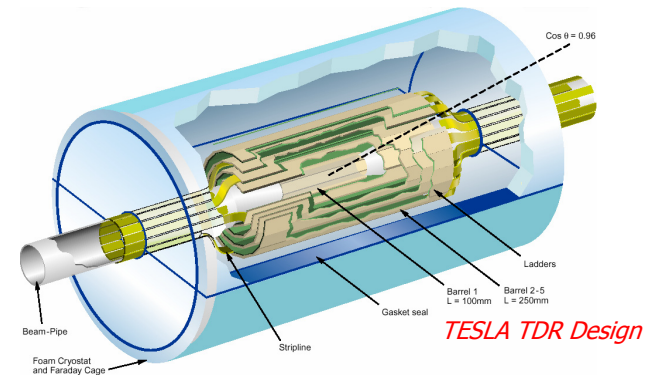


To reach the same accuracy at $\sqrt{s} = 350$ GeV, 500 fb^{-1} are needed

● Generic Layout of the ILC Vertex Detector - 5 layer barrel

superb impact parameter resolution: $\sigma_{r\phi} \approx \sigma_{rz} \approx 5 \oplus 10 / (p \sin^{3/2} \theta)$

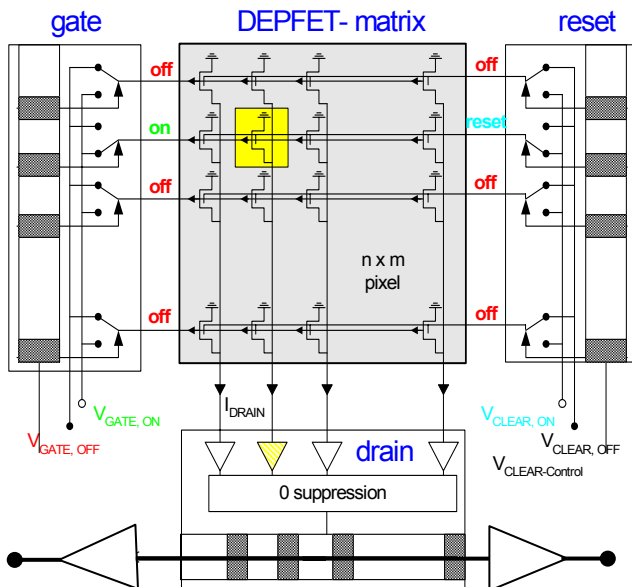
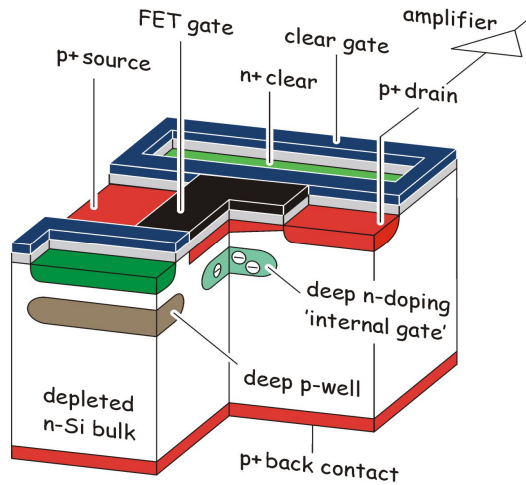
- Minimal material budget: $< 0.1\% X_0$ / layer
(Equivalent to 100 μm of Silicon)
- Minimal power consumption ($< 50\text{W}$)
- 20-30 μm pixel size
- Tolerant to high machine background



Competition of about 10 Technologies with different philosophies how to cope with background

1. read out during bunch train, accumulation of about 75-150 BX
-: CP-CCD, Mimosā, DEPFET..
2. read out during the 200ms pause, accumulation of about 3000 BX
-: FP-CCD
-: ISIS, CAPS, FAPS (in-pixel storage of ~ 20 frames)
3. read out during the 200ms pause and time stamping of each hit
-: ChronoPixel, SOI, 3D Integrated Pixel...

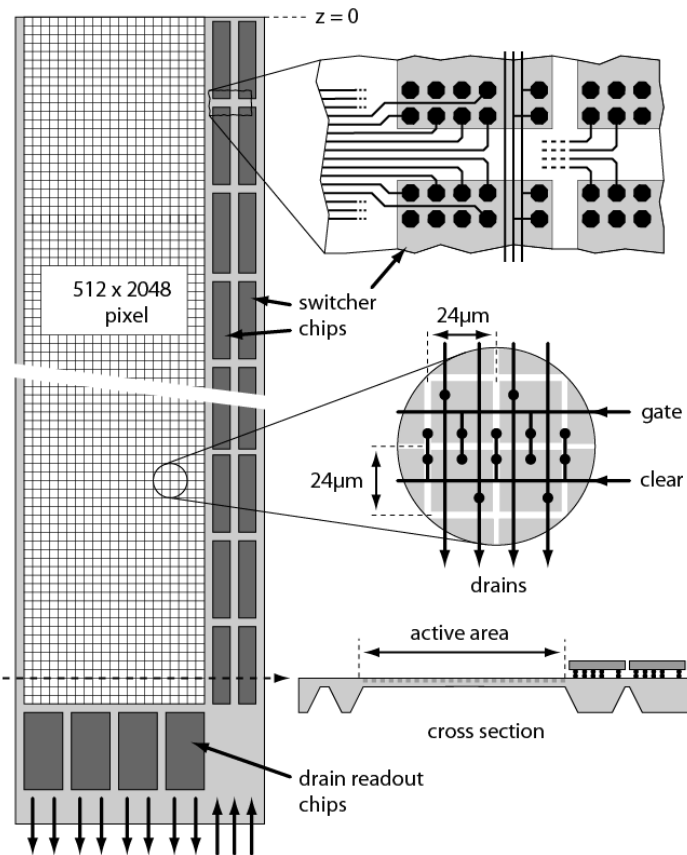
Why DEPFET?



- fully depleted sensitive volume
 - fast signal rise time (\sim ns), small cluster size
- Fabrication at MPI HLL
 - Wafer scale devices possible
 - no stitching, 100% fill factor
- no charge transfer needed (in contrast to CCDs)
 - faster read out
 - better radiation tolerance
- internal amplification
 - large signal, even for thin devices
 - r/o cap. independent of sensor thickness
 - charge-to-current conversion:
 $g_q = dI_d/dq \approx 1 \text{ nA/electron}$, scales with gate length
- Charge collection in "off" state, read out on demand
 - potentially low power device

● The ILC DEPFET Collaboration

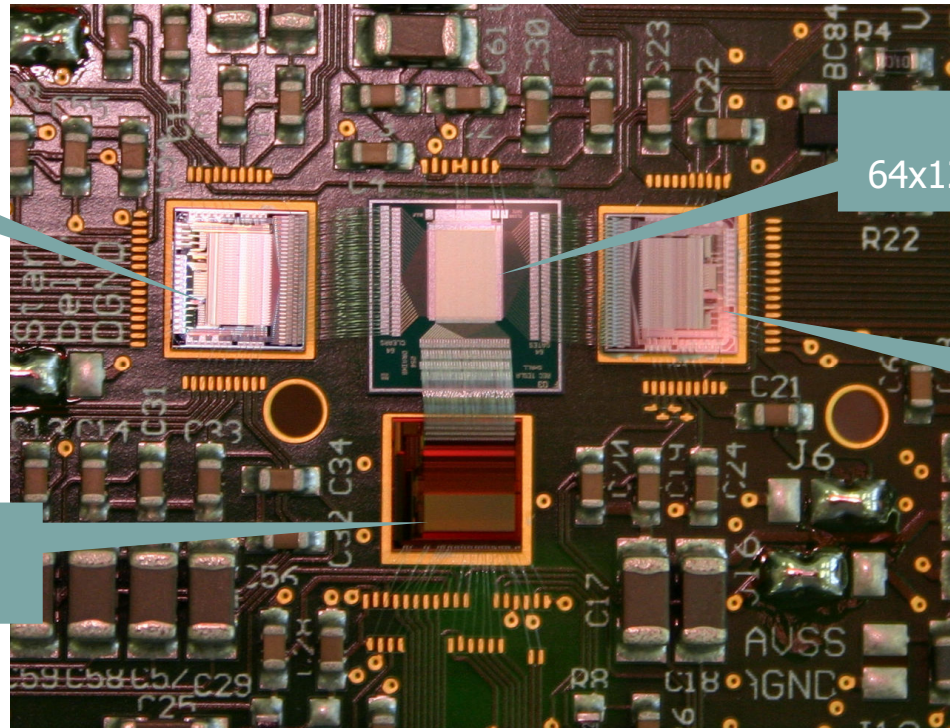
www.depfet.org



- ILC VXD Baseline Design
- 5 layer, old TESLA layout
 - 10 and 25 cm long ladders read out at the ends
 - 24 micron pixel
 - design goal 0.1% X_0 per layer
 - 50 µm thin sensitive region

	DEPFET/Ladder Sim. and Irrad.	Auxiliary ASICs Development	System Development	System Tests and Test Beams
Aachen			X	
Bonn		X	X	X
Karlsruhe	X			
Mannheim		X	X	X
Munich	X			X
Prague			X	X
Valencia			X	X

● ILC Prototype System



Gate Switcher

DEPFET Matrix
64x128 pixels, 33 x 23.75µm²

Clear Switcher
Uni Mannheim

Current Readout
Uni Bonn CUROI I

PXD4 DEPFET version thoroughly tested:

- : Single Pixel Tests
- : Clear Studies and Laser Tests
- : Beam tests at DESY and CERN
- : Tuning of the Sim. with beam test results
- :

In the following minutes:

- : DEPFET Radiation Tolerance
- : News on Thinning Technology
- : The new PXD5 Production

● Radiation Effects: TID and NIEL

In the ILC VXD we expect in 5 years:

From e^-/e^+ pairs by beamstrahlung:

- : few 100 krad TID (total ionizing dose)
- : up to $10^{11} n_{eq}/cm^2$ NIEL

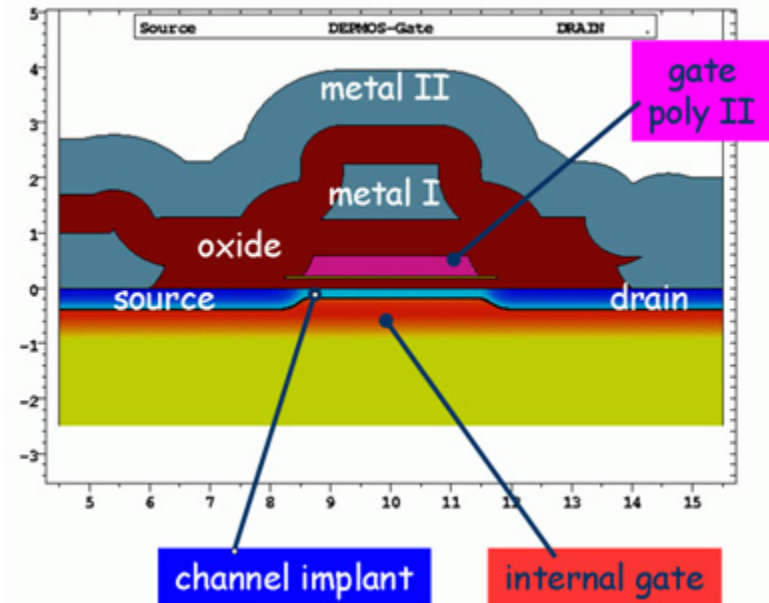
Add:

$10^9 n_{eq}/cm^2$ backscattered neutrons
muons from collimators, synchrotron radiation,
backscattered photons ...

Ionizing Radiation - Total Ionizing Dose (TID)

- Fixed oxide positive charge $\rightarrow \Delta V_T$
- interface trap density \rightarrow
 - reduced mobility (g_m)
 - higher $1/f$ noise

Gate Dielectrics: $\sim 200nm$

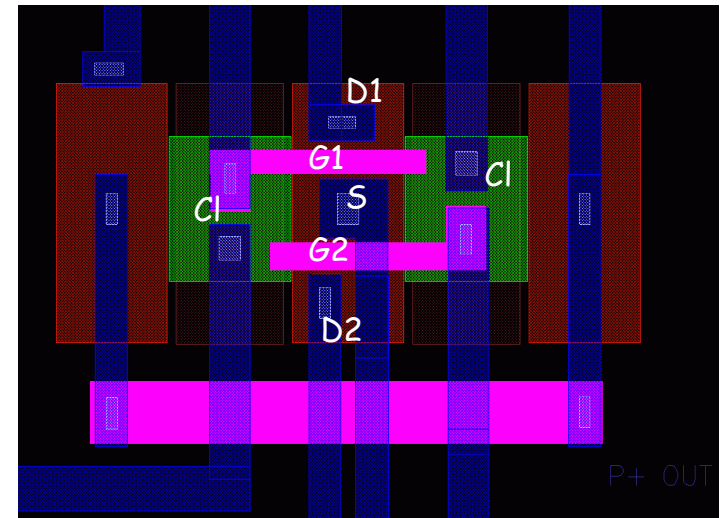


Non Ionizing Energy Loss (NIEL)

- leakage current increase \rightarrow shot noise
- trapping not considered to be critical

● Irradiations - Overview

- : Irradiations with ^{60}Co gammas, protons and neutrons
- : Single pixel structures with 6 and 7 μm gate length
- : Look for degradation in:
 - Electric characteristics (V_{th} shifts, g_m and g_q)
 - Leakage current
 - noise spectrum (1/f noise)
 - Spectroscopic performance

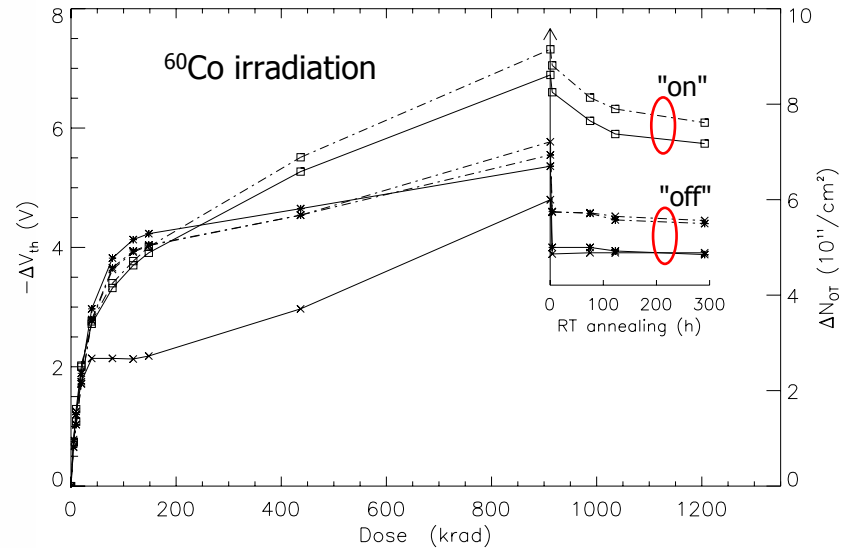
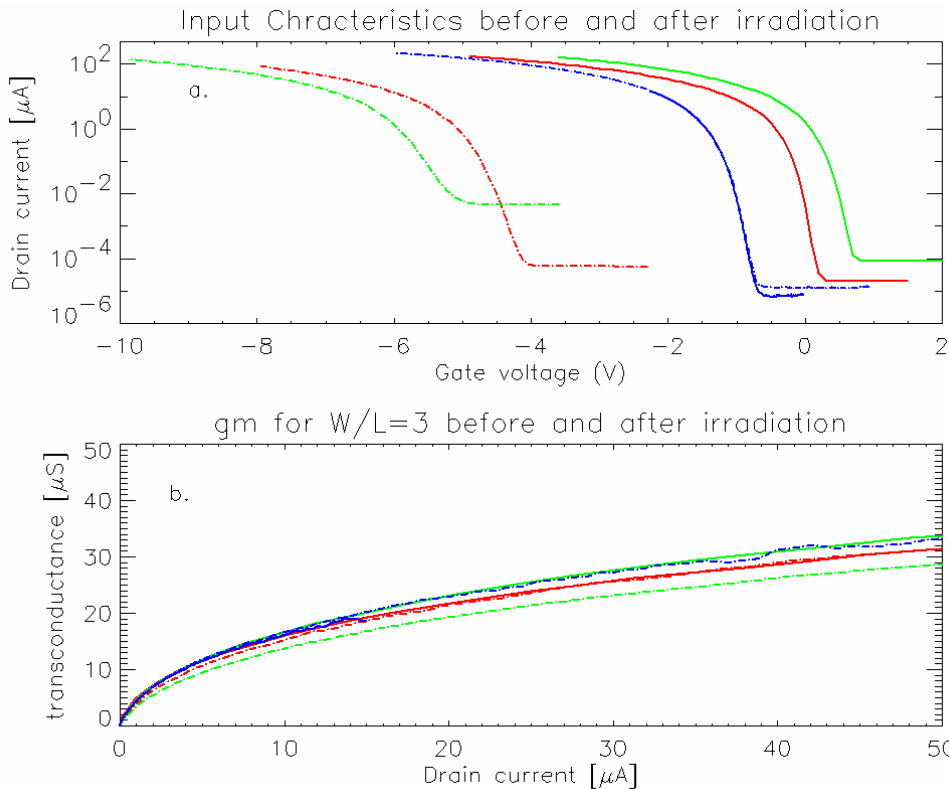


	PXD4-10 MO2	PXD4-5 M05	PXD4-2 J14
Type	Protons, 30MeV	Neutrons, 1-20MeV	Gammas - ^{60}Co
Fluence / Dose	$1.2 \cdot 10^{12}$ p/cm ²	$1.6 \cdot 10^{11}$ n/cm ²	913kRad
1MeV n equivalent	$3 \cdot 10^{12}$ n _{eq} /cm ²	$2.4 \cdot 10^{11}$ n _{eq} /cm ²	n/a

LBNL Cyclotron

GSF Munich

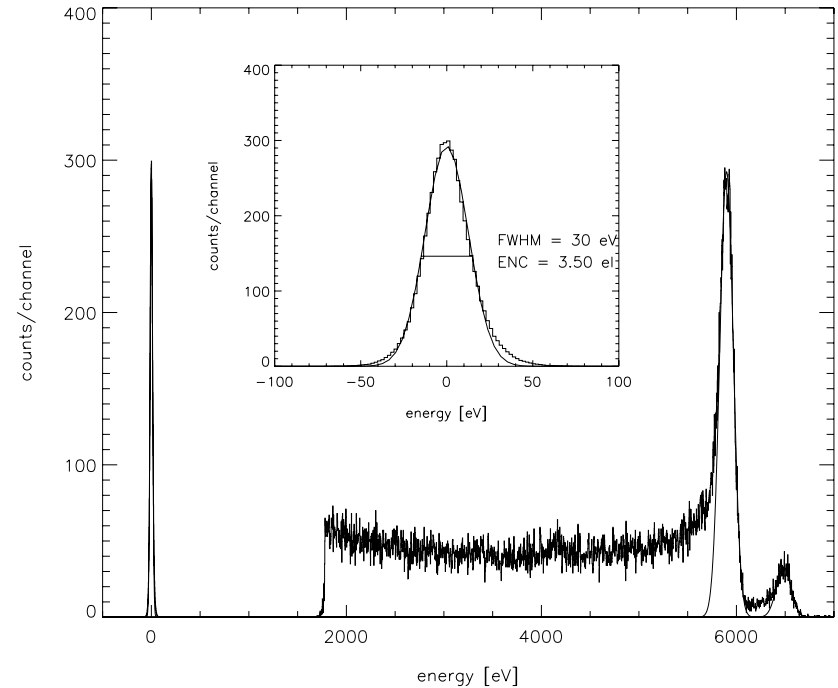
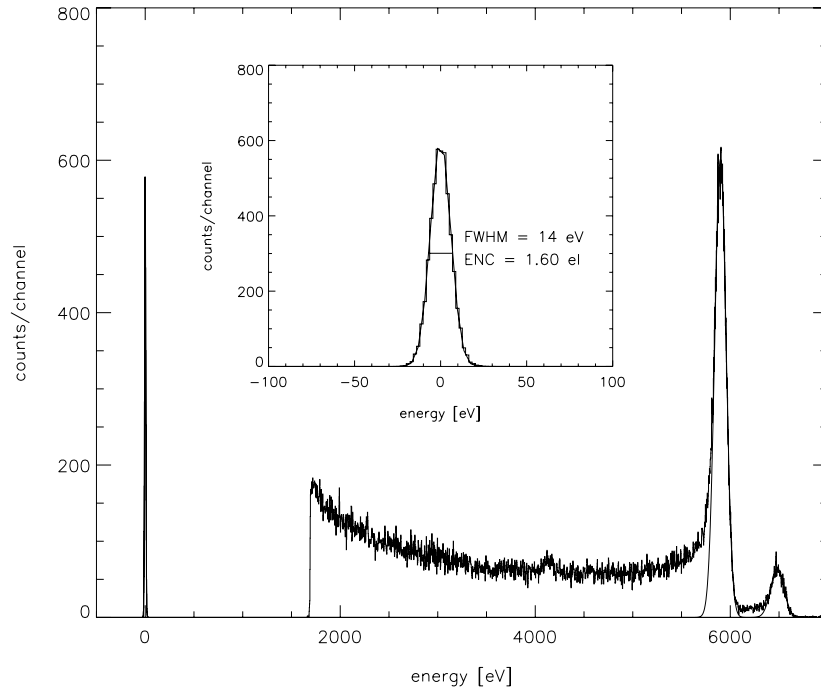
Basic Characteristics: ΔV_{T} , g_m , I_{Leak}



irradiation	TID / NIEL fluence	ΔV_{th}	g_m	I_{Leak} in int. gate at RT(*)
gamma ^{60}Co	913 krad / ~ 0	$\sim -4\text{V}$	unchanged	156 fA
neutron	~ 0 / 2.4×10^{11} n/cm ²	~ 0	unchanged	1.4 pA
proton	283krad / 3×10^{12} n/cm ²	$\sim -5\text{V}$	$\sim -15\%$	26 pA

(*) 5..22 fA non irradi.

● Spectroscopic Performance - ^{60}Co irradiation



non-irradiated

$V_{\text{thresh}} \approx -0.2\text{V}$, $V_{\text{gate}} = -2\text{V}$
 $I_{\text{drain}} = 41 \mu\text{A}$
 time cont. shaping $\tau = 10 \mu\text{s}$

Noise ENC = 1.6 e⁻ (rms)

at $T > 23 \text{ degC}$

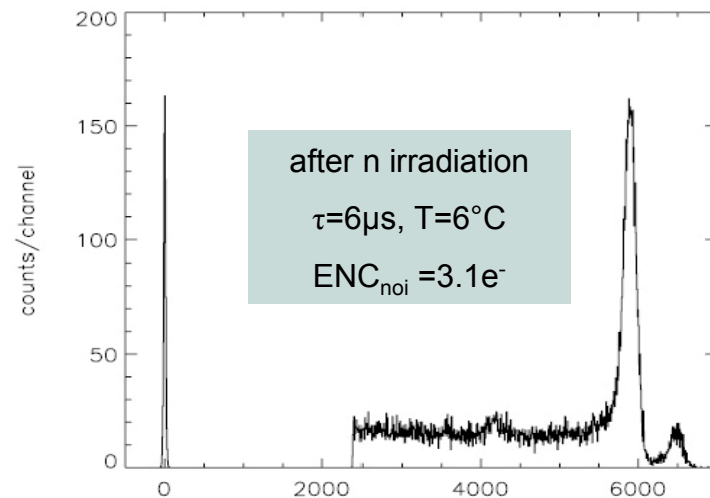
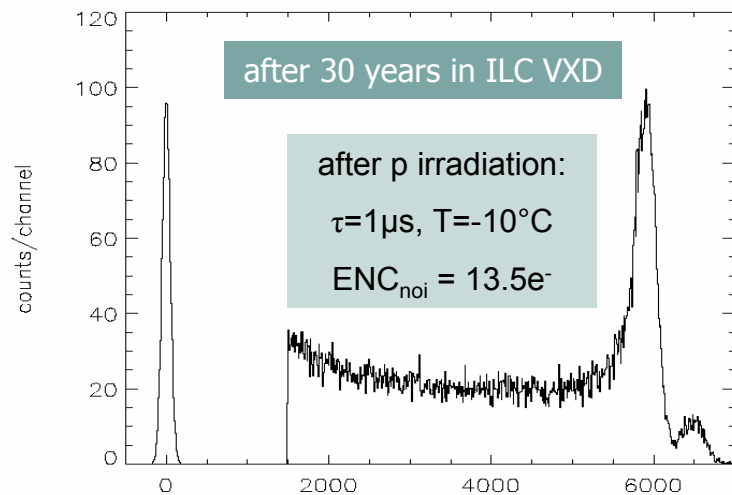
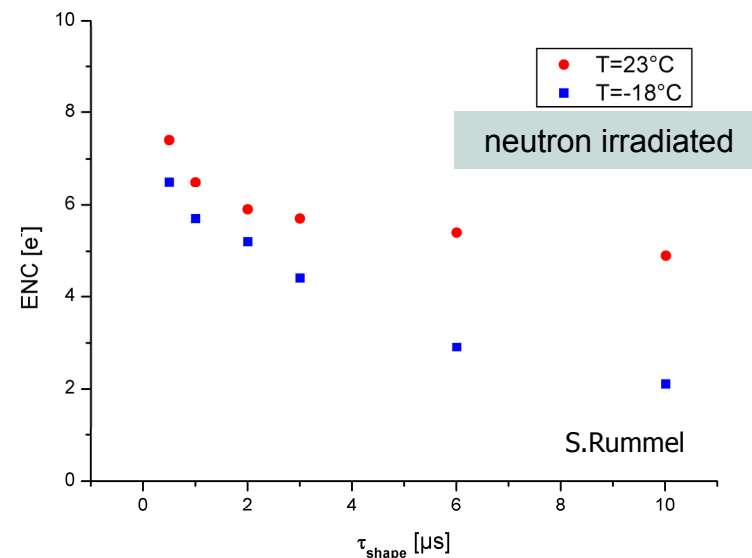
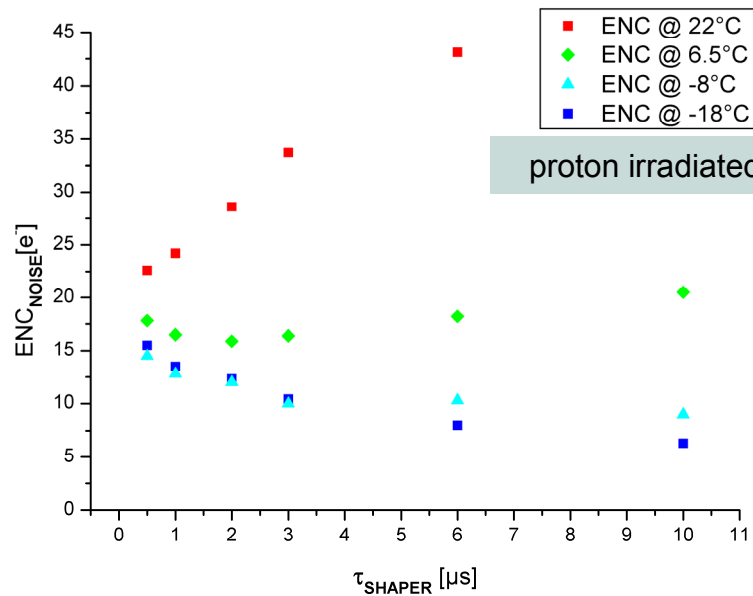
913 krad ^{60}Co

$V_{\text{thresh}} \approx -4.0\text{V}$, $V_{\text{gate}} = -6.0\text{V}$
 $I_{\text{drain}} = 40 \mu\text{A}$
 time cont. shaping $\tau = 10 \mu\text{s}$

Noise ENC = 3.5 e⁻ (rms)

at $T > 23 \text{ degC}$

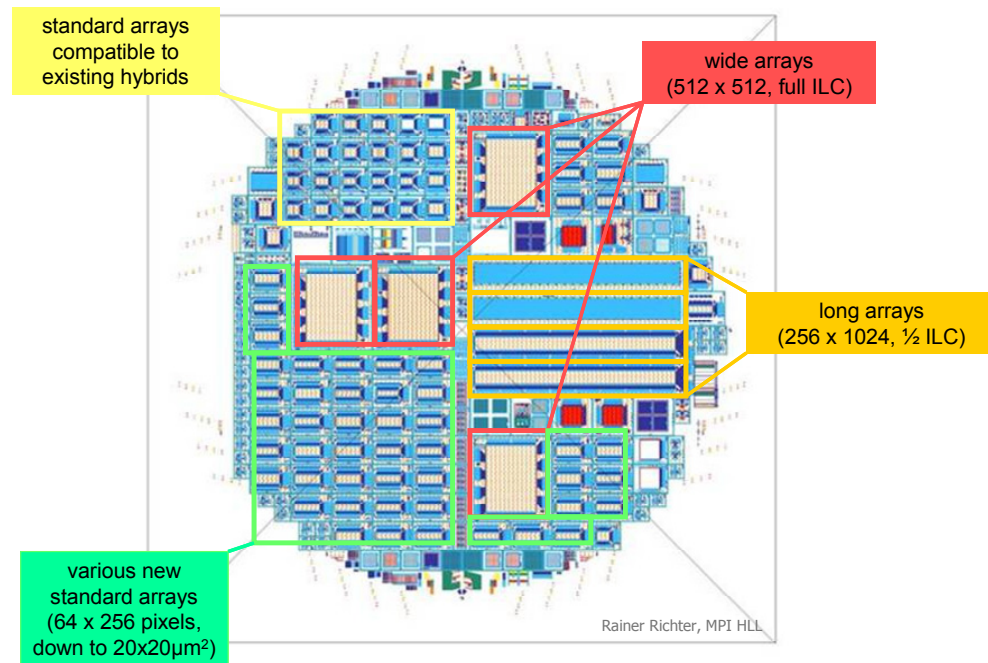
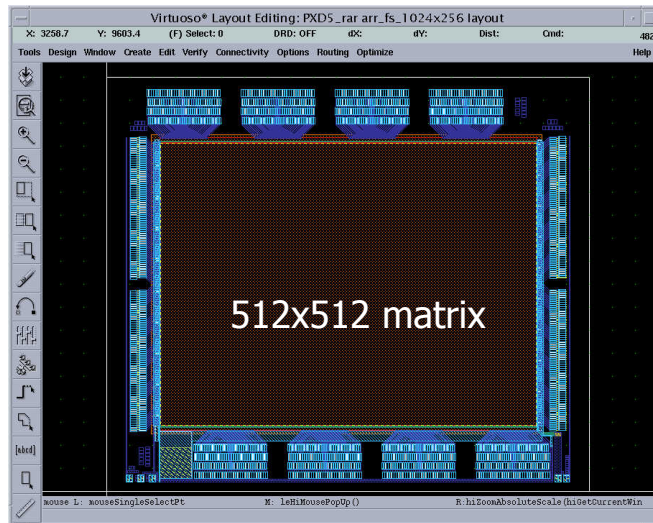
● Spectroscopic Performance - p and n irradiation



● New DEPFET Generation 'PXD5'

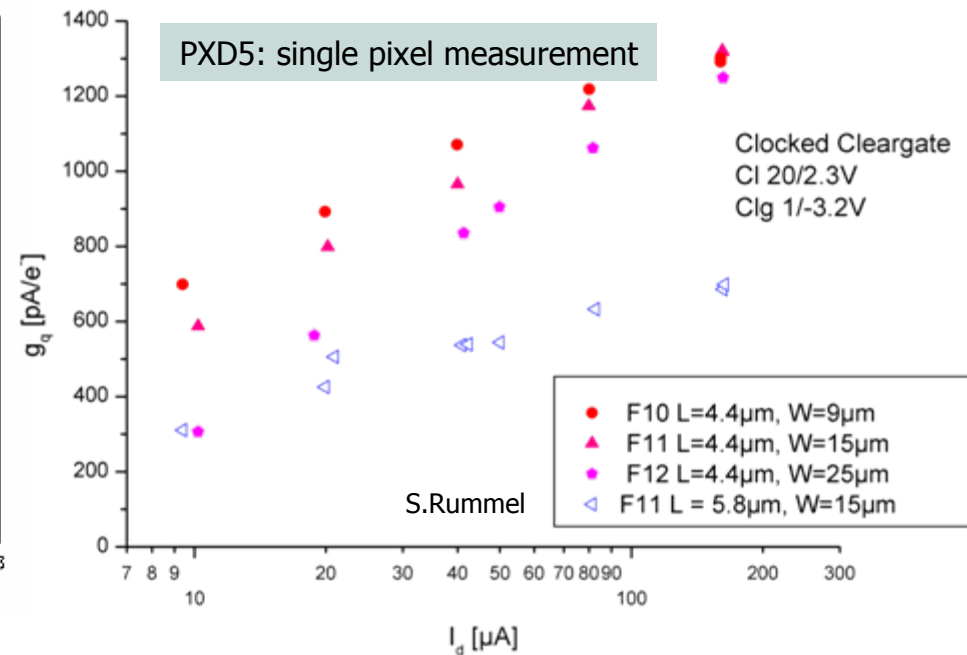
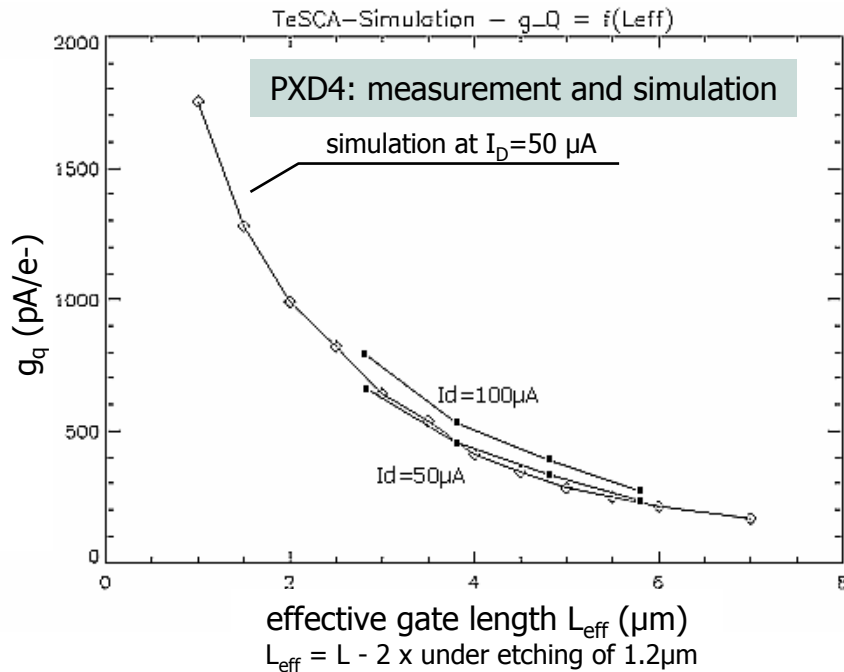
- Mostly use 'baseline' linear DEPFET geometry
- Build **larger matrices**
 - Long matrices (full ILC drain length)
 - Wide matrices (full Load for Switcher Gate / Clear chips)
- Try new DEPFET variants:
 - reduce **clear voltages** (modified implantations, modified geometry)
 - Very **small** pixels ($20\mu\text{m} \times 20\mu\text{m}$)
- Increase internal **amplification** (g_q)

Production finished
June 2007



Internal amplification g_q

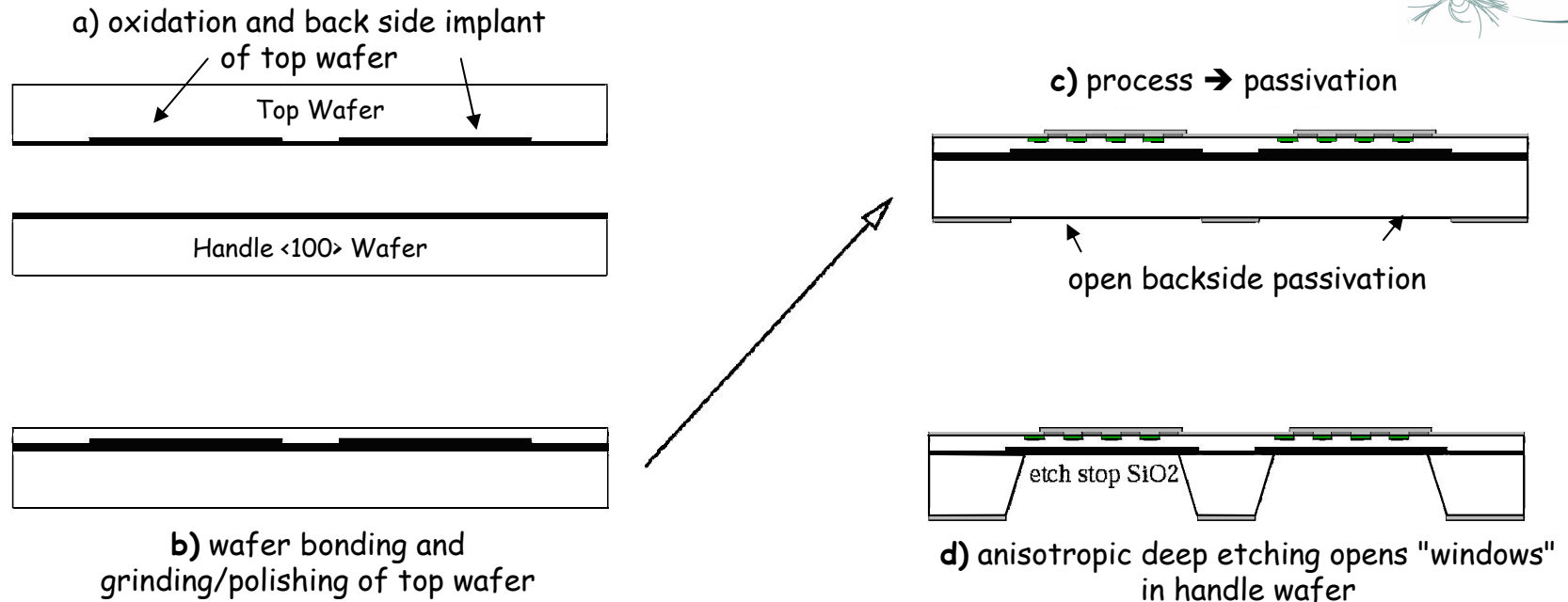
$$g_q = \frac{dI_D}{dQ} = -\frac{\mu_p}{L^2} (V_{GS} - V_{th}) \quad (\text{neglecting short channel effects})$$



As long as noise is dominated by r/o chip \rightarrow S/N linear with g_q

PXD4 has $L=6 \mu m$, some matrices in PXD5 have now $L=4 \mu m \rightarrow$ expect factor 2 better S/N

● Thinning Technology



Compatibility with the main production line tested

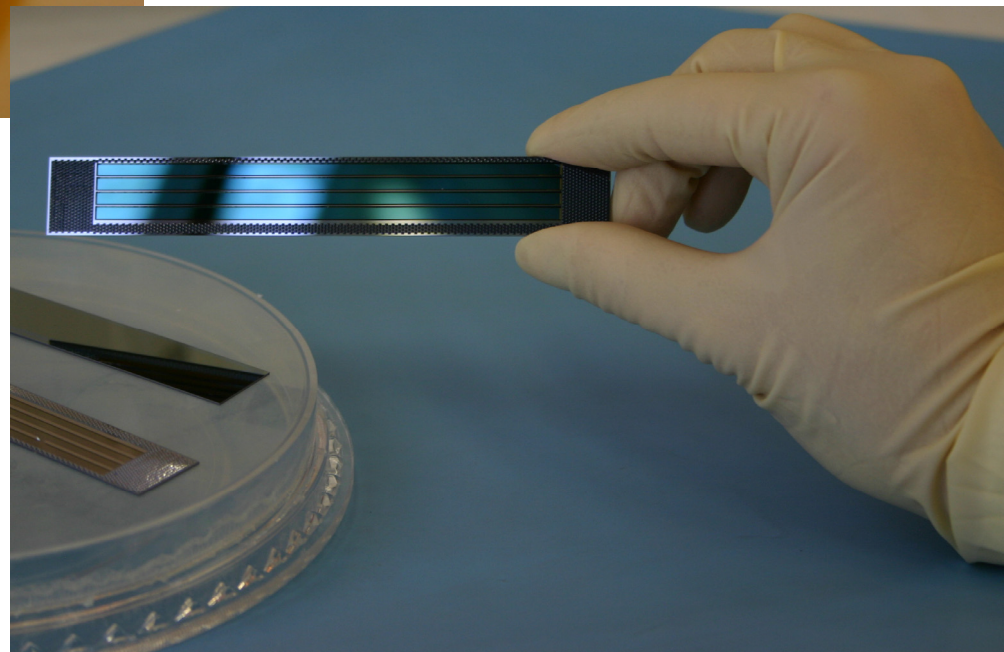
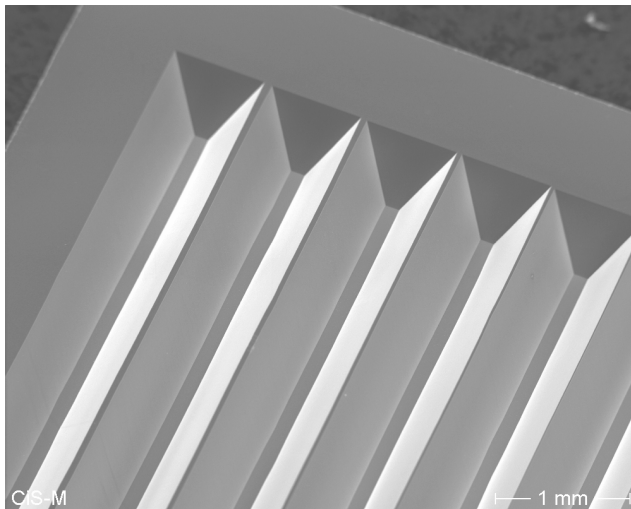
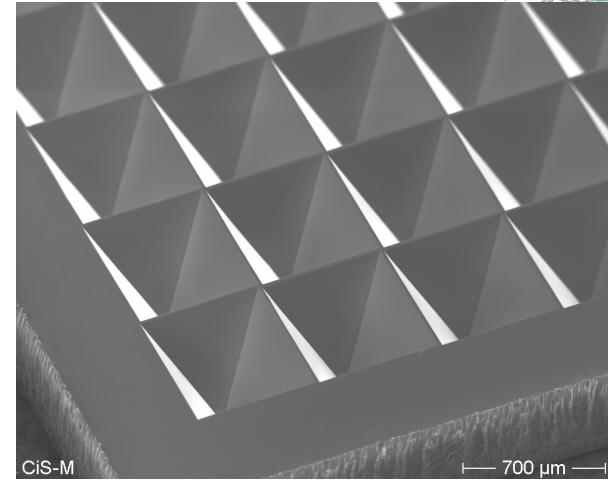
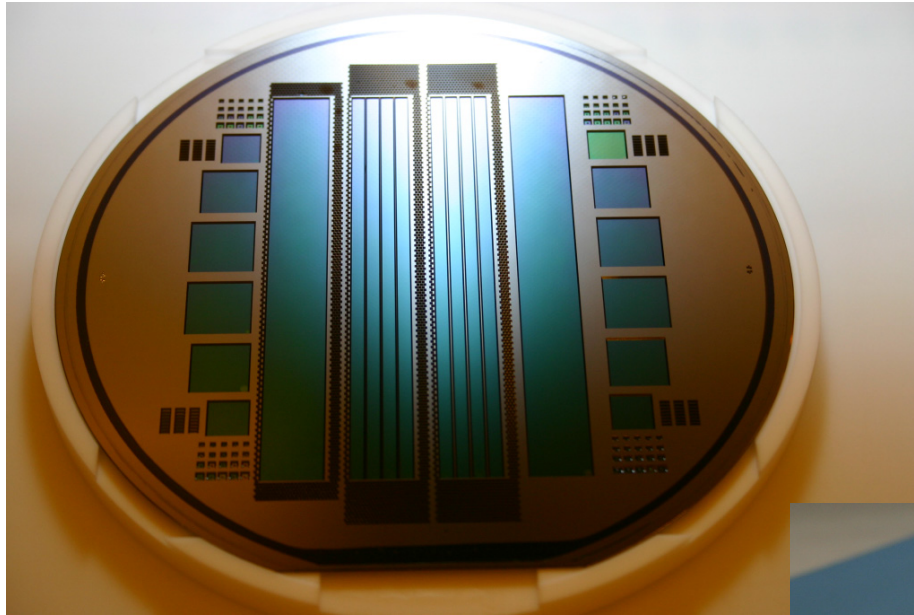
So far:

- : mechanical samples
- : test structures (diodes) on SOI wafers

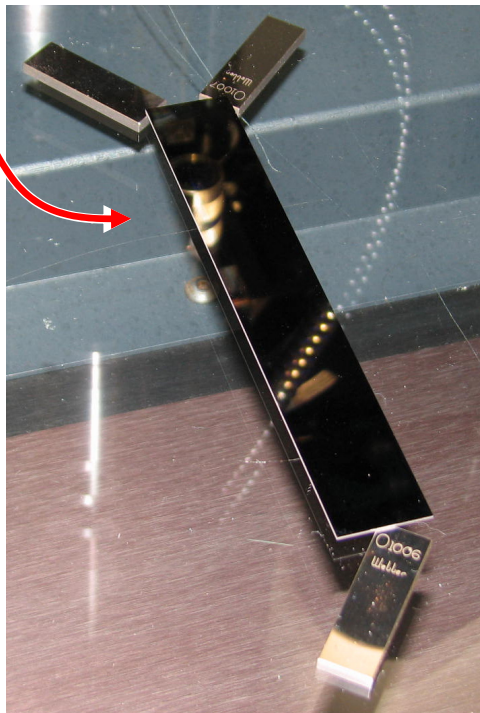
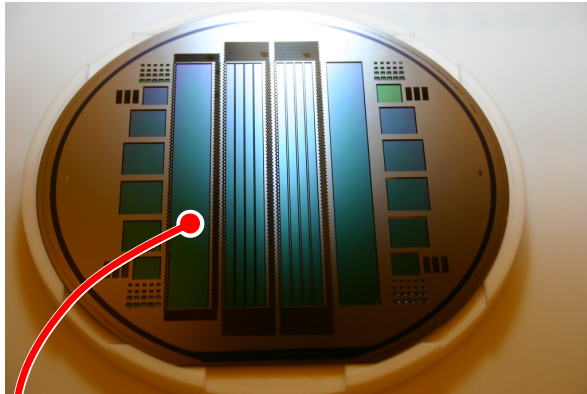
The technology found its way into other projects:

- : production of thin (75 and 150 μm) ATLAS pixel sensors for sLHC
- : first production of SIMPL Geiger-mode APDs on 70 μm top layer

● Thinning : mechanical samples



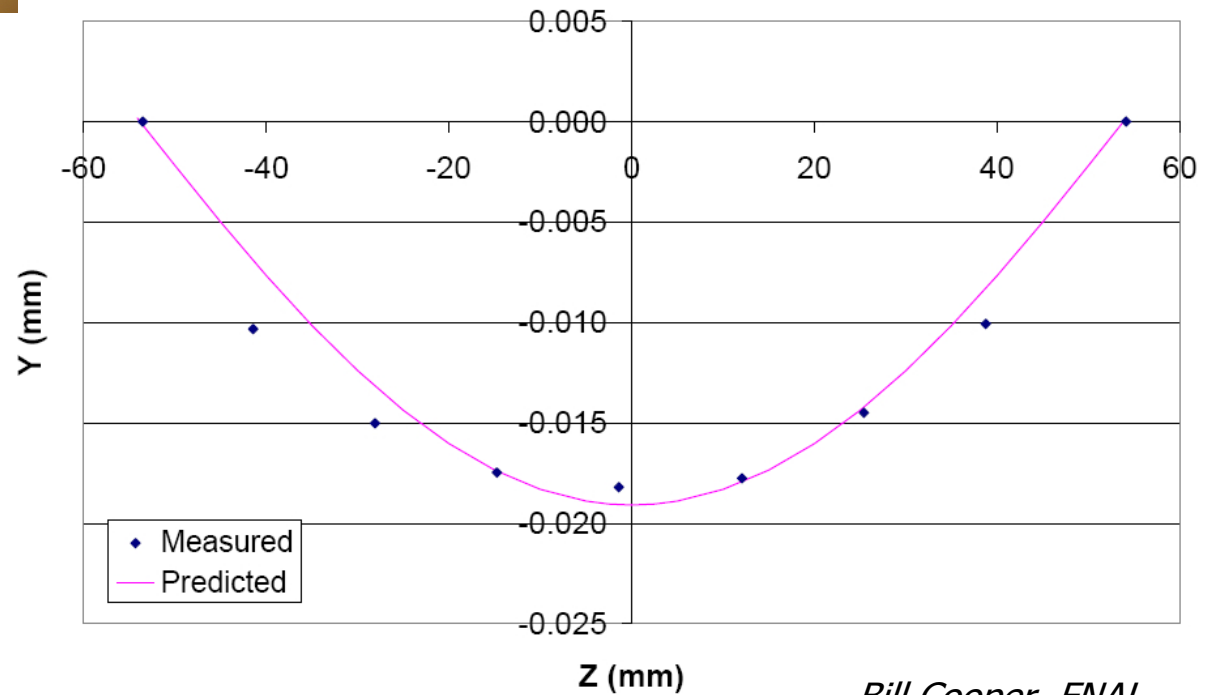
● Thinning : mechanical samples



full size 1st layer module:

100x13 mm² sensitive area, 50 μm thin, 400 μm frame,
no support bars

→ 20 μm deflection due to gravity



Bill Cooper, FNAL

● In Summary



- 2007 was an eventful year for the ILC
 - : Release of the Reference Design Report (RDR)
 - : Call for LOIs for the detectors
 - : Start of a new optimization studies for all concepts
 - : Detector R&D Panel had a series of reviews
 - : Tracking, Calorimetry, and Vertexing

- MPI is an active player in this project
 - : Design and production of DEPFET sensors for the VXD
 - : Involvement in the Calorimeter initiated
 - : Software development and detector optimizations

- Highlights 2007
 - : New DEPFET production finished, currently under test
 - : Software tools (Simulation and Reconstruction) developed at MPI now widely used within the ILC Community

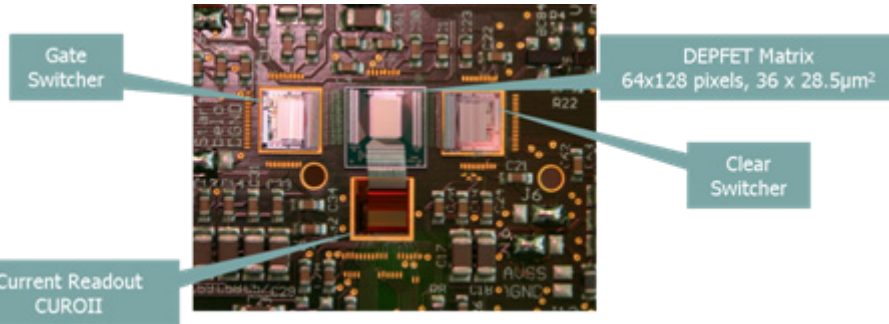
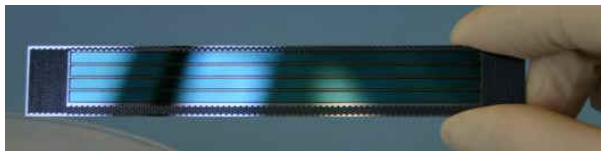
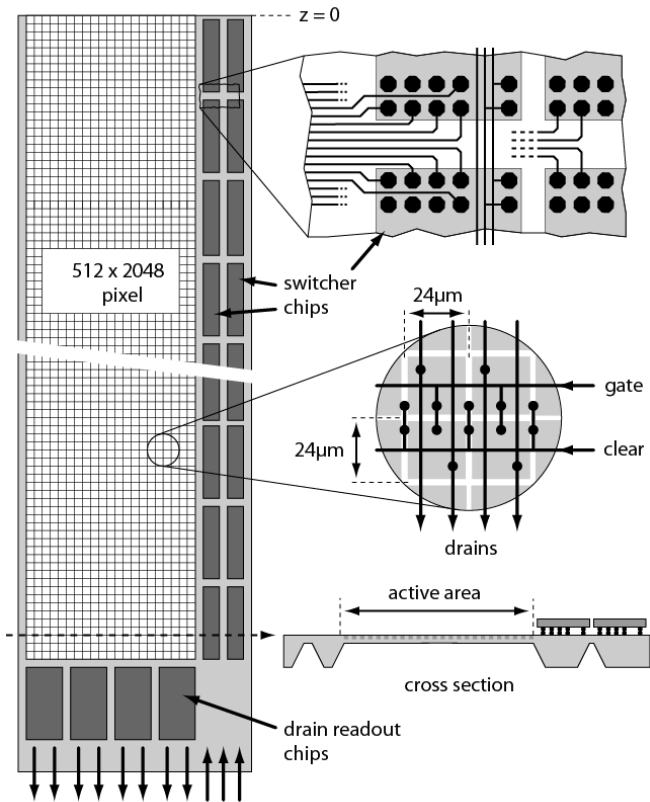
People involved in this Project:

Allen Caldwell, Xun Chen, Ariane Frey, Christian Kiesling, Andreas Moll, Vassiliy Morgunov, Kolja Prothmann, Alexei Raspereza, Ron Settles, Frank Simon, Ladislav Andricek, Hans-Guenther Moser, Jelena Ninkovic, Rainer Richter, Stefan Rummel

- Backup slides follow....
-



● In Summary: Achievements



- ✓ Prototype System with DEP-FETs (450µm), CURO and Switcher
- ✓ test beam @ CERN:
 - ✓ $S/N \approx 110$ @ 450 µm \leftrightarrow goal $S/N \approx 20-40$ @ 50 µm
 - ✓ sample-clear-sample 320 ns \leftrightarrow goal 50 ns
 - ✓ s.p. res. 1.3 µm @ 450 µm \leftrightarrow goal ≈ 4 µm @ 50 µm
- ✓ Thinning technology established, thickness can be adjusted to the needs of the experiment (~ 20 µm ... ~ 100 µm)
- ✓ radiation tolerance tested with single pixel structures up to 1 Mrad and $\sim 10^{12}$ n_{eq}/cm²
- ✓ Simulations show that the present DEP-FET concept can meet the challenging requirements at the ILC VXD.

● In Summary: Prospects



- ✓ Production of 2nd iteration DEPFETs was finished summer 2007,
- ✓ higher internal amplification demonstrated ($g_q=0.4nA/e \rightarrow$ almost 1 nA/e), better S/N
- ✓ New Switcher3 chips tested and functional
- ✓ New r/o chips DCD designed for read-out of large matrices are under test

Power Consumption for the ILC VXD (baseline design) with these new chips

layer 1: 8 ladders, 4096x512 pix./ladder $\rightarrow \sim 12W/ladder \rightarrow \sim 100 W/layer$

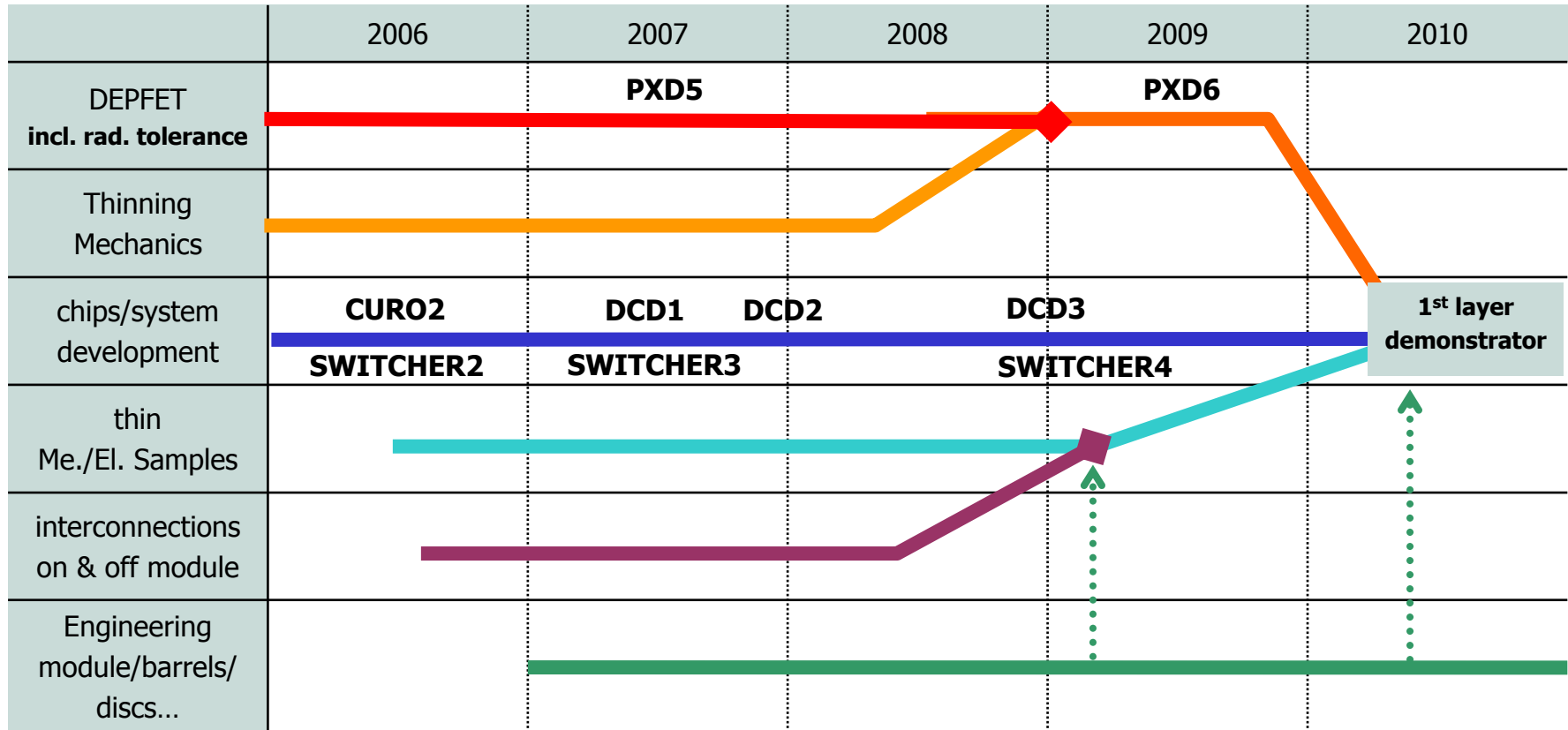
layer 2-5: 56 ladders, 10496x928 pix./ladder $\rightarrow \sim 21W/ladder \rightarrow \sim 1200 W/ 4 layers$

$\rightarrow 1300 W \rightarrow$ **6.5 ... 13 W** with pulsed power operation 1/200 - 1/100

About 90% of the power is dissipated at the ladder ends (r/o chips DCD)

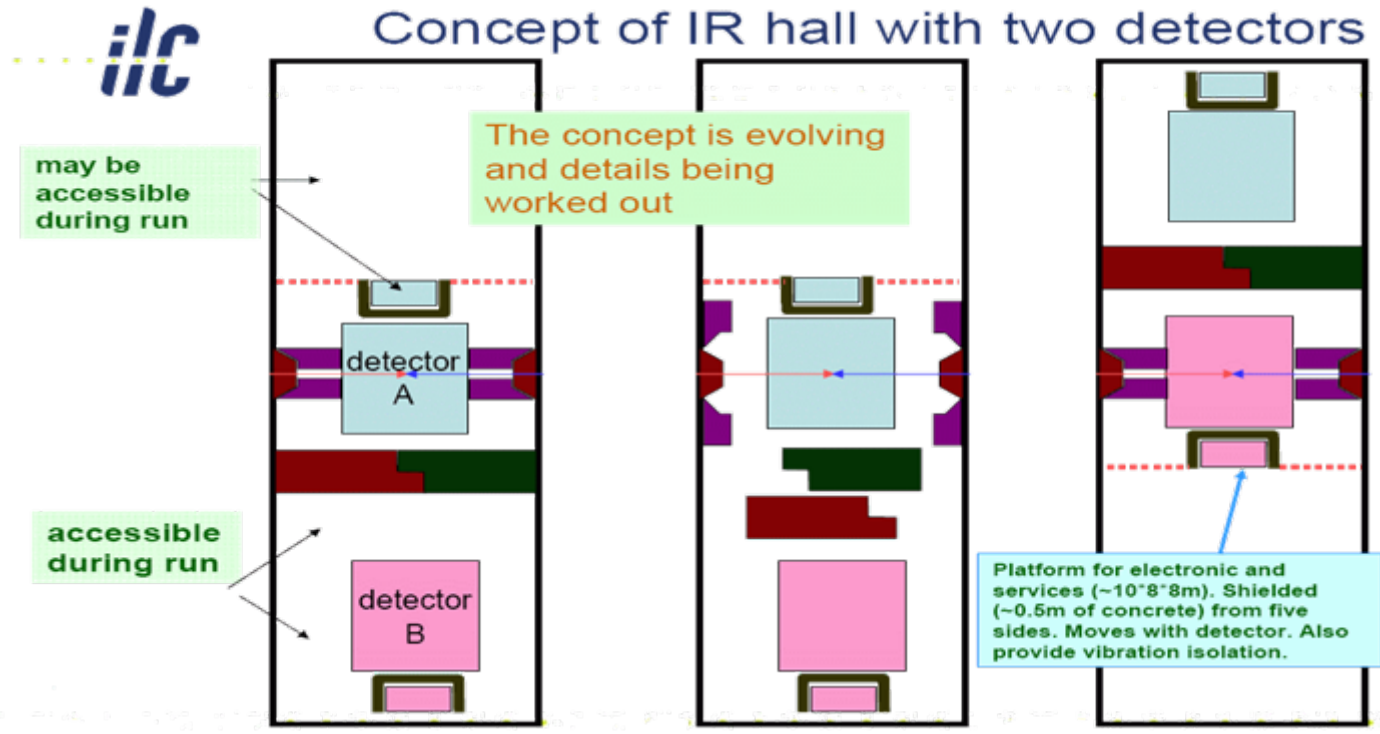
Based on the experience made with the prototype system, we are confident that the DEPFET in the **present baseline design** can meet the requirements at the ILC VXD. In this concept, with the read out at the end of the ladders, the biggest challenge is the required row rate and the capacitive load at the f/e inputs. There are several ideas how to increase the "head room" in this respect, one of those being the use of the emerging 3D technologies. This will be one of the future R&D directions.

●towards a thin demonstrator (in baseline design)



- ✓ ASIC production: UMC, AMS, IBM, TSMC.... use the best available process
- ✓ DEP FET prototyping and series production of the sensors at the MPI Halbleiterlabor

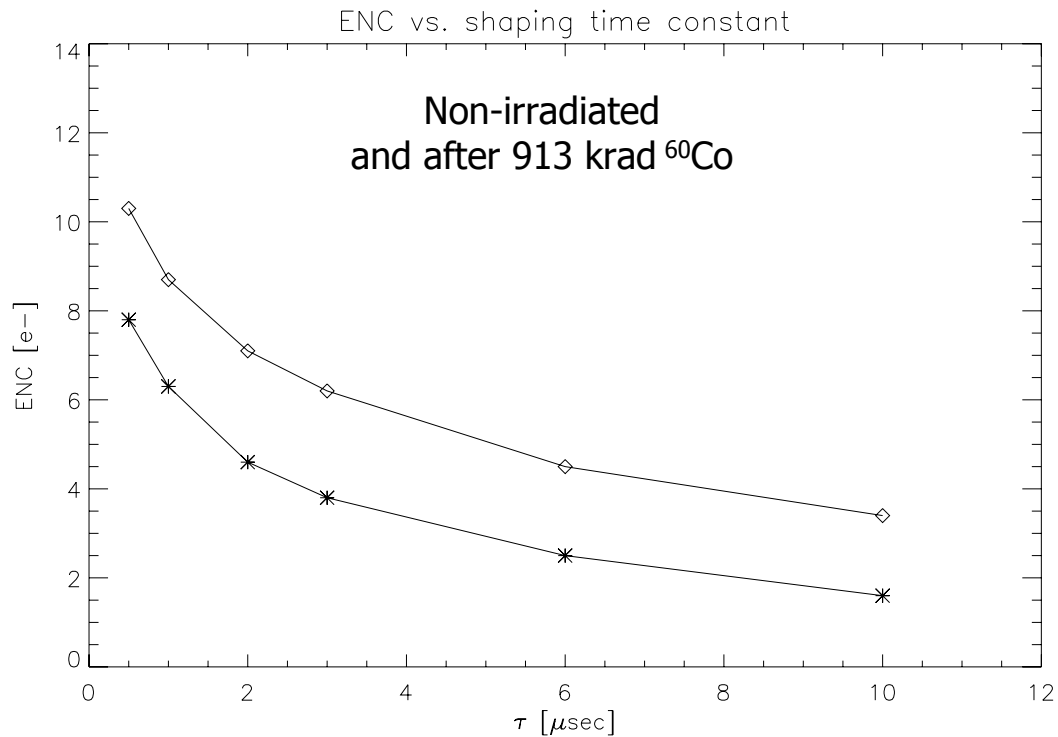
- One IR, but two Detectors → Push-Pull



Task force formed by WWS and GDE: The first quick conclusion is

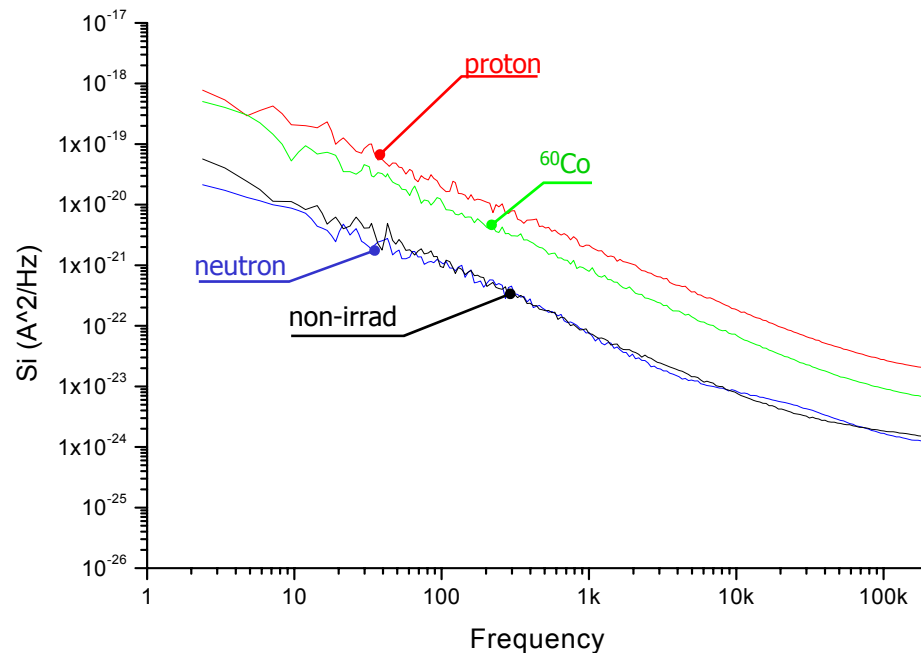
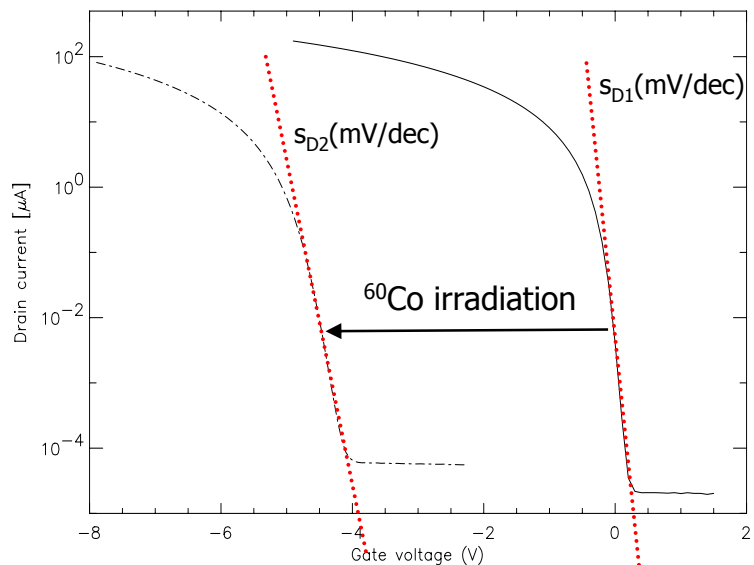
- : no show stoppers
- : but needs careful design...
- : keep 2 IRs as alternative (!)

● Noise vs. shaping time τ - ^{60}Co irradiation



$$ENC = \sqrt{\underbrace{\alpha \frac{8kTg_m}{3g_q^2} \frac{1}{\tau}}_{\text{Therm. noise}} + \underbrace{2\pi a_f C_{tot}^2}_{1/f} + \underbrace{qI_{Leak}\tau}_{I_L}}$$

● Subthreshold current → Interface trap density → 1/f noise



$$\Delta N_{it} = \frac{C_{ox}}{kT \cdot \ln(10)} \cdot (s_{D2} - s_{D1})$$

irradiation	TID / NIEL fluence	Δs (mV/dec)	ΔN_{it} (cm ⁻² ·eV ⁻¹)
gamma ⁶⁰ Co	913 krad / ~ 0	88	1.6 · 10 ¹¹
neutron	~ 0 / 2.4x10 ¹¹ n/cm ²	~ 0	~ 0
proton	283krad / 3x10 ¹² n/cm ²	230	4.2 · 10 ¹¹

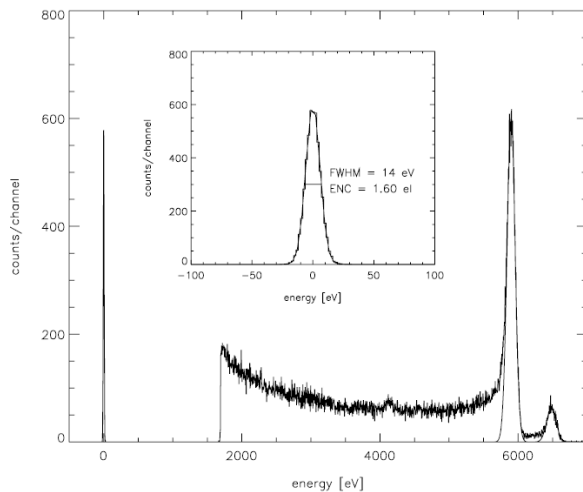
Lit: ~ 10¹²-10¹³ cm⁻²·eV⁻¹ for 200nm gate oxide

● Bandwidth and Noise

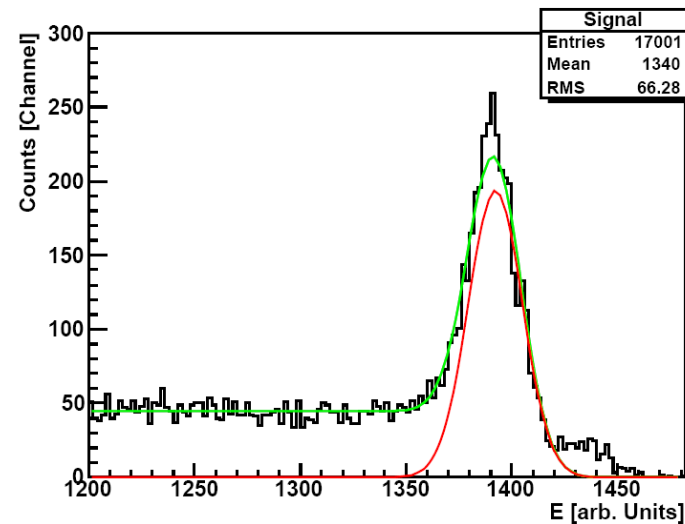
High readout speed → high bandwidth → short shaping times

$$ENC = \sqrt{\alpha \frac{8kT g_m}{3g_q^2} \frac{1}{\tau} + 2\pi a_f C_{tot}^2 + qI_{Leak}\tau}$$

Measurements of a single pixel with an external high bandwidth amplifier



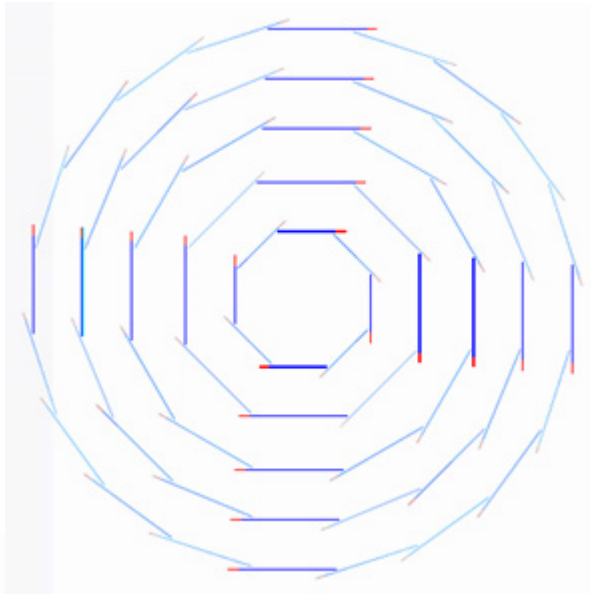
1.6 e ENC at t=10 μs



40 e ENC at t=20ns (50MHz)

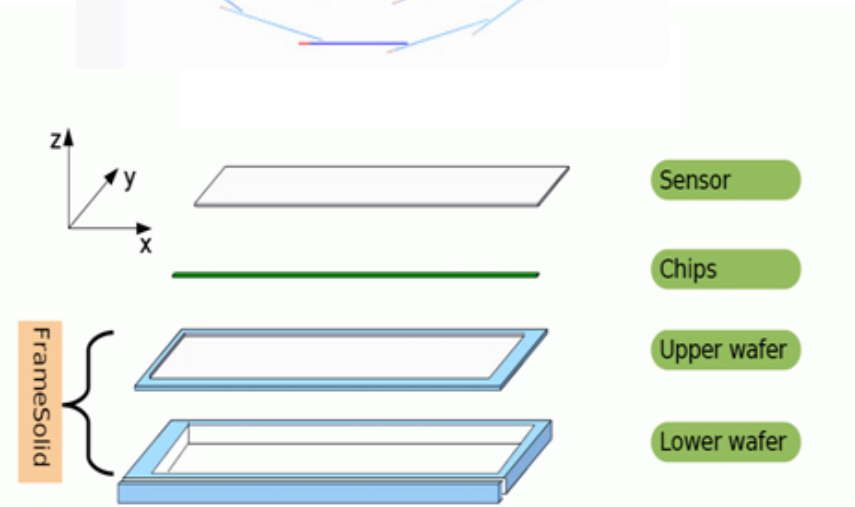
Intrinsic DEPFET noise sufficiently low for high speed operation at ILC

Simulation: LDC Geometry description

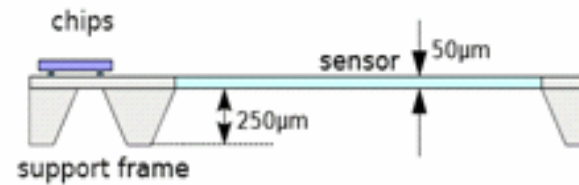


Sensitive layer thickness = $50\ \mu\text{m}$
Pixel size = $25 \times 25\ \mu\text{m}^2$

	Radius (cm)	Ladders	Length (cm)
1	1.5	8	10.0
2	2.6	8	2×12.5
3	3.8	12	2×12.5
4	4.9	16	2×12.5
5	6.0	20	2×12.5



→ LDC ladders with support frames

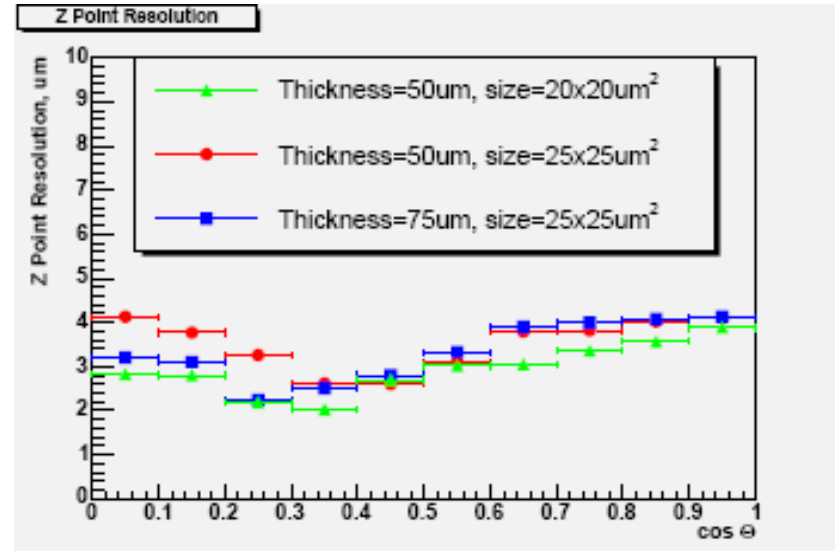
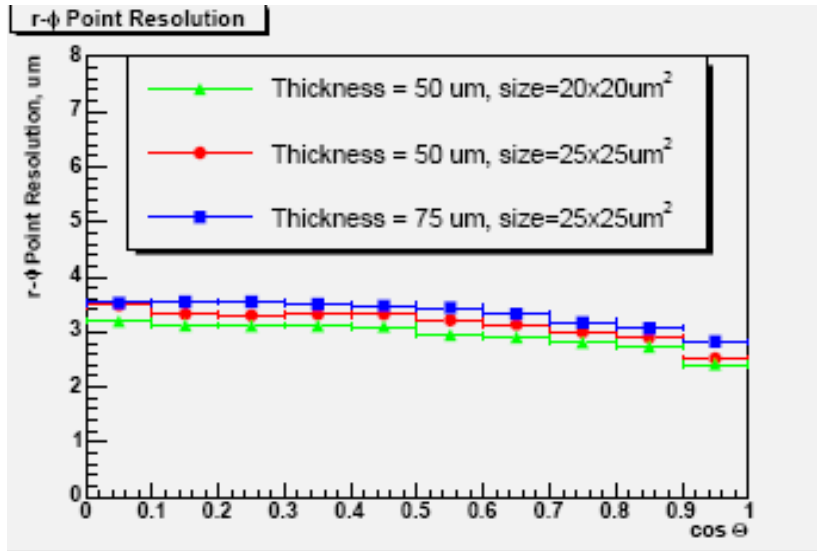


Material up to first layer : beam pipe ($500\ \mu\text{m}$ beryllium)

MC Studies



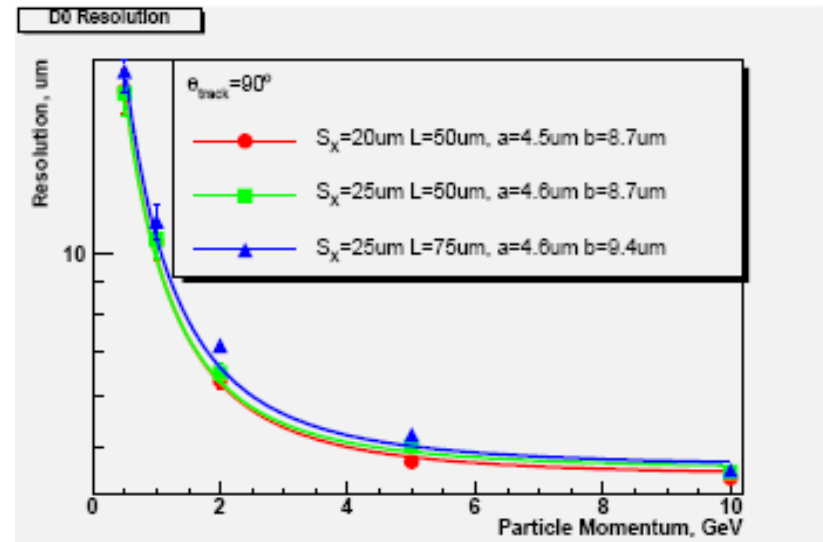
Spatial resolution for 50 mm thick 25 x 25 mm² pixels: <3.5 mm (r-φ), <4.0 mm (z)



Impact parameter resolution
(5 layers, frames, 500 mm Be beam pipe)

$$\sigma(\text{IP})_{r-\phi} = 4.5 \mu\text{m} \oplus \frac{8.7 \mu\text{m}}{\rho(\text{GeV}/c) \sin^{3/2}\theta}$$

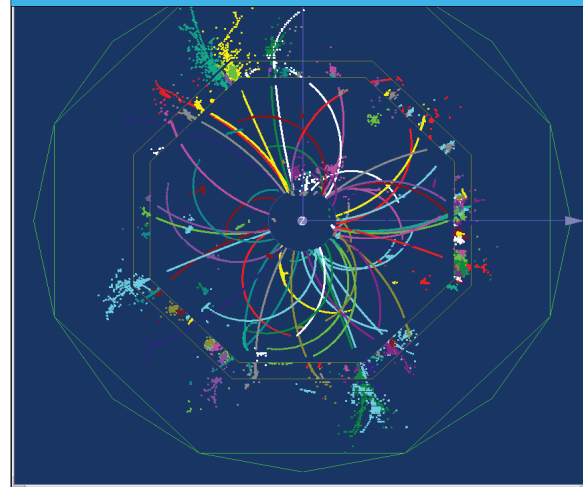
ILC requirements fulfilled



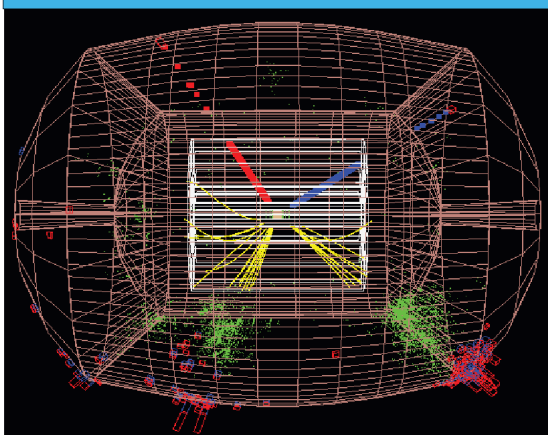
Detector Concepts

- SiD, LD & GLD driven by pflow, differ by size and B field
 - SiD/LDC/GLD : $R_{\text{solenoid}} = 3.3/3.8/4.4 \text{ m}$, $B = 5/4/3 \text{ T}$
- high granularity sandwich calorimeters (few cm^2 cell size) efficient shower separation & individual particle reconstruction in multi-jet events
- Pixelized VXD (5 layers, innermost layer at 1.5cm from IP)
- Central tracking : gaseous detector (TPC) : LDC & GLD; double-sided silicon strip layers : SiD
- Instrumented return yoke as muon detector

$tt \rightarrow 6\text{jets}$ @ 500 GeV in LD



$ZH \rightarrow \mu\mu qq$ in 4th detector



- 4th Concept : emphasis on calorimetry
- reconstruction of jet as a whole object with dual readout calorimeters; projective copper towers with embedded quartz and scintillating fibers enable to measure separately EM energy fraction within showers and thus improve energy resolution
- The same concept of tracking system as in LDC & GLD

● PiN Diodes on thin Silicon

