

# ASIC monitoring and SEU correction

PXD Workshop

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# ASIC monitoring

- Configurable ASICs of PXD are DHP and DCD
- Both provide internal mechanisms to prevent single event upsets
- Configuration is applied via JTAG from DHE/DHI during TURNINGON
  
- In May 2020 a monitoring of register was installed at KEK
  - Read 3 registers of the DHP (DCD is write-only) every 20s
  - Compare all PVs with its previous value and ConfigDB
  - Logged as warnings
    - later manually pushed to BIIPXDH-554

# ASIC monitoring

- In nearly all cases no changes in occupancy were visible
- Some configuration flips could be addresses to occupancy spikes
- After detection the register was reset by an expert some time later or automatically when PXD was power cycled (VXD abort, etc.)
  
- On 2022-04-06 we observed multiple changes by module 1.4.2 only in DHP4, but happened for consecutive read out cycles
  - most likely some issue with JTAG communication
  - happened again one day later with DHP2 of same module
  - fixed by power cycle of this module

BIIPXDO-423

# SEU correction

- Full rewrite of monitoring logic was necessary
- Changed DHP registers are reverted afterwards
- Only the DHP with changed registers is rewritten
- Additional information to the shifter if the register was recovered
- In case of multiple changes (>10) the module is shut down directly
  - From CR side, it looks like a TRIP
  - The module is ramped back to PEAK with fresh configuration

# SEU correction

- DCDs configuration can be rewritten
- But the JTAG chain is altered, which can cause OVPs when not correctly timed with DHP temperature monitoring
- Including the switchers (always connected via DCD 1 or 4) can induce noise
  
- All read and write commands wait for a temperature read out cycle (5 seconds interval, 4 seconds for completion)
- Additional delay afterwards in order to read out all registers of all modules not at the same time to prevent JTAG communication spikes

# SEU correction

- New monitoring released in April 2022
- So far no SEUs detected
- DCD rewriting showed a problem on DHP3 of module 2.4.1
  - DHP link is not alive (missing frame sync signal)
  - Link is recovered automatically
  - other module and their occupancy did not show increased noise
  - Sequence adjustment was introduced to handle each DCD one by one, but the problem remains
- DCD rewriting is remained off

# Future Plans / Considerations

- skip one problematic DCD?
- monitoring of DHP memory to be discussed
  - SEUs in memory seem less likely,  
a change in the switcher sequence should be directly visible