The HV-current Puzzle

L. Andricek, C. Koffmane, J. Ninkovic, R. H. Richter

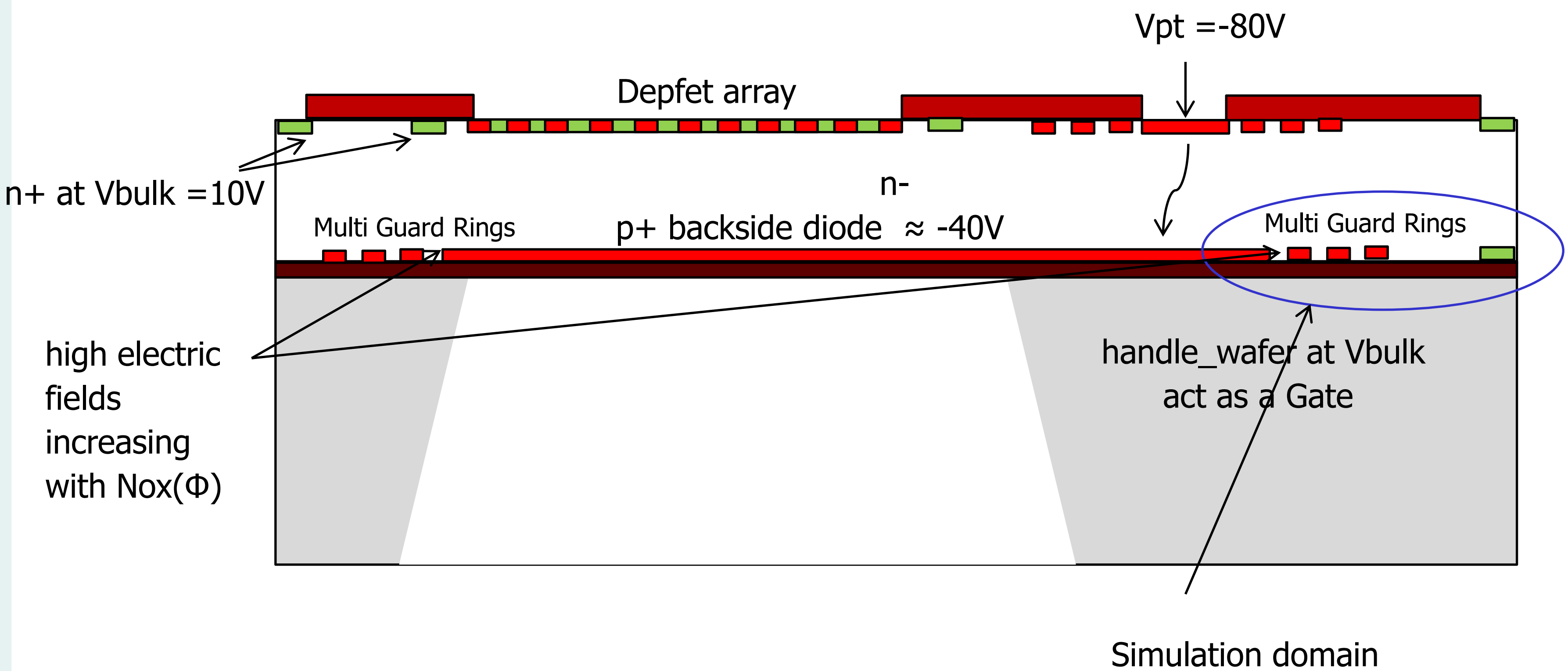
- HV – currents are going up with irradiation at Belle2 and in the Lab.
- Reason for the current increase is Avalanche multiplication (electron-hole pair generation by impact ionization) by high electric fields deduced from the simultaneous increase of bulk current

- Where does it happen?

- Why are more Icemos wafers more affected than Shinetsu ones?

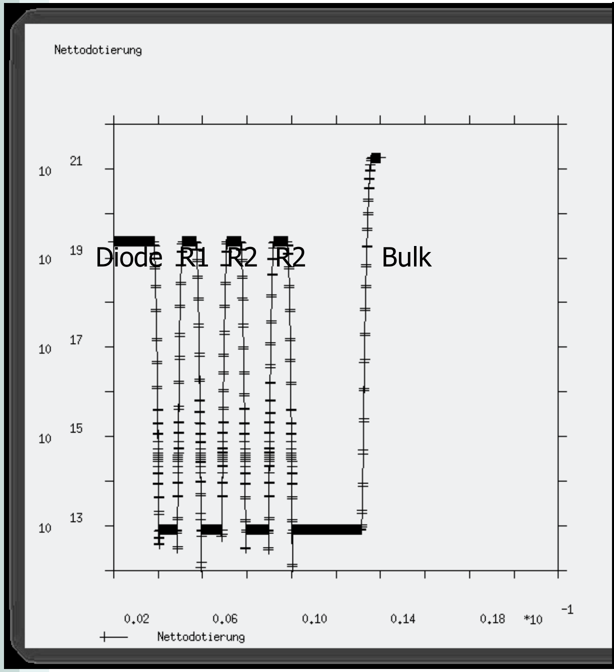
- How can we explain this ?

Module cross section

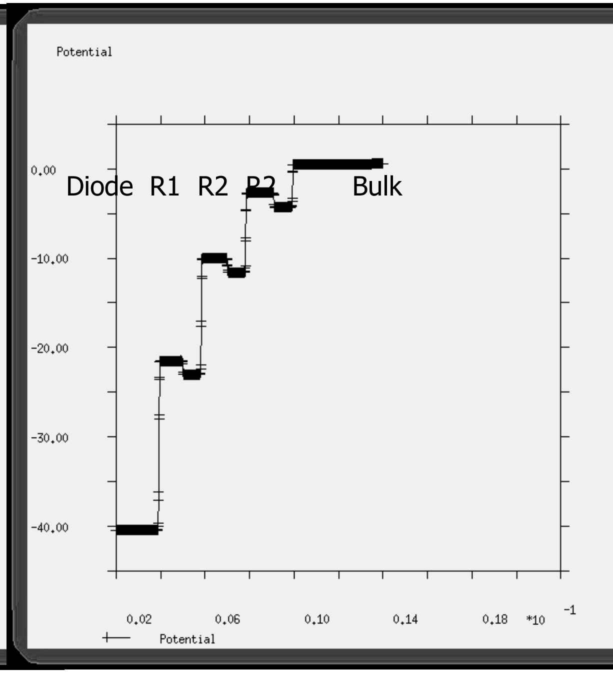


Along the Si-SiO2 Interface at backside

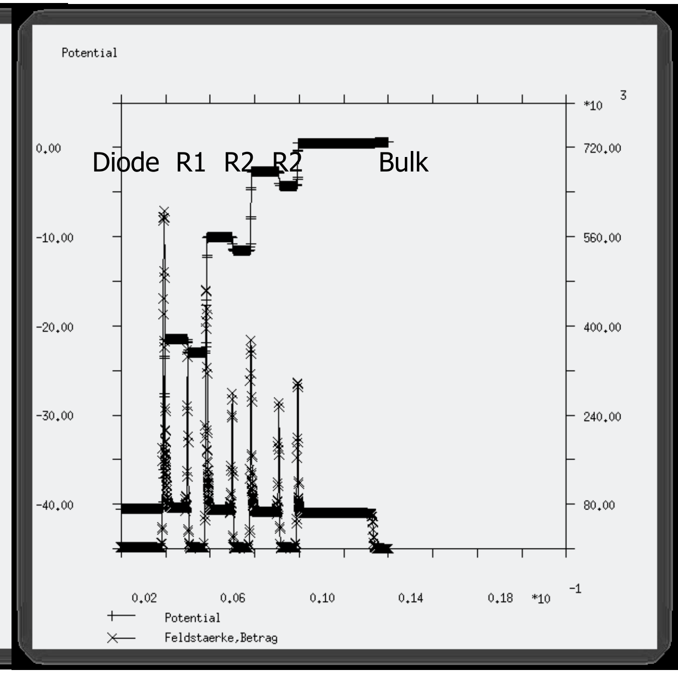
Doping



Potential



Potential and electric field

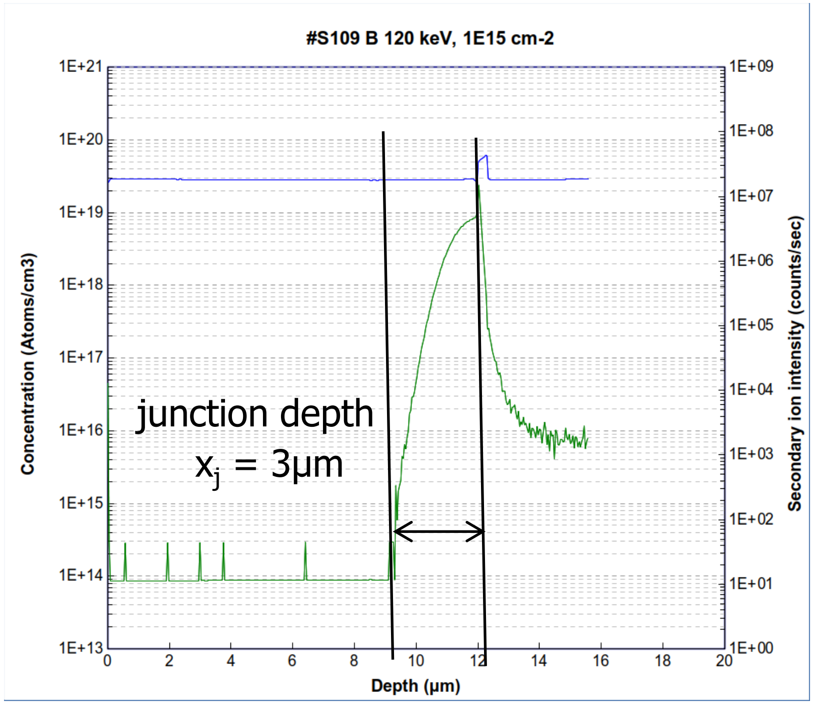


Emax = f(gap, Nox(Φ), Vhandle, 1/tox)

Box oxide thickness: tox Icemos: 560nm
Shinetsu: 350nm

But Icemos modules are much more affected than Shinetsu ones !??
Is the Shinetsu wafer bond oxide so much more rad hard than the Icemos oxide that it even over compensates this dependancy?? But both to wafer oxides where grown at HLL !!?

Dopant depth profile measurement by SIMS*



*SIMS – secondary ion mass spectroscopy

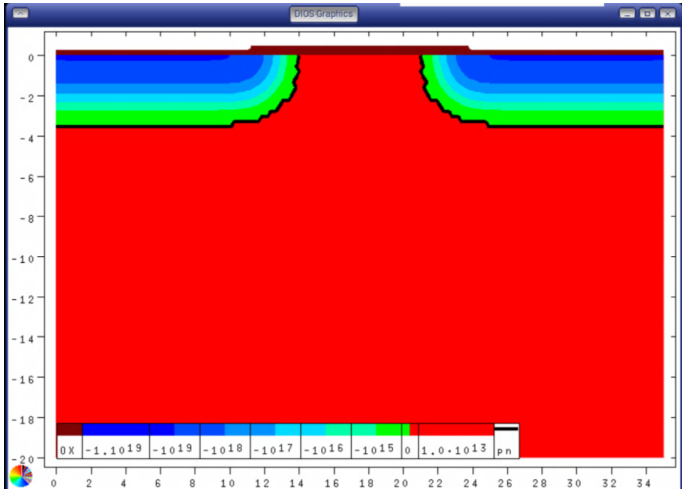
Lateral diffusion not measurable

Simulation T =1100°C, 100min

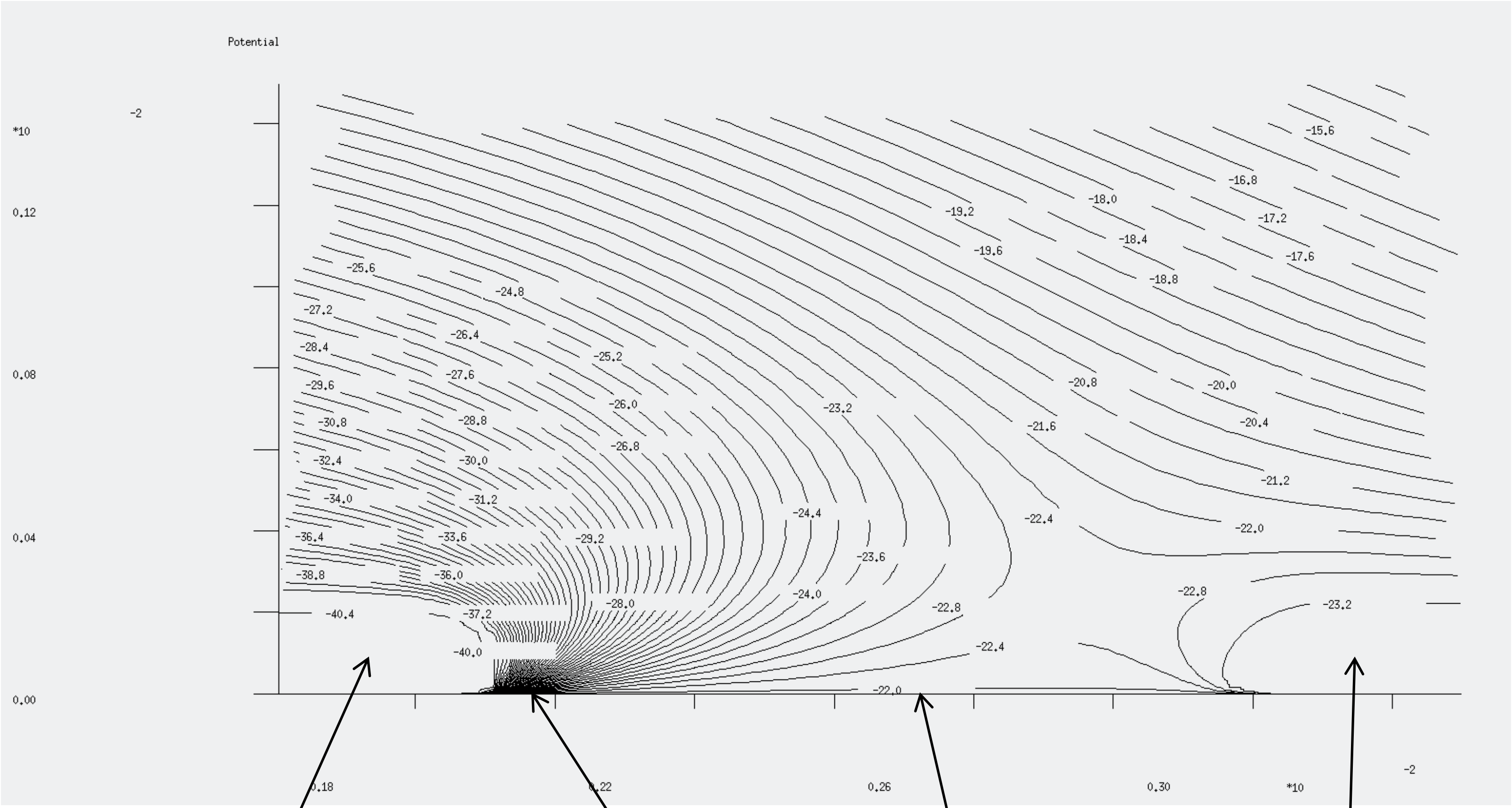
Diode

lateral diff. -> gap reduction 13µm -> 10µm

1. Ring



Potential distribution between diode and first guard ring



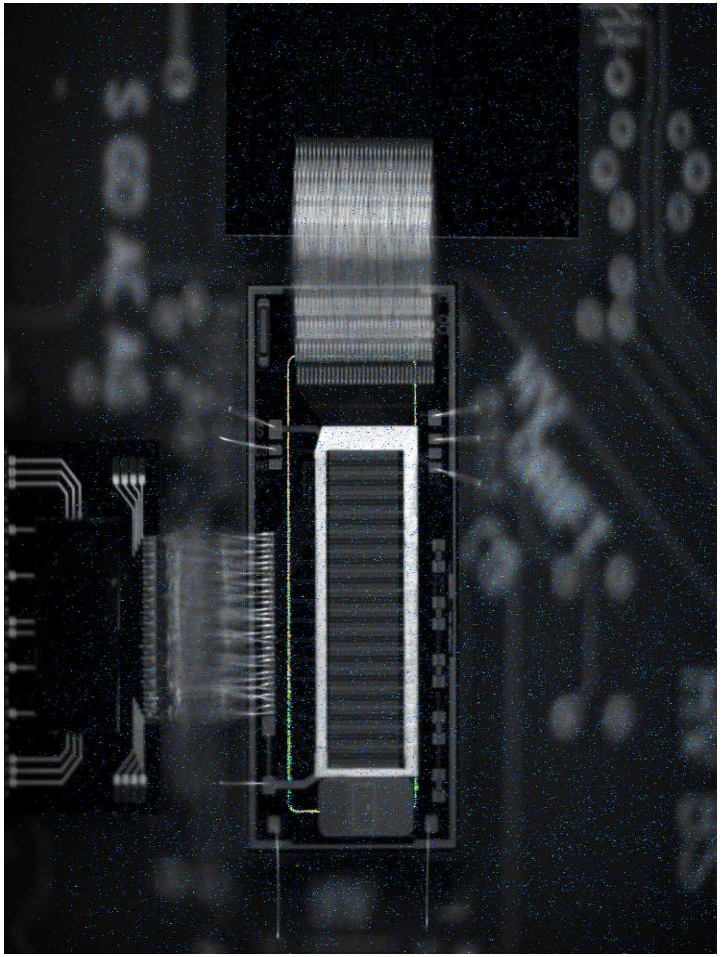
Diode implant -40V

break down position

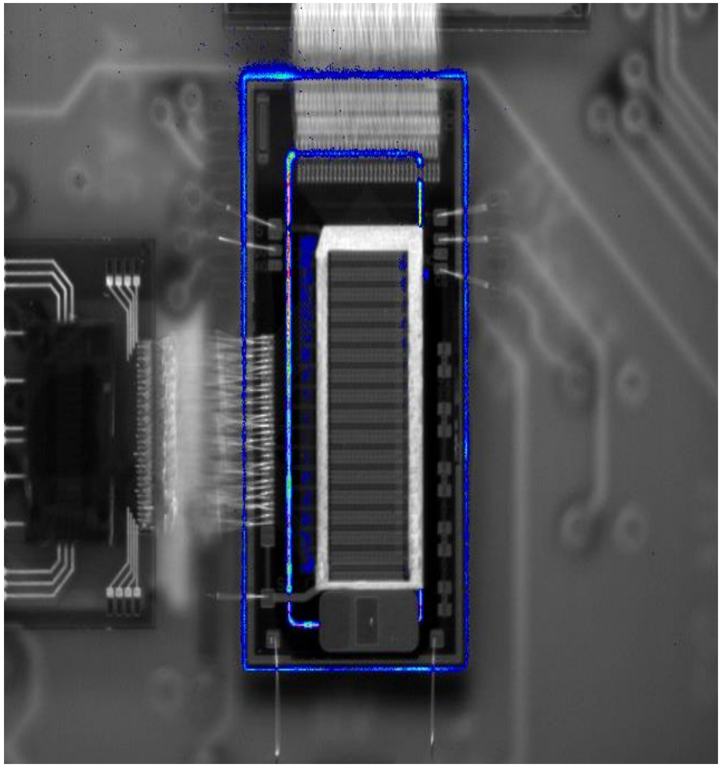
Vif = -22V
electron accumulation layer

1. Guard ring implant -23V

Investigation of an irradiated module with a therma emmision camera Phemos (Hamamatsu) H5.0.29



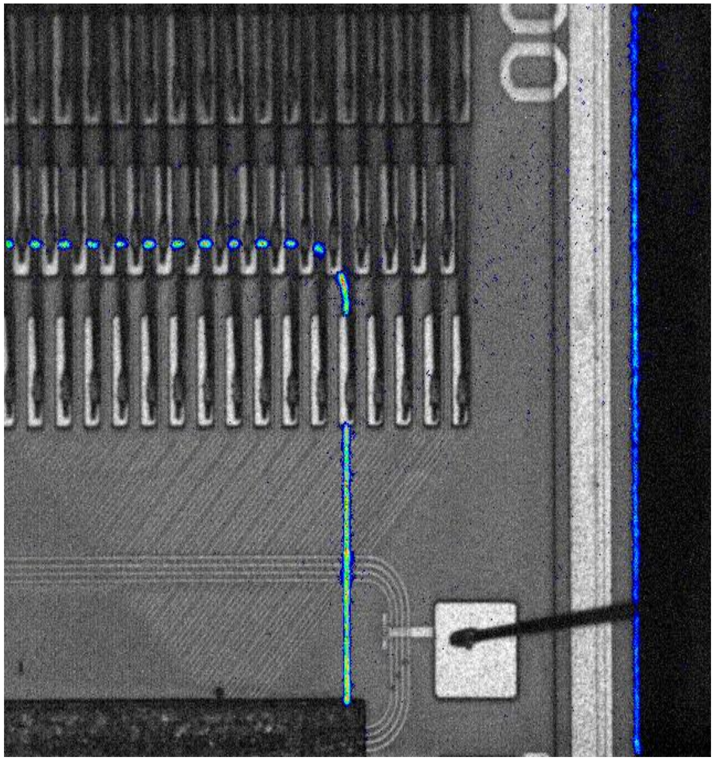
Lens: macro
Camera: Si



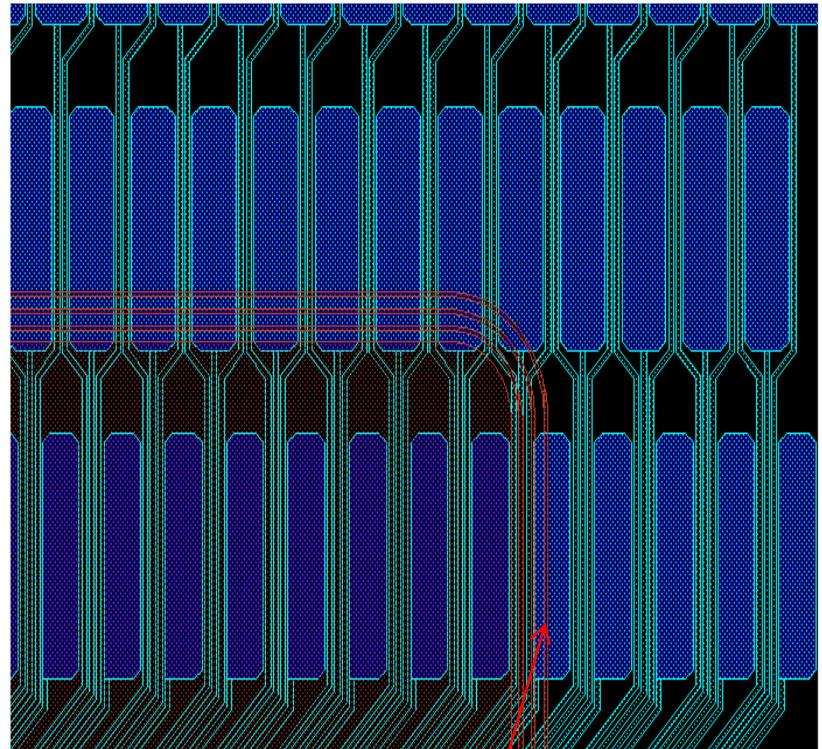
Lens: macro
Camera: InGaAs, integration time: between 60 – 120 s

Bias using the Samtec connector and a breakout board to connect to the SMUs.
SMU1: HV = -105 V; I_hv = 440 µA
SMU2: Bulk = 0V;

H5.0.29



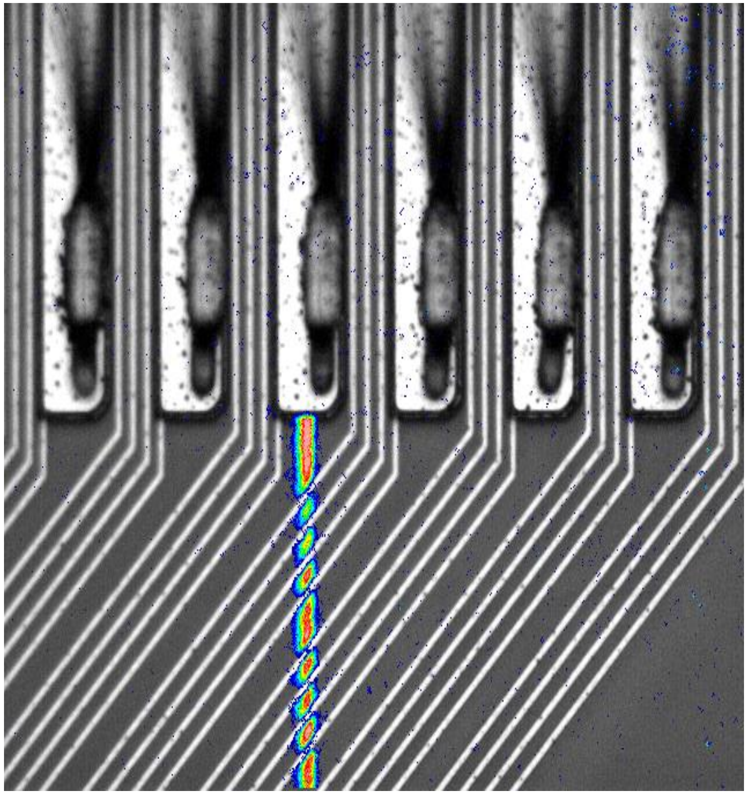
Lens: x5
Camera: InGaAs



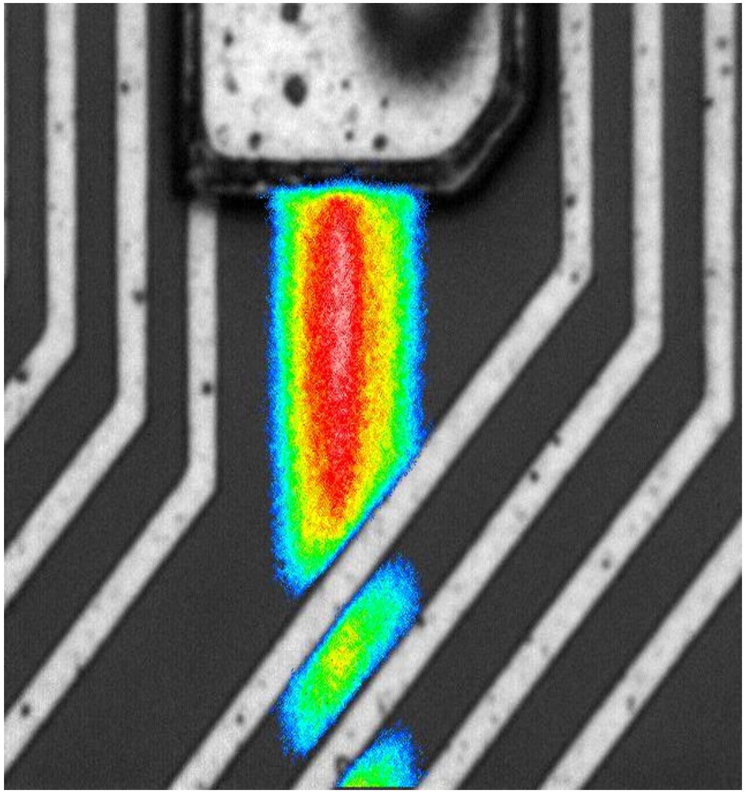
PXD9 layout: poxp & al2n

Break through at **outer most** guard ring!
(against all expectations)

H5.0.29



Lens: x20
Camera: InGaAs



Lens: x100
Camera: InGaAs

What could be the reason ?

Something shorts our guard rings ?

- much deeper implants than expected

  but simulations base on measured doping profiles (SIMS)

  Do the SIMS samples reflect the reality ?

  - different annealing temperatures during wafer bonding?
  - wrong SIMS meas?

  - -> repeat SIMS measurements !

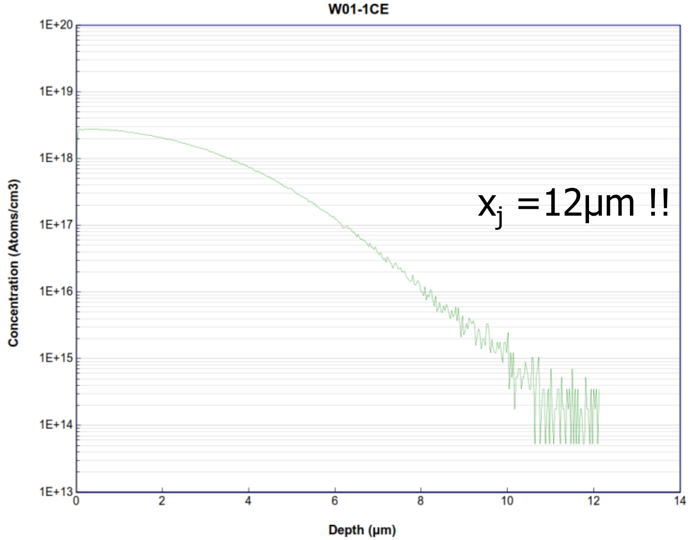
Formation of oxide charges Nox(E) – completely different than expected

much higher charge density at the 3rd guard ring than at the diode ??!

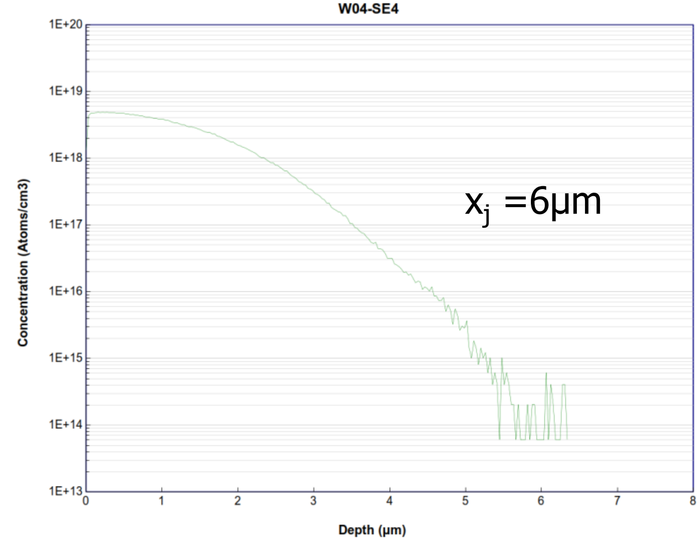
New SIMS measurements – completely different than before

this time from backside surface

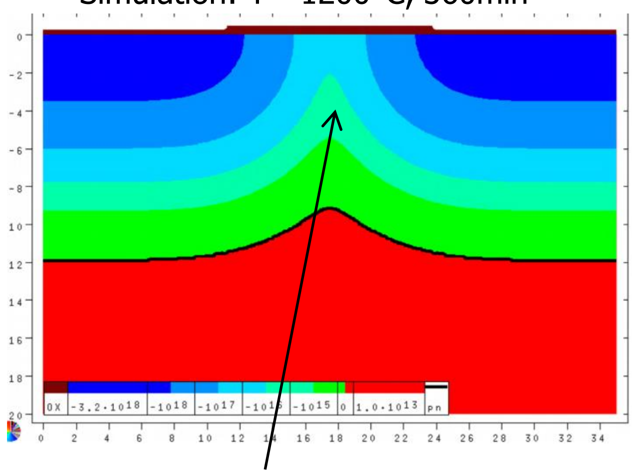
ICEMOS



Shinetsu

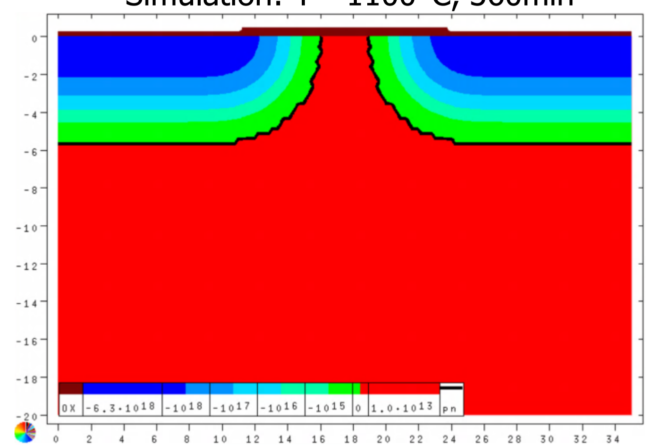


Simulation: T =1200°C, 360min



No n-doping, no space charge, no pot. barrier

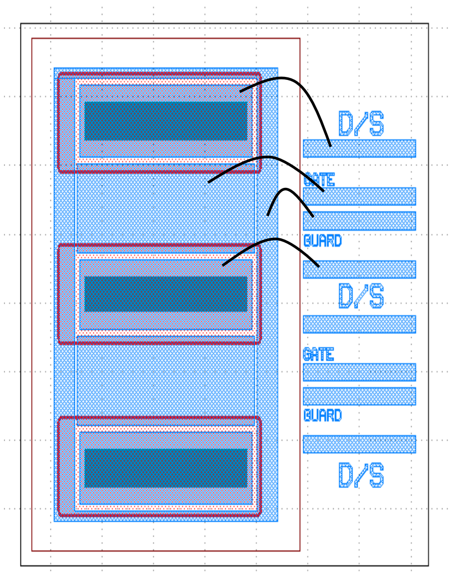
Simulation: T =1100°C, 360min

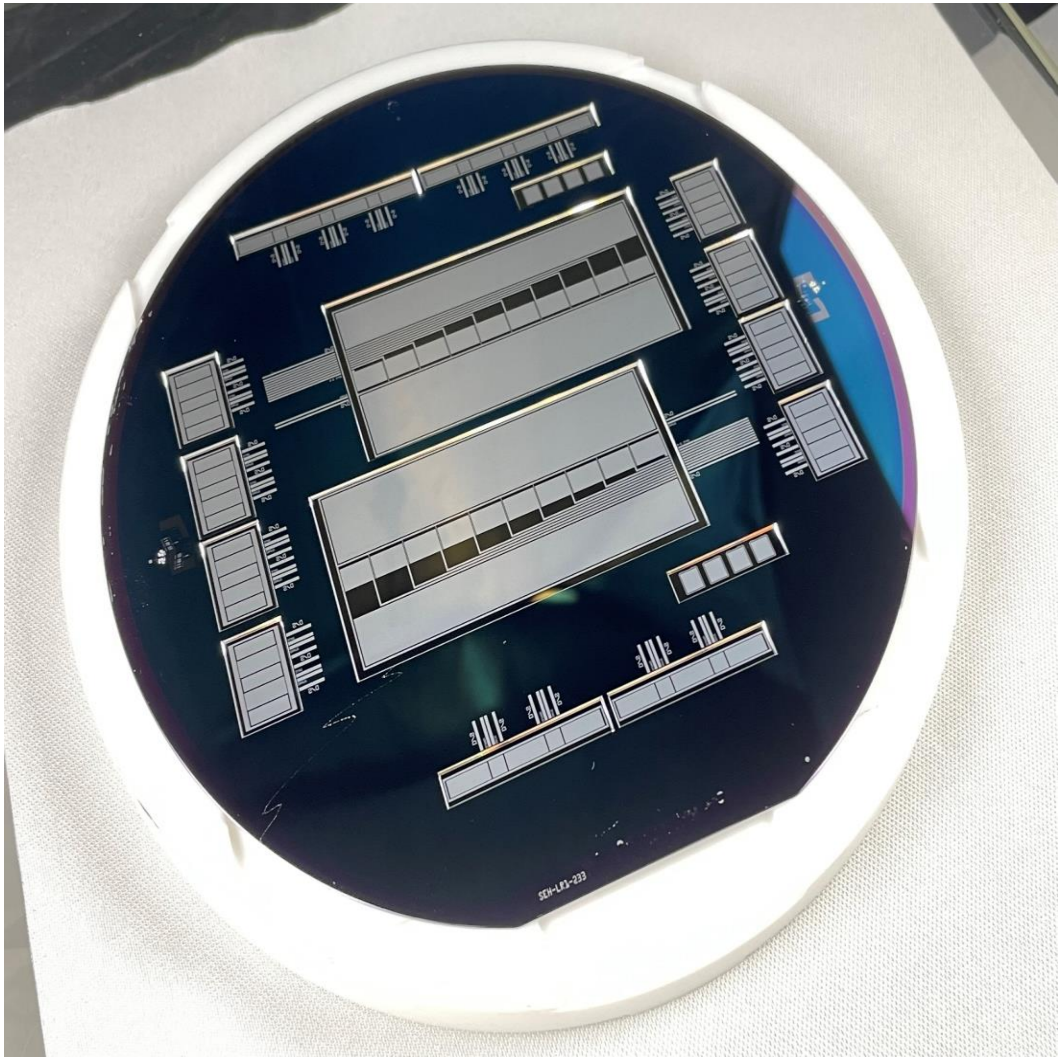


some n-doping, some charge, weak pot. barrier

The last Unknown Nox -> MOS Structures on BOX

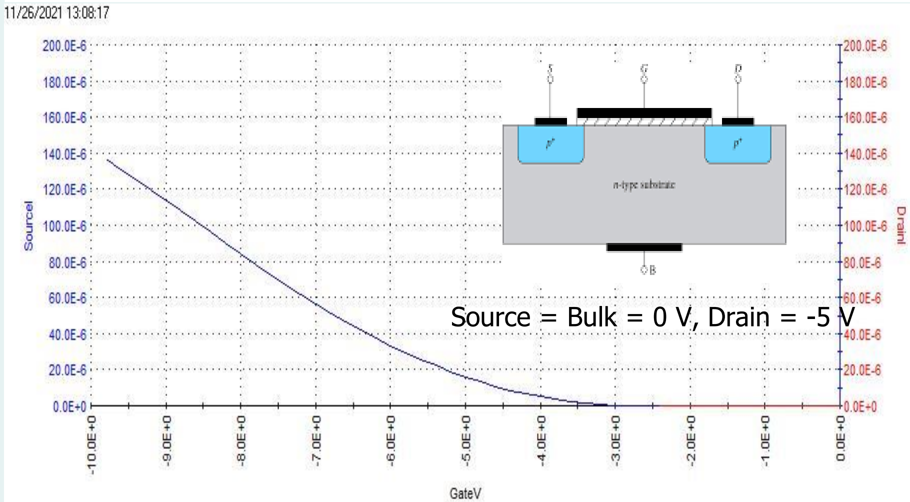
- ▷ 6 Wafers
  - ↳ 3 Icemos and 3 Shin-etsu bonded SOI
- ▷ Backside p+-implants as source and drain, BOX as gate isolator, Alu as gate → PMOS transistors
- ▷ MOS caps on BOX in addition



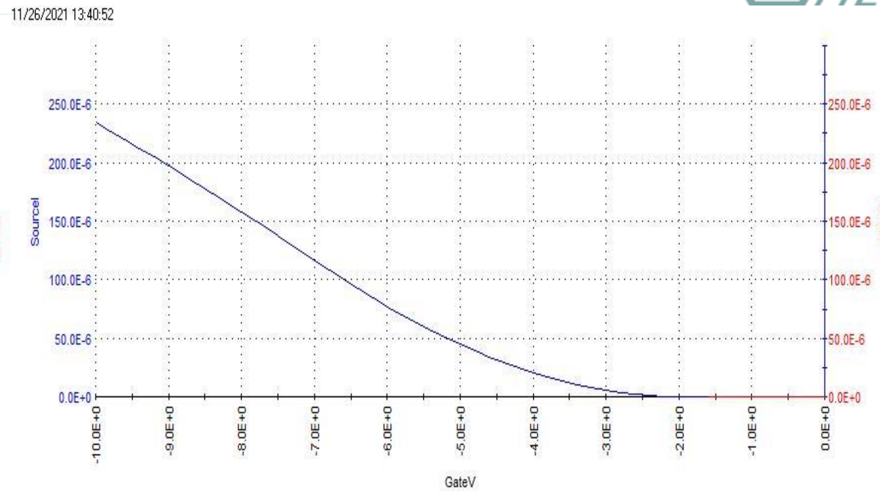


- ▷ Use a few chips for destructive SIMS implant profiling

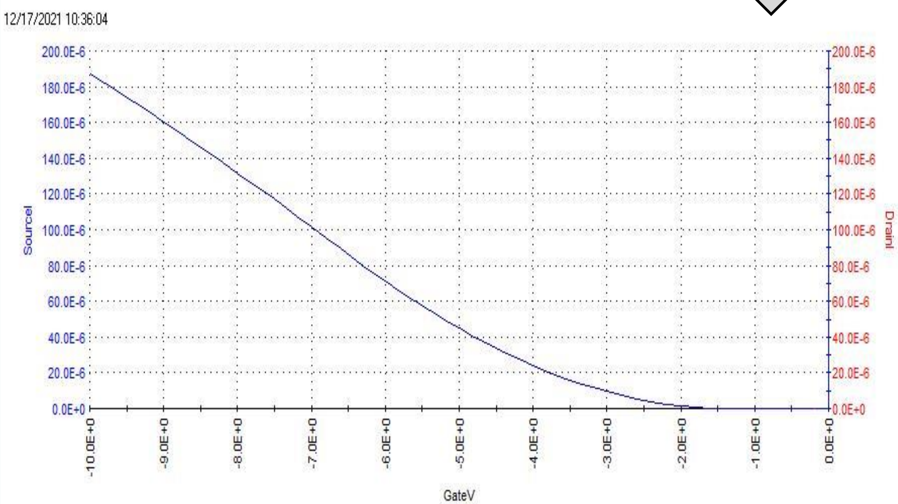
pMOS $I_{Drain}(V_{Gate})$: Before and after H2 anneal

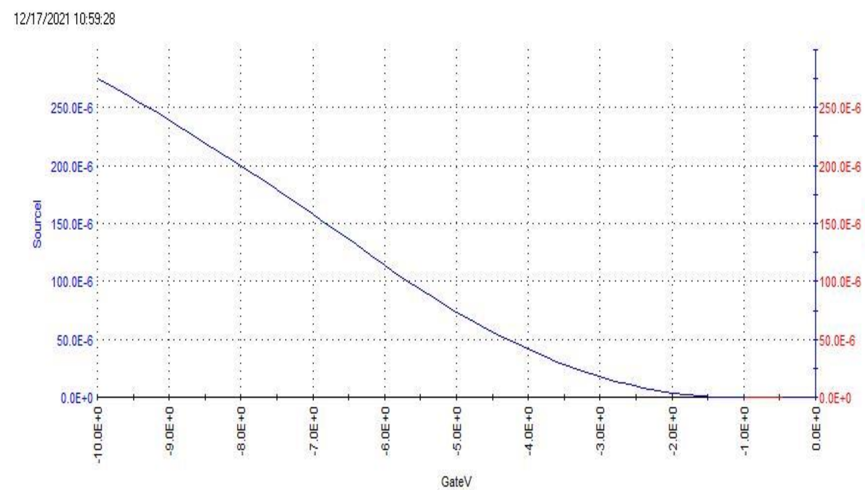


Source = Bulk = 0 V, Drain = -5 V



ICE 1h @ 400 degC in forming gas SHE





Summary

Reason for our HV current problems is understood

Underestimation of (lateral) diffusion due to very high temperature treatment at SOI suppliers

wrong backside doping profile measurement (SIMS)

Multi guard ring structure at BS to closely spaced -> shortage

It does not work at all (Icemos) - works badly (Shinetsu)

What are the plans for the MOS – structures on BOX? (Meeting)

Backup

Oxide charge densities

Not sure what is correct?

at break down position

Vhandle_wafer – Vif = 35V + 40V
= 75V

1V ≙ 0.5e11cm^{-2}

Qox = 3.75e12cm-2

at electron acc. layer

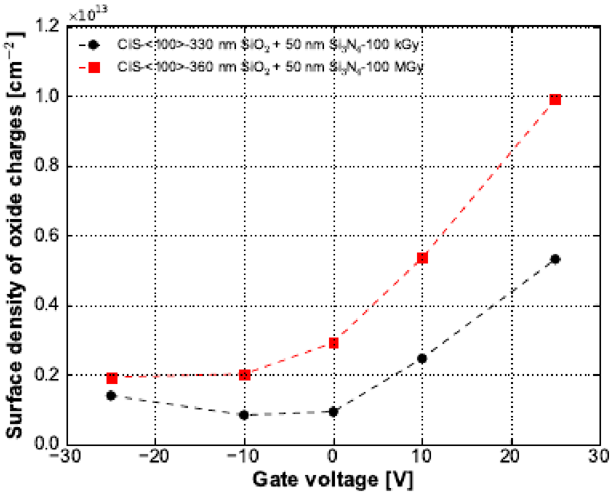
Vhandle_wafer – Vif = 35V + 22V
= 57V

1V ≙ 0.5e11cm^{-2}

Qox = 2.85e12cm-2

Oxide charge saturation density (X-ray radiation

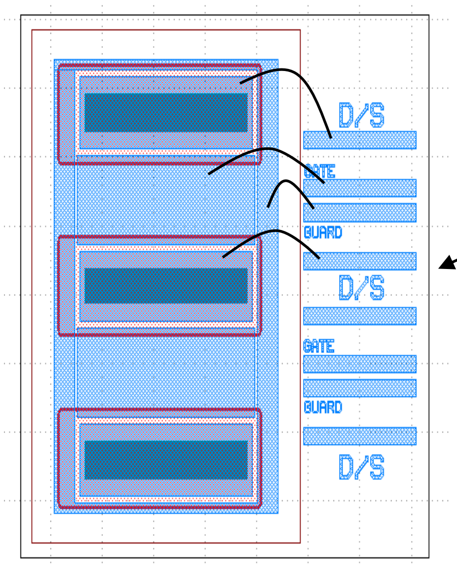
Moscatelli et al. (2016): 1.8e12cm-2
Zhang et al. (2011): 2.8e12

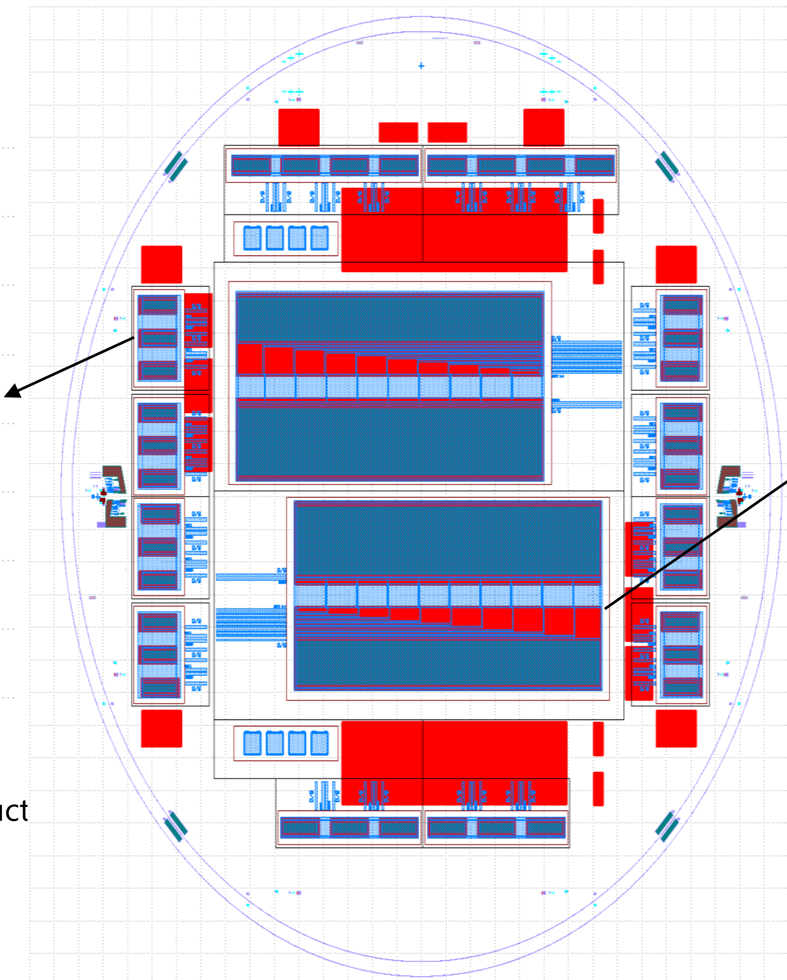


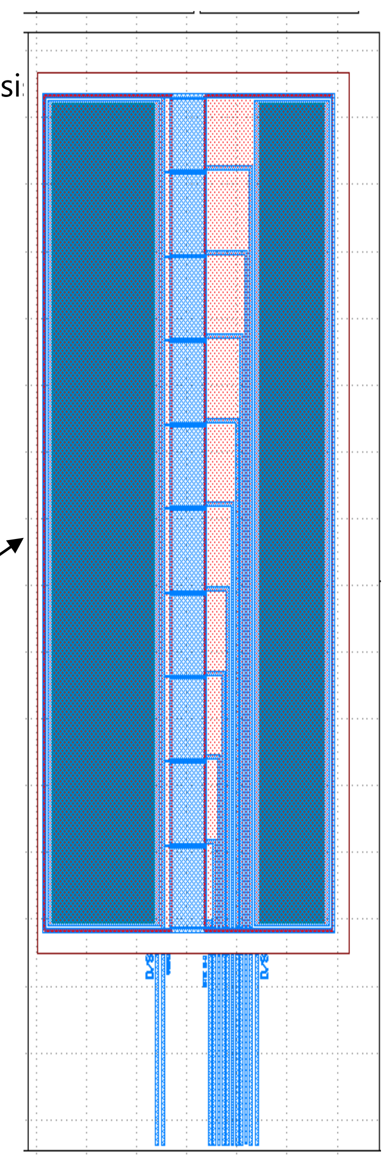
Highest values: Zhang et al. (2012):
but for 100MGy

MOS Structures on BOX

- 6 Wafers
  - 3 Icemos and 3 Shin-etsu bonded SOI
- Backside p+-implants as source and drain, BOX as gate isolator, Alu as gate → pMOS transi
- MOS caps on BOX in addition







- Use a few chips for destruct
  SIMS implant profiling