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SI LAB
Silizium Labor Bonn

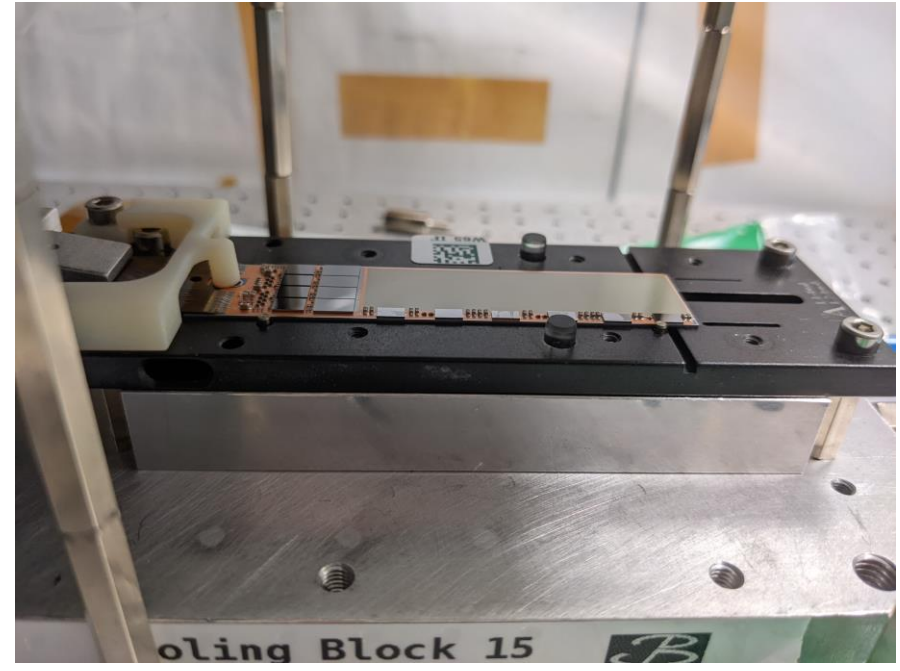
DCD gain, g_m and g_q measurement of PXD modules

24th International DEPFET workshop

Master Thesis by Larissa von Jasienicki
Talk by Munira Khan on behalf of the Bonn group

CALIBRATION OF PXD MODULES

- 12 module testing steps to check functionality and characterize modules
- Homogeneous efficient pixel response
  - Tuning of matrix biasing voltages
  - Tuning of DCD voltages and parameters
- All studies presented here are on fully optimized modules



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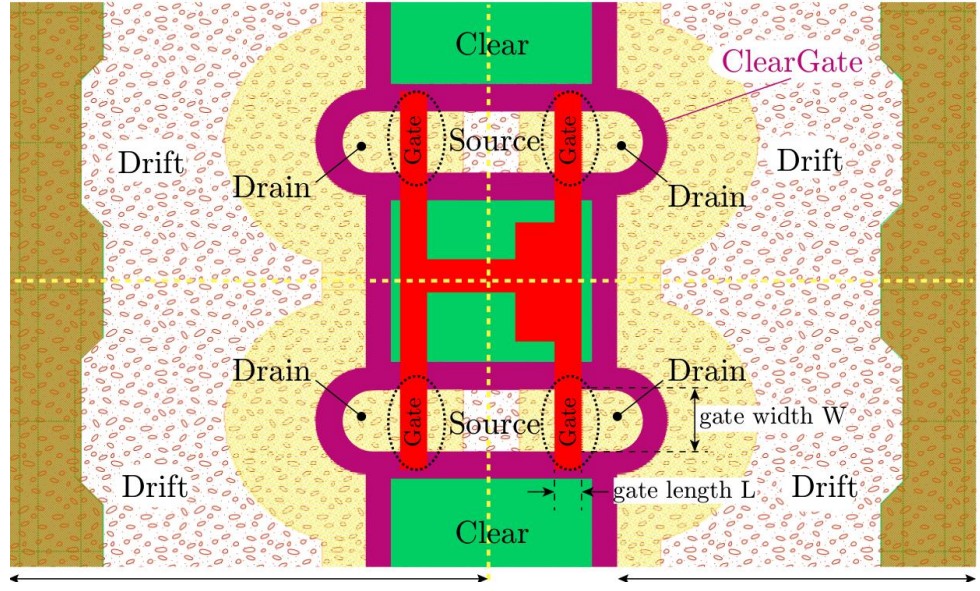
PXD Module Characterization

Biasing voltage studies

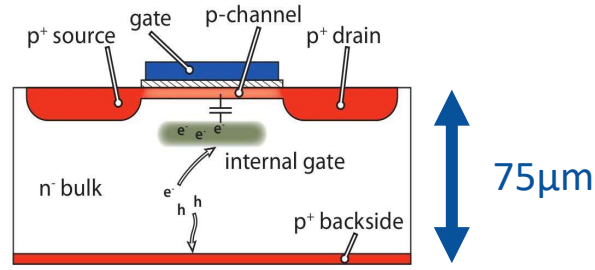
BIASING VOLTAGE STUDIES

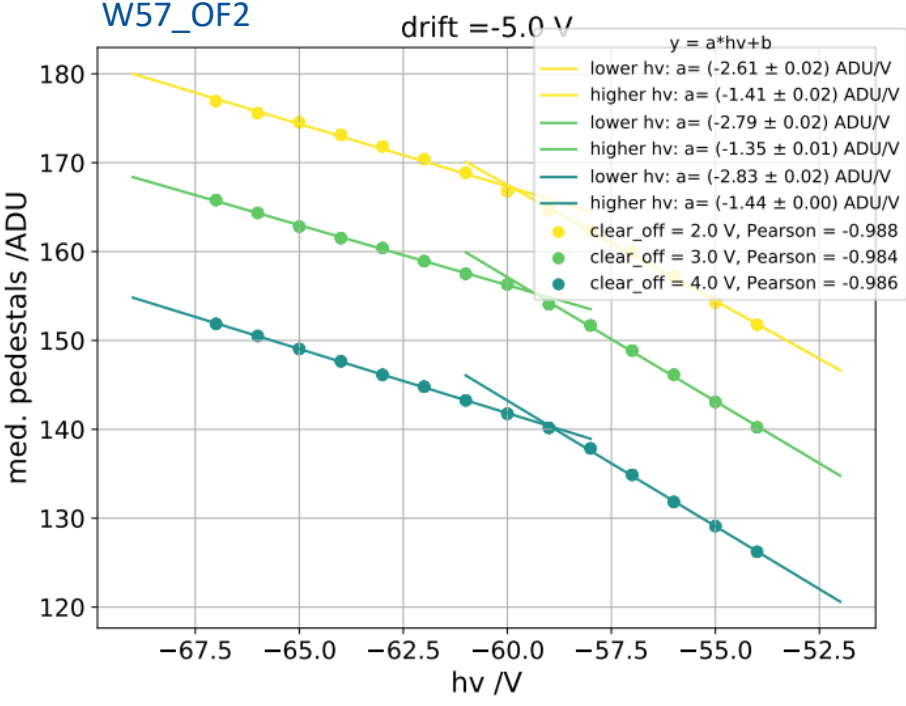
- Impact of different biasing voltages on pedestals
- Biasing voltages:
  1. hv: backside
  2. drift voltage: drift implants
  3. clear-off voltage: clear contact



Müller Felix (2017): Characterization and optimization of the prototype DEPFET modules for the Belle II Pixel Vertex Detector.

IMPACT OF HV

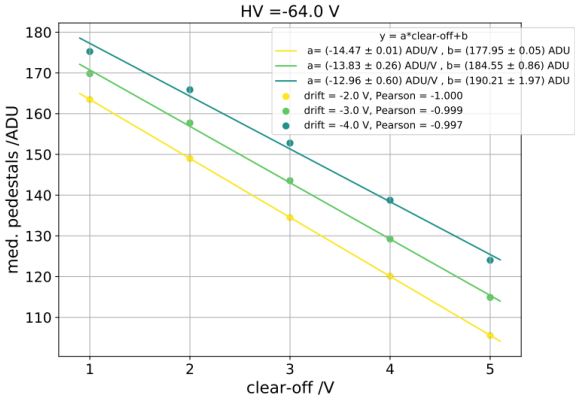




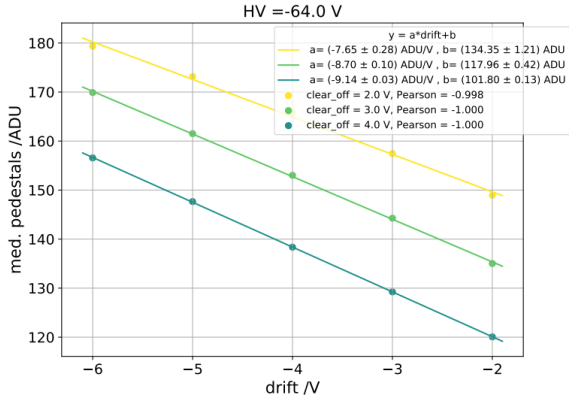
- hv influences pedestals!
  - Acts as remote gate (~75µm)
  - Coupling to FET
  - Change of potential influences drain current
- hv > -60V: not fully depleted

IMPACT BIASING VOLTAGES

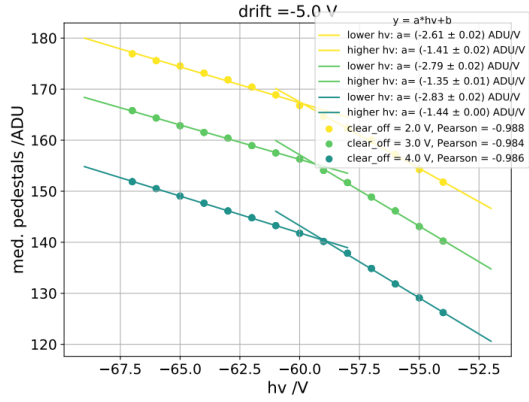
W57_OF2



-13.7 ADU/V

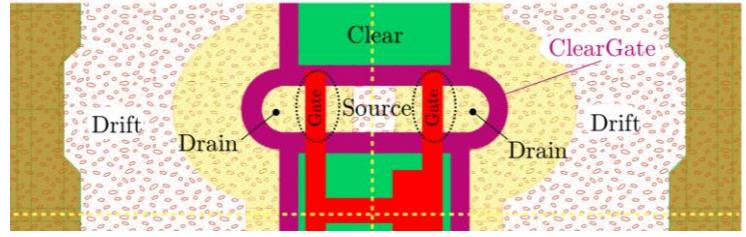


-8.5 ADU/V



-1.9 ADU/V

- Couplings to FET
- Clear-off voltage has highest impact on FET



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Tuning of DCD parameters
Measurements of g_m and g_q

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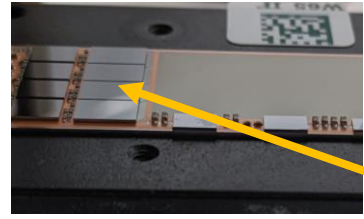
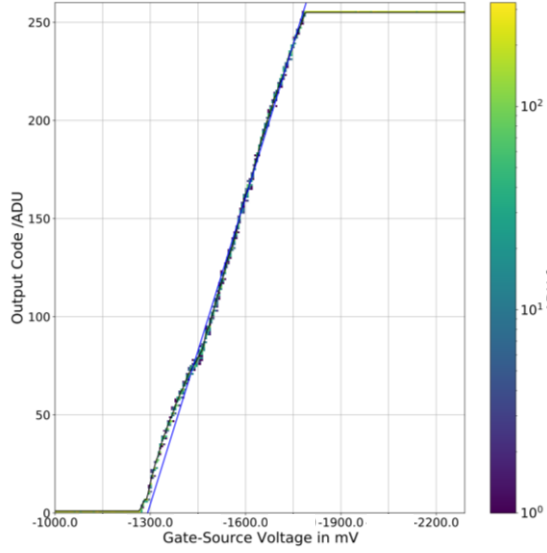
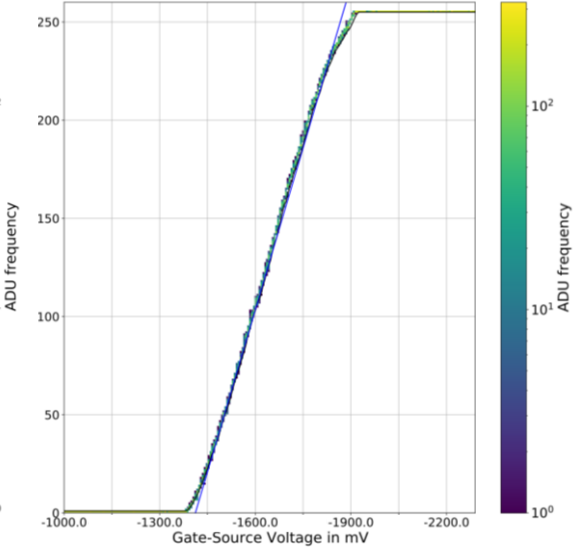
TUNING DCD PARAMETER



- 256 ADC (Analog to Digital Converter) channels per chip
- Optimize ADC response:
  - Tune voltages and settings
    - Whole dynamical range
    - No missing codes
    - As linear as possible
- No DCD gain in units of current



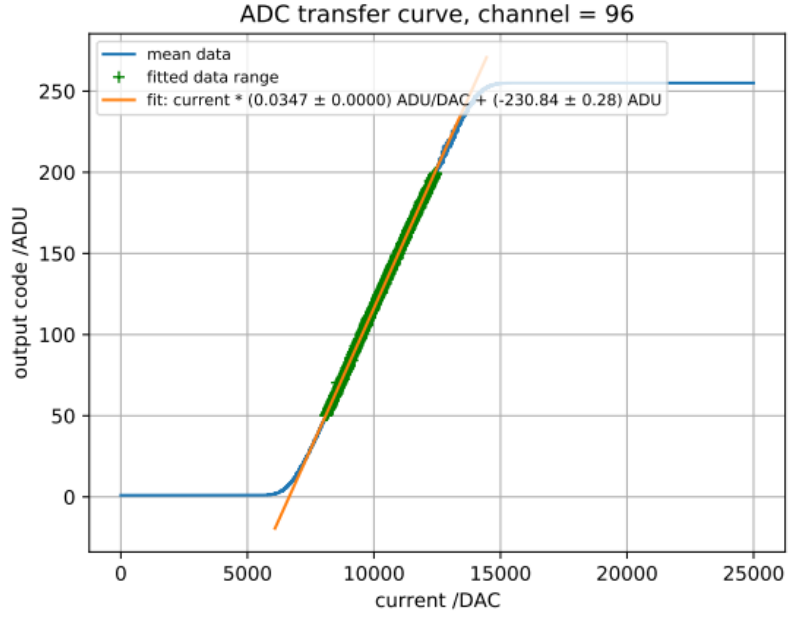
Bad setting



Good setting

DCD GAIN MEASUREMENT

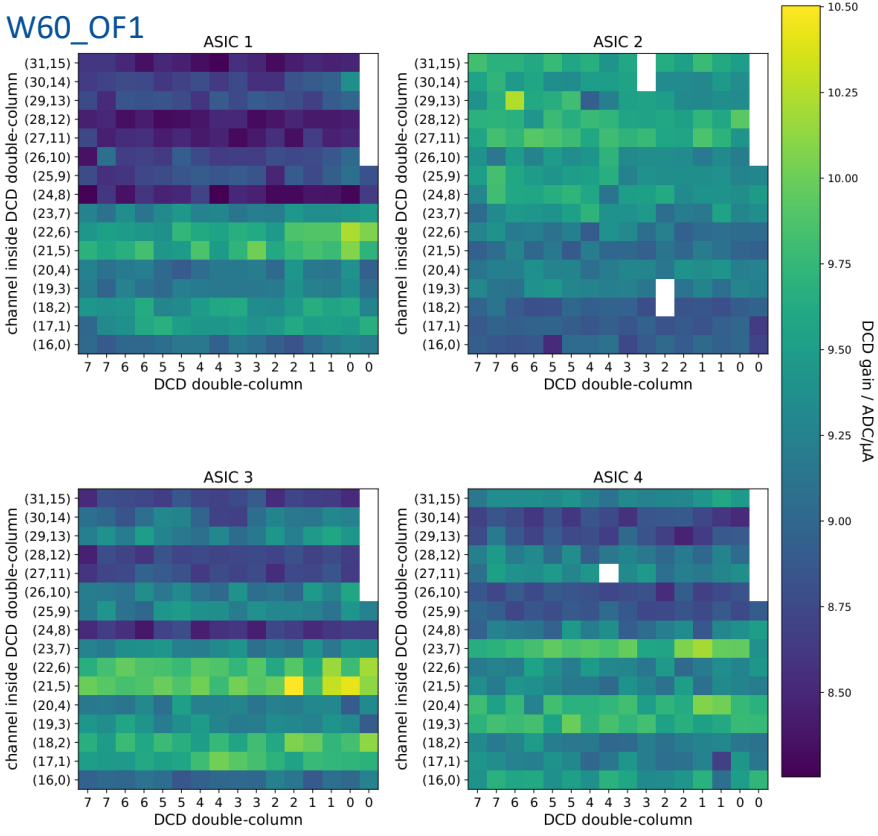
- Exact channel-by-channel calibration through injection of external current
- Necessary to evaluate DEPFET parameters, such as g_m and g_q



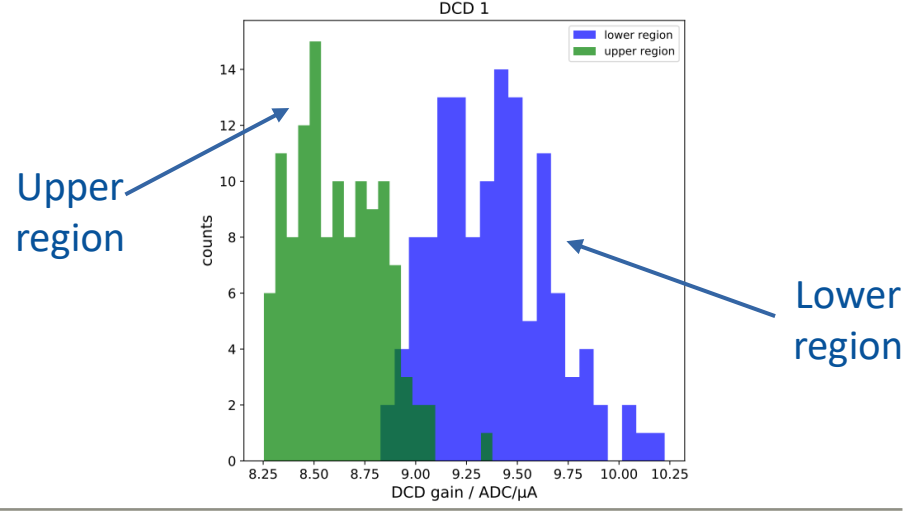
	W56_OF1	W56_OF1	W57_OB1	W57_OF2	W57_IB	W60_OF1
DCD gain ADU/µA	9.51	9.74	9.40	9.66	9.93	9.20

DCD GAIN PER CHANNEL

W60_OF1



- Deviations within upper and lower half DCD
  - Relative difference of around 6%
  - Internal voltage drop?



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CHARACTERIZATION ON PIXEL LEVEL

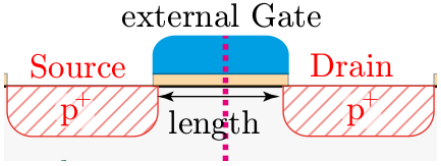
Fundamental DEPFET pixel properties:

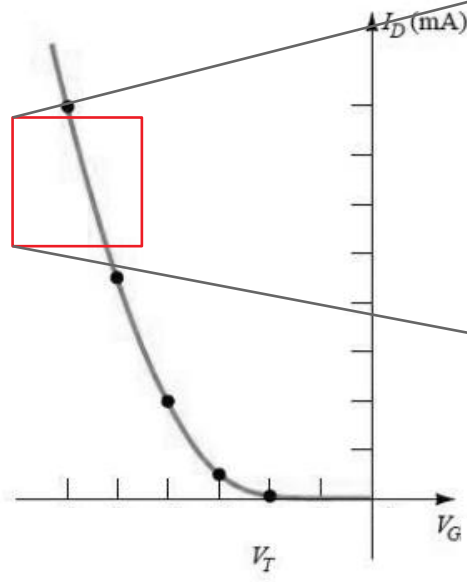
- **Transconductance g_m**: amplification of FET $g_m = \frac{\partial I_D}{\partial V_G}$
- **Charge amplification g_q**: amplification of pixel $g_q = \frac{\partial I_D}{\partial Q_{sig}}$
  - Rough expectation: $g_q \approx 400 - 600\, pA/e^-$

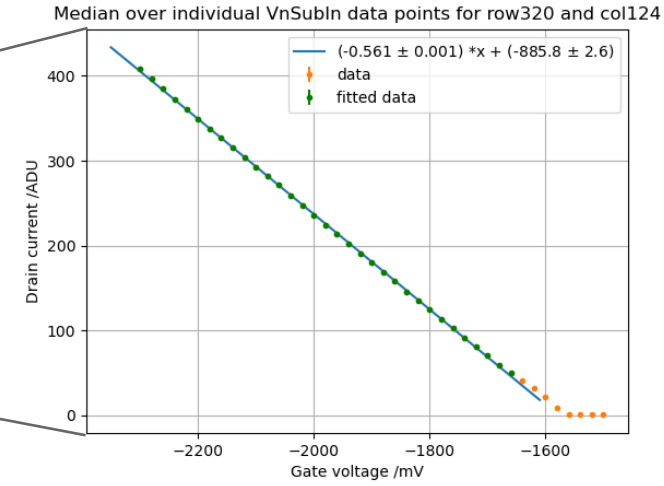
→ Investigation on pixel level

TRANSCONDUCTANCE G_M

W60_OF1







$$g_m = \frac{\partial I_D}{\partial V_G}$$

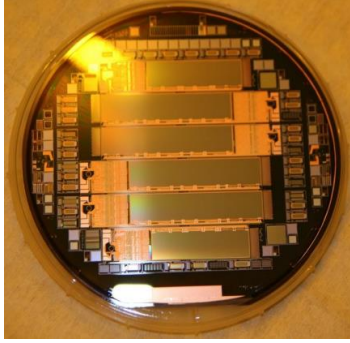
I_D: measured current

V_G: gate voltage

$$g_m = \frac{slope}{A_{DCD}} = -62.9\,\frac{\mu A}{V}$$

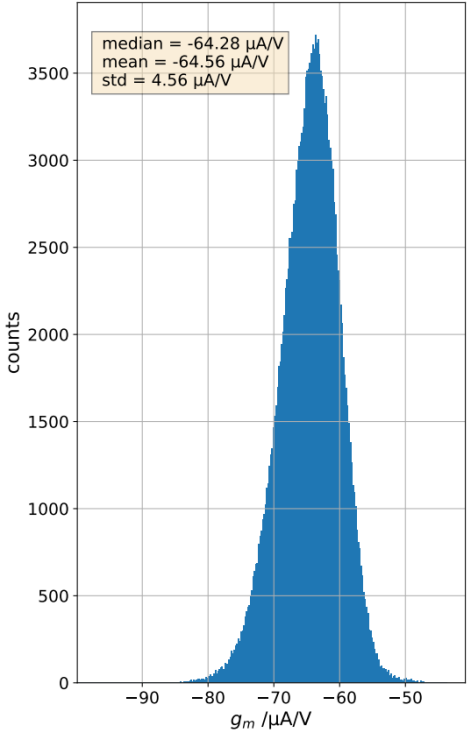
A_{DCD}: DCD Gain

RESULTS OF G_M MEASUREMENT



Ladislav Andricek, MPG Halbleiterlabor

W60_OF1



Wafer number

Location in detector

	W56_OB1	W56_OF1	W57_OB1	W57_OF2	W57_IB	W60_OF1	W67_IB
g_m / $\frac{\mu A}{V}$	-72.8	-73.4	-61.7	-65.9	-65.6	-64.3	-46.0

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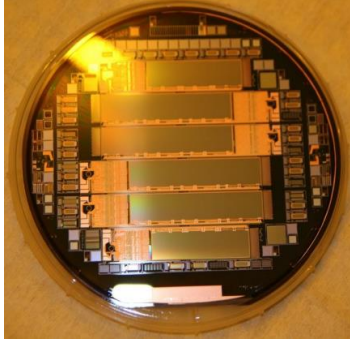
RESULTS OF G_M MEASUREMENT



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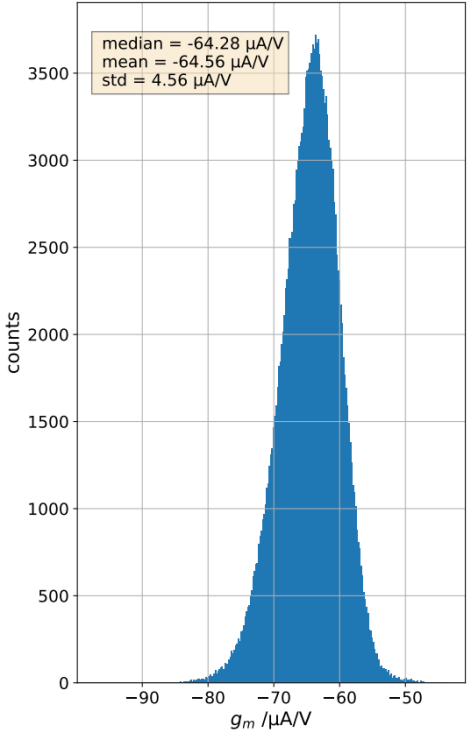
W60_OF1

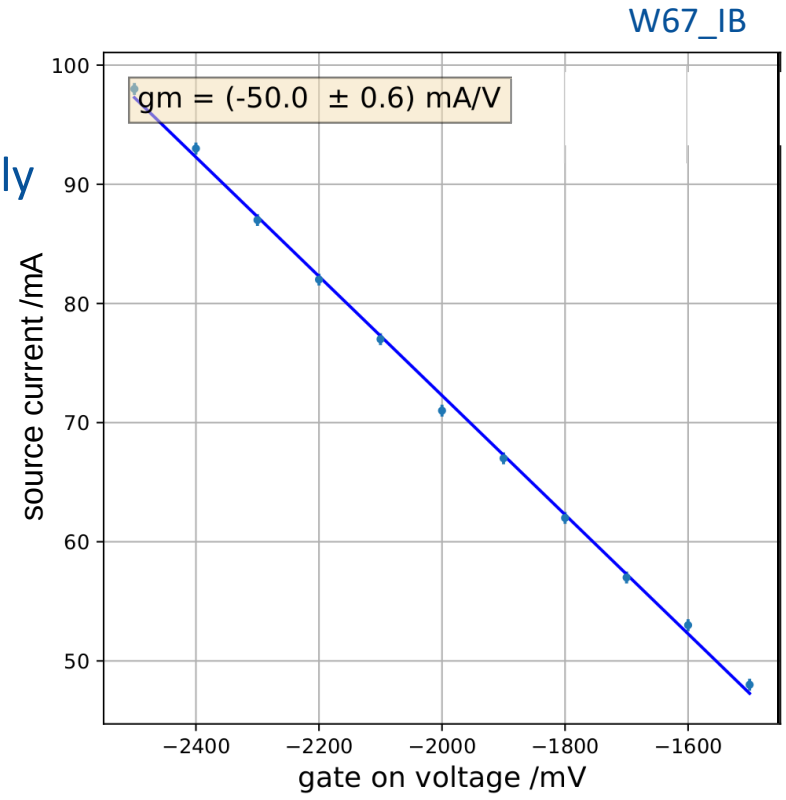


	W56_OB1	W56_OF1	W57_OB1	W57_OF2	W57_IB	W60_OF1	W67_IB
g_m / $\frac{\mu A}{V}$	-72.8	-73.4	-61.7	-65.9	-65.6	-64.3	-46.0

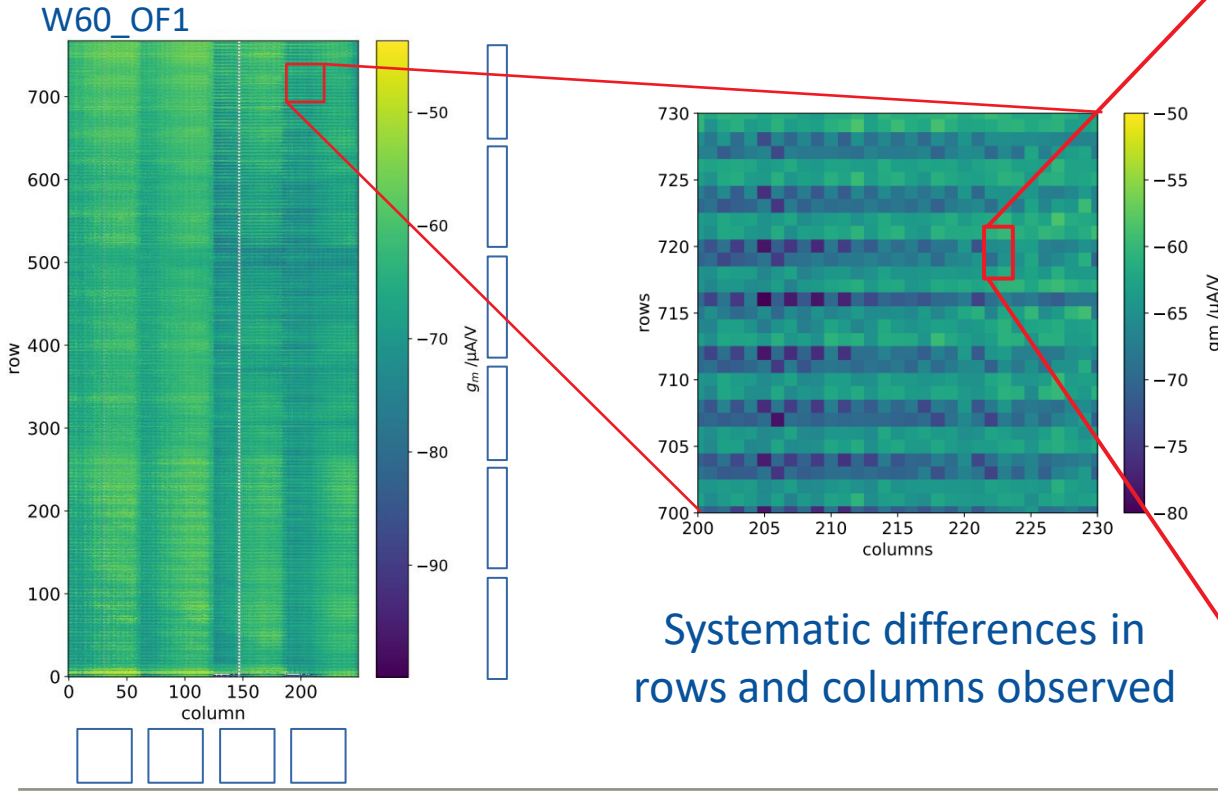
→ Dependence between wafer and mean g_m observed

CROSS-CHECK FOR G_M MEASUREMENT

- Read drain current directly from power supply
- g_m measured over all drain lines (not per pixel!)
- Previous method: $-46.45\,\frac{\mu A}{V}$ with std. of $6.6\,\frac{\mu A}{V}$ over all pixels
- Cross-check value: $(-50.0 \pm 0.6)\,\frac{\mu A}{V}$



G_M PIXEL STRUCTURES

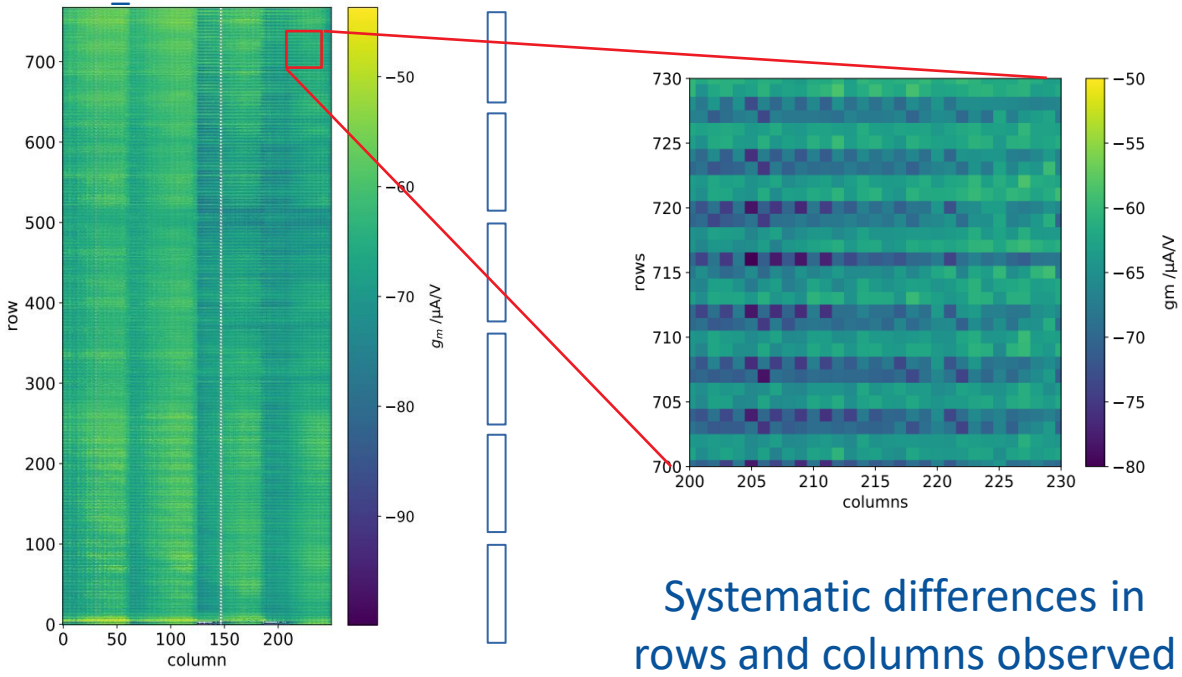


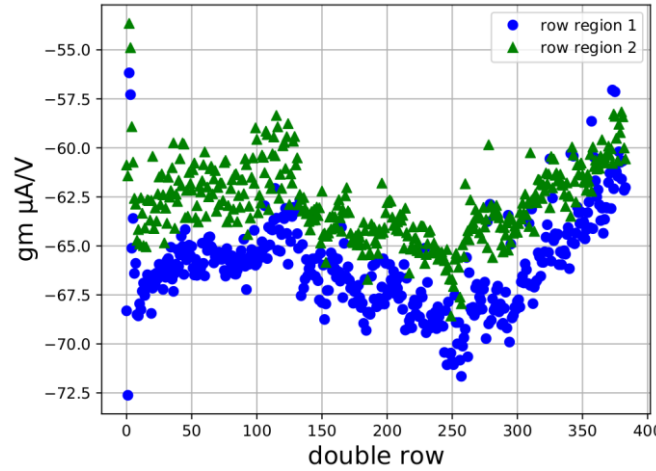
Systematic differences in rows and columns observed

Felix Müller (2017): Characterization and optimization of the prototype DEPFET modules for the Belle II Pixel Vertex Detector

PROJECTION TRANSCONDUCTANCE G_M: ROWS

W60_OF1

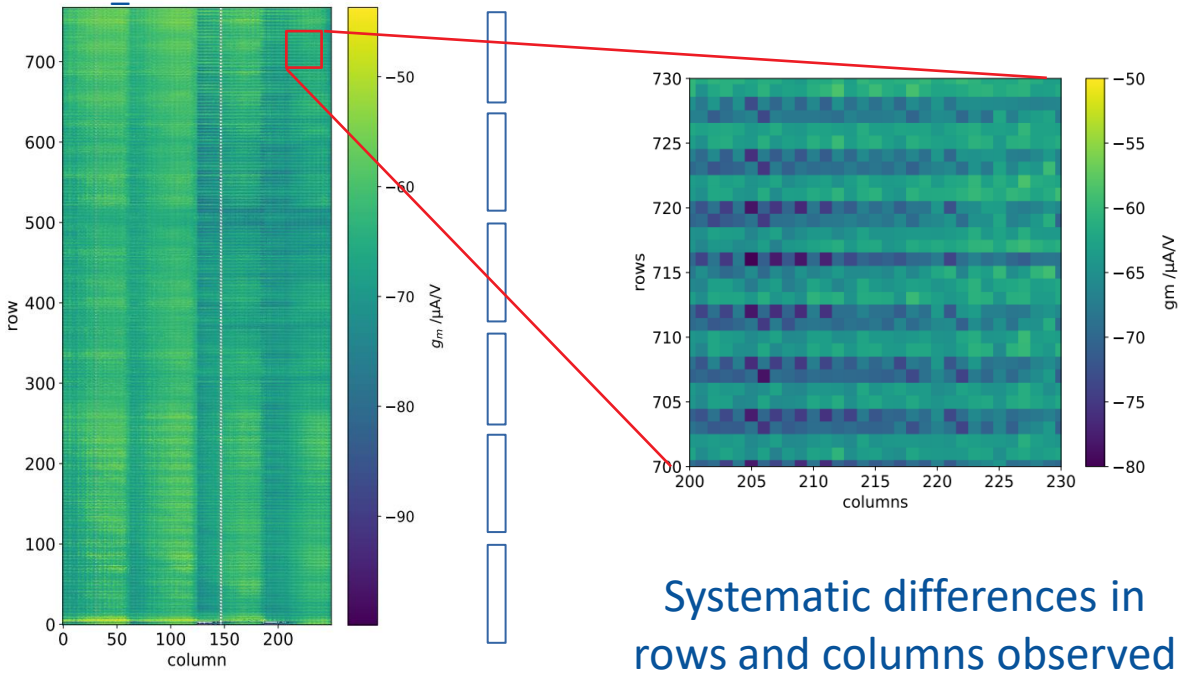


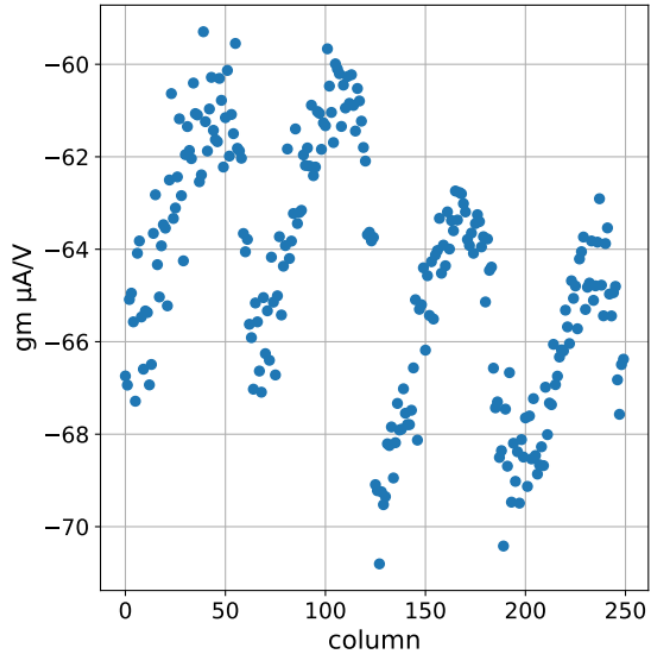


Systematic differences in rows and columns observed

PROJECTION TRANSCONDUCTANCE G_M: COLUMNS

W60_OF1





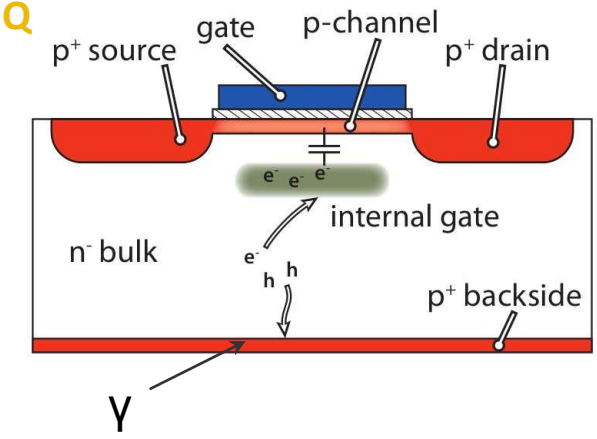
Systematic differences in rows and columns observed

CHARGE AMPLIFICATION G_Q

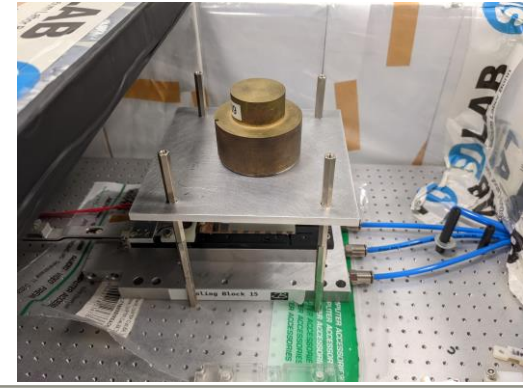
$$g_q = \frac{\partial I_D}{\partial Q_{sig}}$$

I_D: measured current

Q_{sig}: signal charge



- Signal generated with radioactive ^{109}Cd photon source (1850 MBq)
- 6300 electron-hole pairs in silicon



SINGLE PHOTON SPECTRUM

$$g_q = \frac{\mu}{A_{DCD}} \Big/ \frac{E_{K_\alpha}}{E_{eh}} = 743.8\,pA/e^-$$

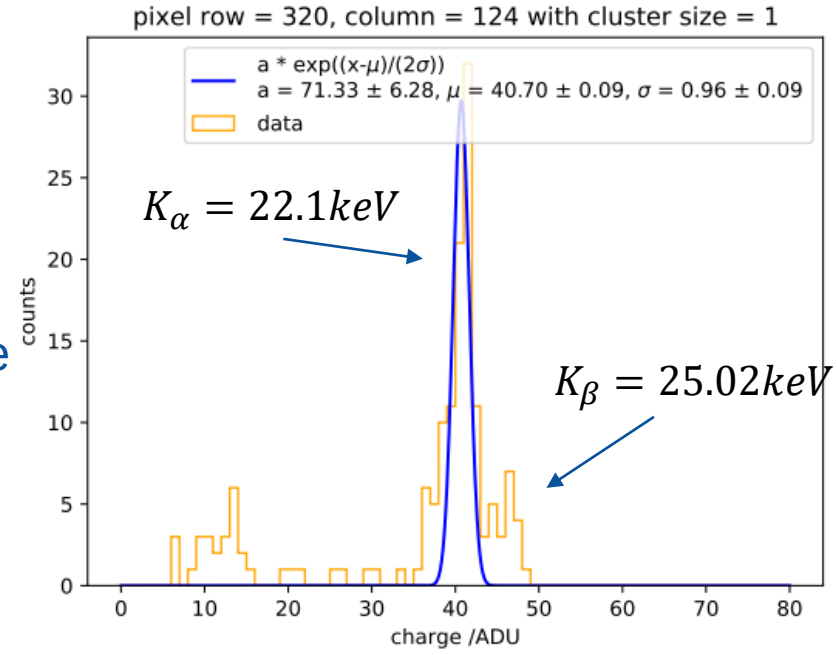
$E_{eh} = 3.65\,eV/e^-$ average energy to create electron-hole pair

E_{K_α}: energy ^{109}Cd K_α

μ: measured K_α peak

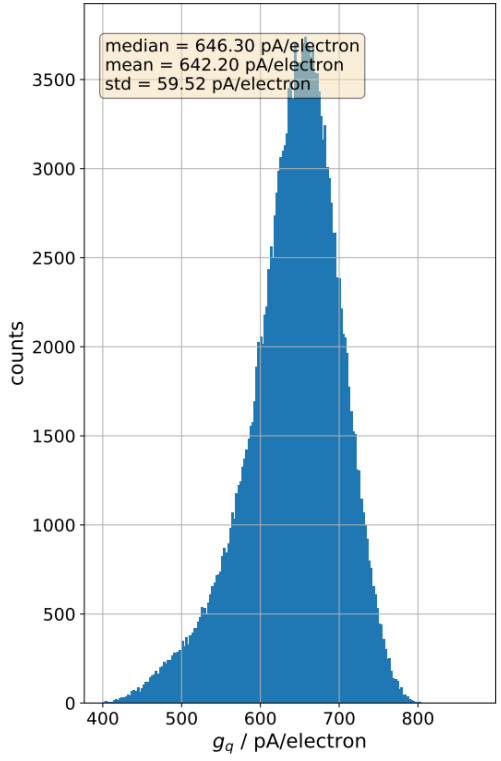
A_{DCD}: DCD Gain

W60_OF1



RESULTS OF G_Q MEASUREMENT

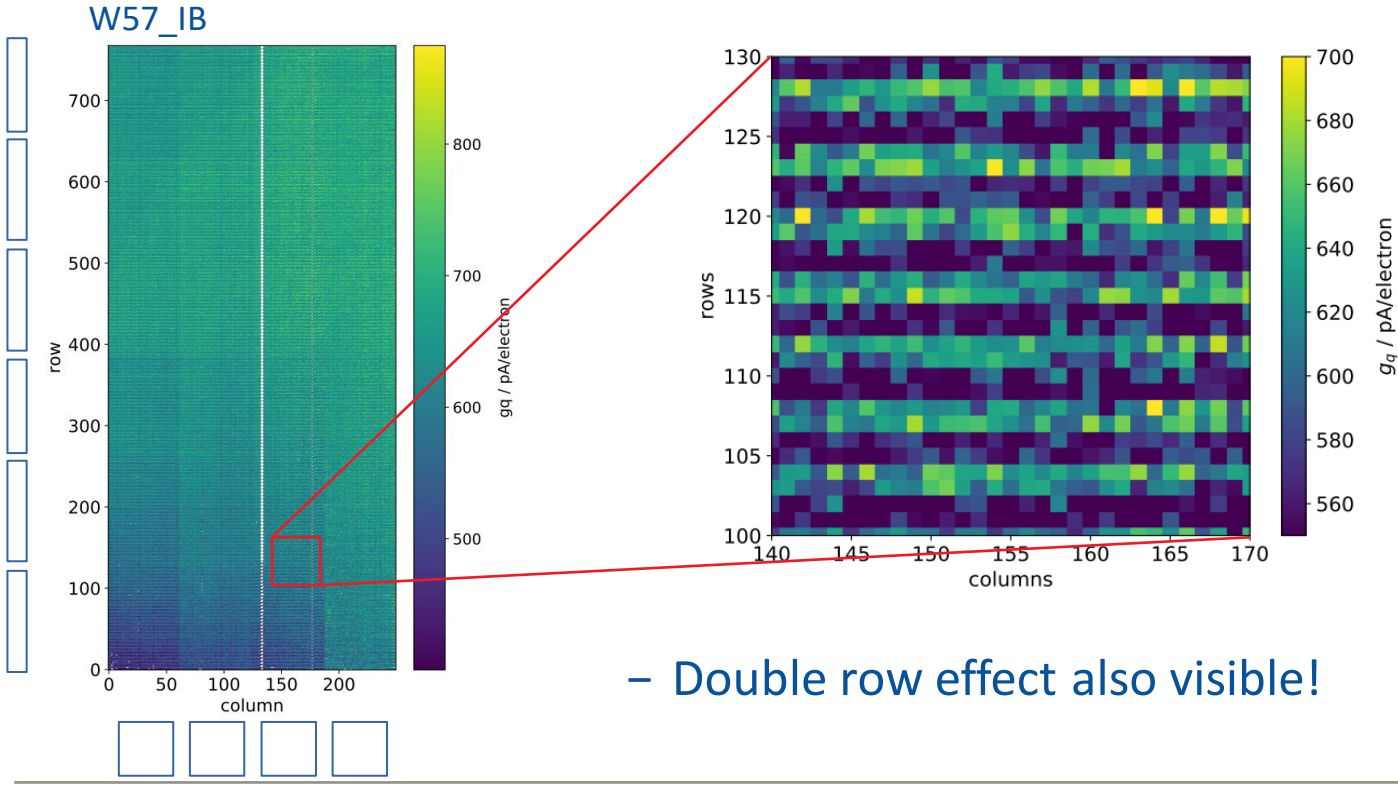
W57_IB



	W60_OF1	W57_IB	W67_IB
$g_q/pA/e^-$	743.91	648.55	517.40

- Assumed: $g_q \approx 400 - 600\,pA/e^-$
- All measured with gate-on = 2.1V
- Different source current

G_Q PIXEL STRUCTURES



– Double row effect also visible!

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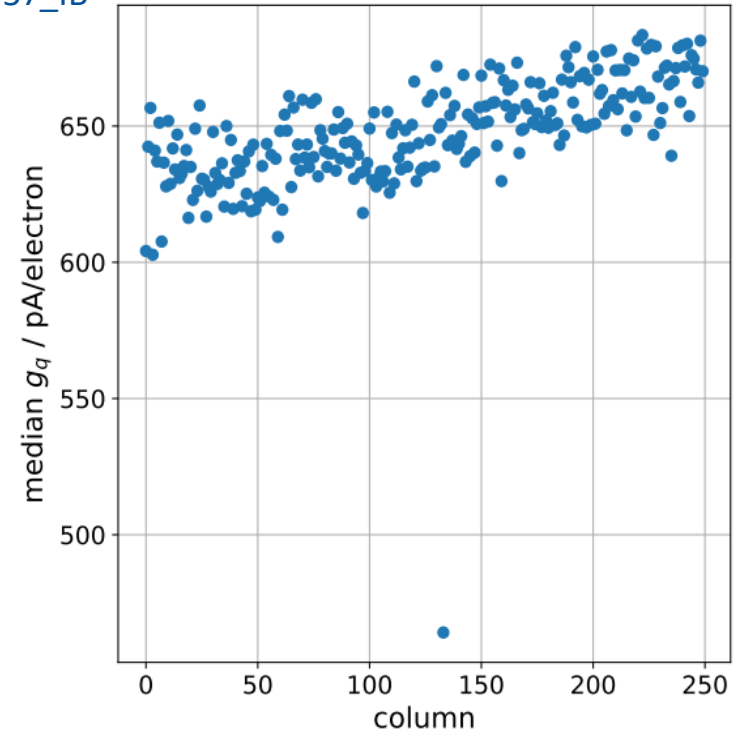
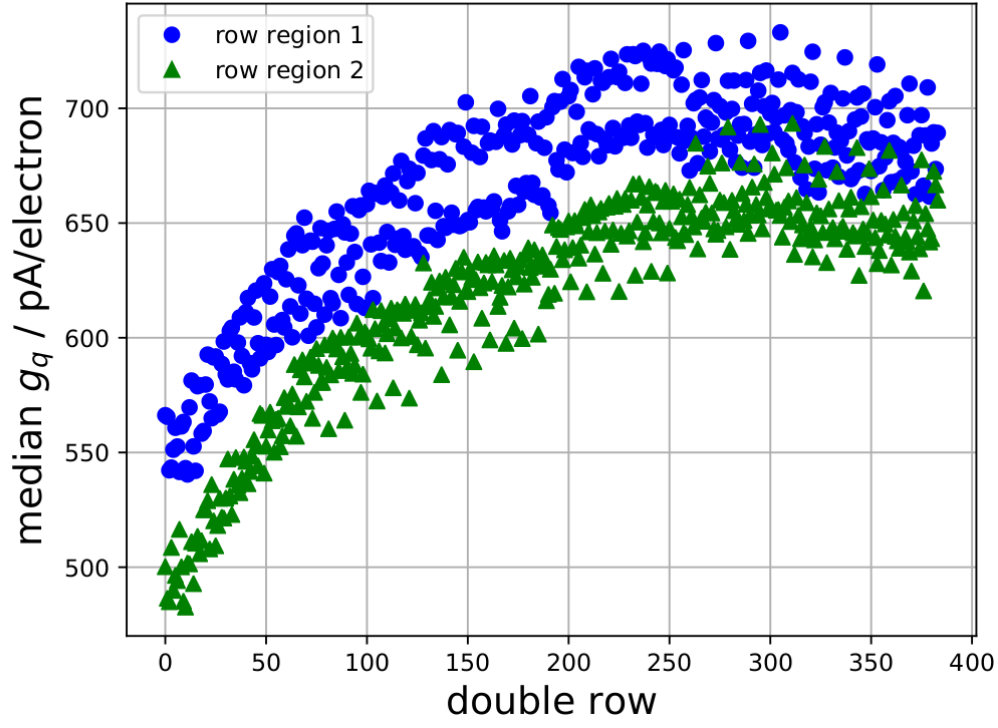
PROJECTION OF CHARGE AMPLIFICATION G_Q

W57_IB





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CONCLUSION

- Biasing Voltage Studies
  - Potential couplings between Implants and FET
- Detailed channel by channel /pixel by pixel characterization
  - Deviations between modules
    → More statistics needed for g_q! Observed wafer dependent variations in g_m
  - Recurring pattern inside sensitive area → Several patterns under investigation
- Outlook: Different structures when irradiating modules?

→ All plots for all tested modules can be found in Larissa's thesis


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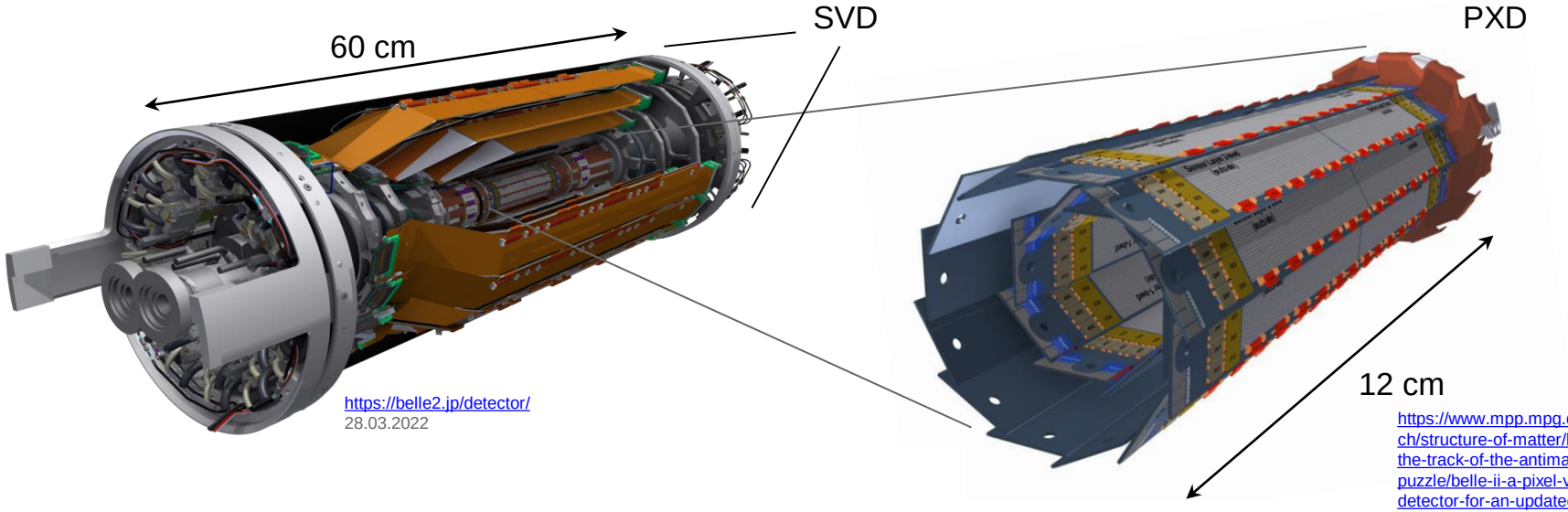
VERTEX DETECTOR



https://belle2.jp/detector/
28.03.2022

https://www.mpp.mpg.de/en/research/structure-of-matter/belle-ii-on-the-track-of-the-antimatter-puzzle/belle-ii-a-pixel-vertex-detector-for-an-updated-accelerator 28.03.2022

- 4 layers of double sided silicon strips (SVD)
  - R = 3.9 cm, 8.0 cm, 10.4 cm, 13.5 cm
  - Area ~ 1 m^2
- 2 layers DEPFET pixel detector (PXD)
  - R = 1.4 cm, 2.2 cm
  - Area ~ 0.03 m^2

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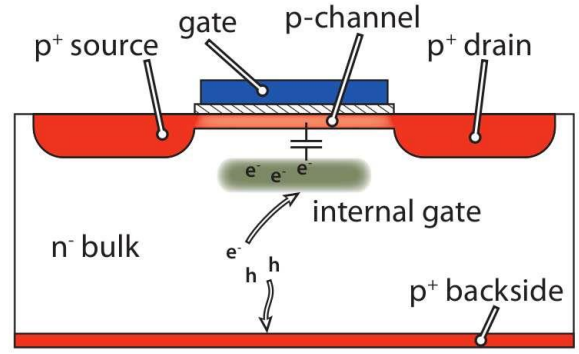
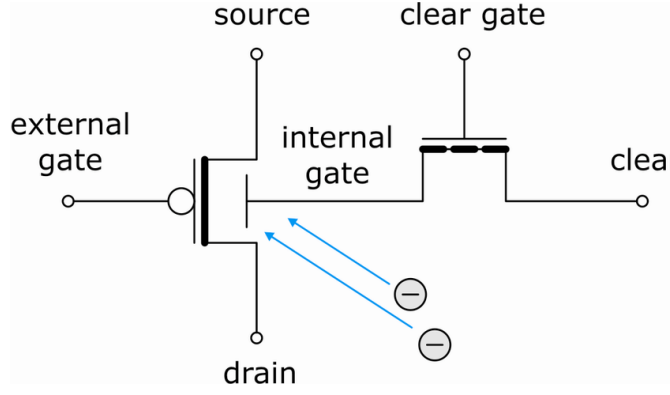
THE DEPFET PIXEL

- Field Effect Transistor (FET): source, gate, drain
- Depleted silicon bulk
- Fast charge collection in internal gate (~ns)
  - Modulates drain current I_D
- Additional FET for clear mechanism
  - Internal gate cleared periodically
  - Clear-on voltage applied at clear contact
- Pedestals: drain current without charge inside internal gate

$$I_{sig} = I_D - I_{ped}$$





https://indico.belle2.org/event/2751/contributions/13095/attachments/7153/11097/2020_09_14_belle2_germany_pxd6.pdf

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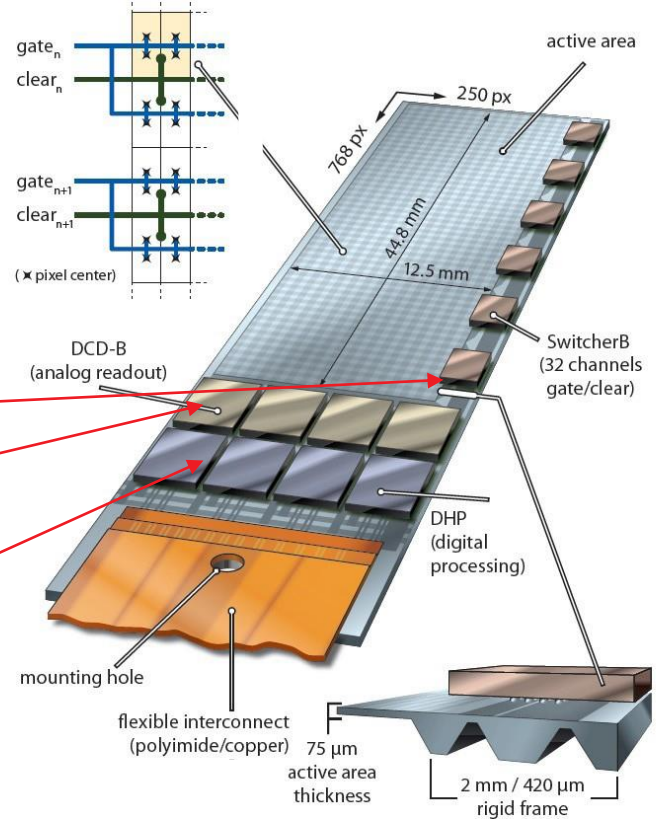
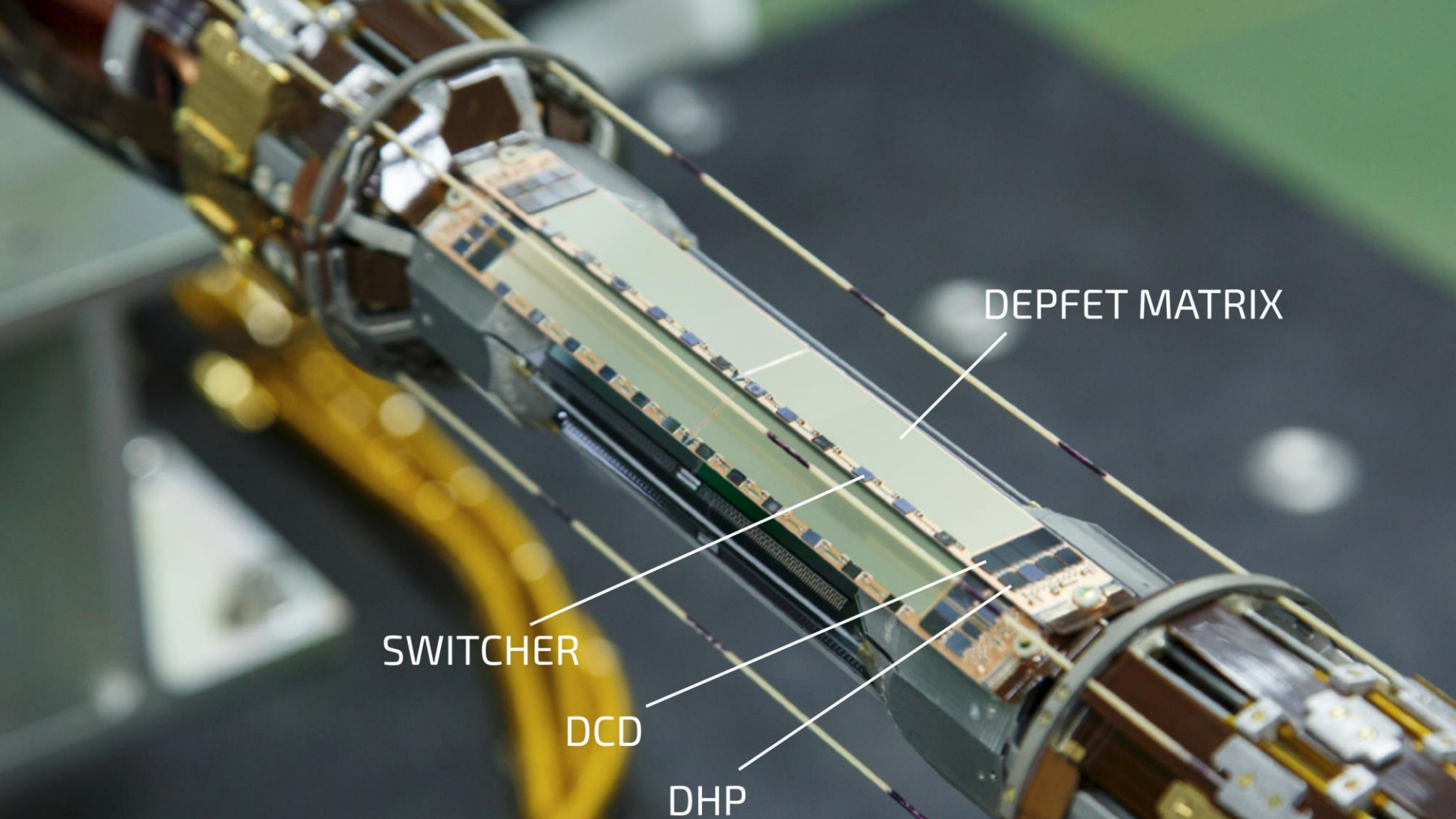
THE PXD MODULE

- Thickness of active area: 75 µm
- Rolling shutter readout: row wise
  - Drain current read with ~20 µs integration time
  - Controlled by gate and clear voltage
- **Switcher**:
  - Control gate and clear lines
- **Drain Current Digitizer (DCD)**:
  - 256 Analog to Digital Converters (ADCs)
  - Digitizes drain current
- **Data Handling Processor (DHP)**:
  - Processes data further




DEPFET MATRIX
SWITCHER
DCD
DHP

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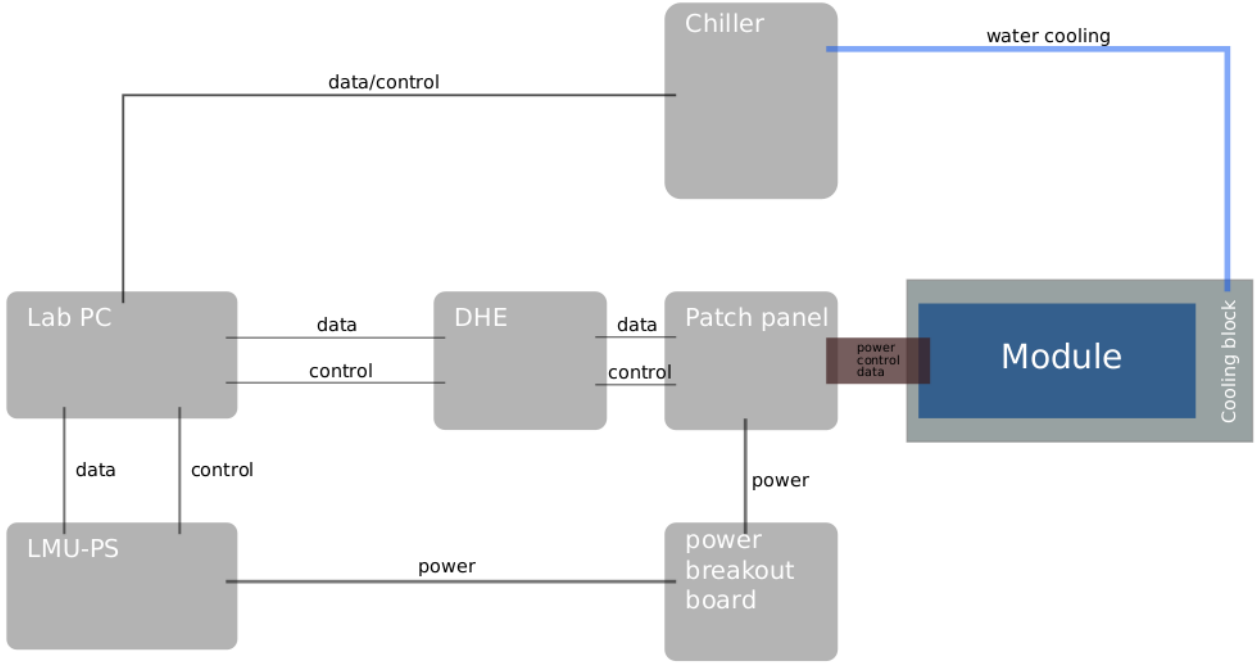
MODULE TESTING SETUP



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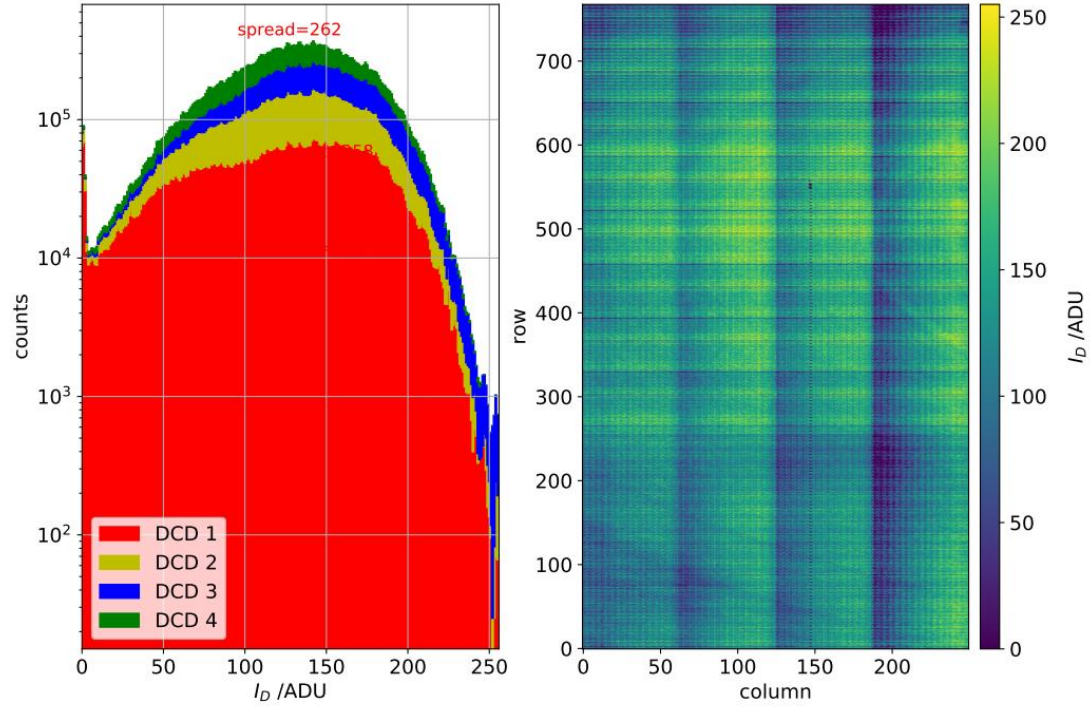
PEDESTALS

- Spread due to:
  - Process variations
  - DCD gain influence
  - g_m and threshold
- Pedestals need to be uploaded frequently:
  - Temperature
  - Radiation



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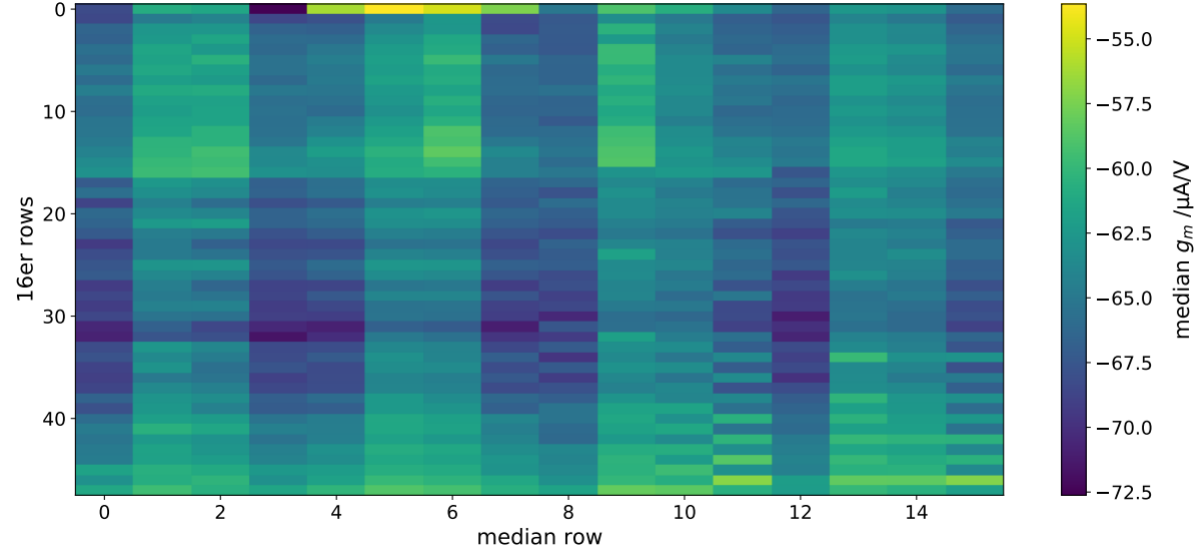
16ER ROW PATTERN

- Differences in pattern for larger/smaller pixel
  - Production of implants
  - Lithography masks overlapping



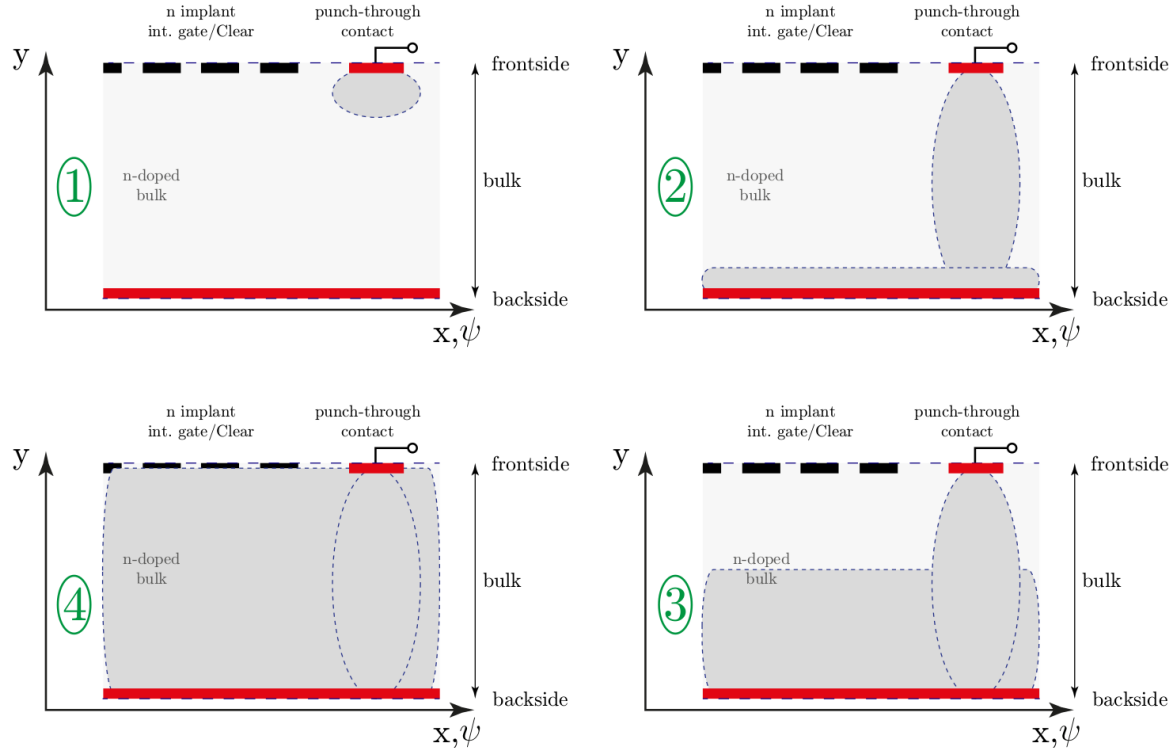
DEPLETION DEPFET PIXEL

1) high voltage (hv) applied to punch-through contact

2) hv ~ -35 V depletion zone spreads to the backside

3) Bulk starts to get depleted

4) Bulk fully depleted

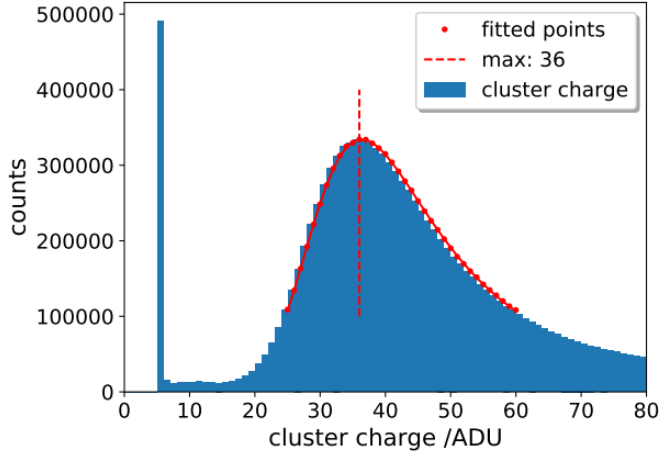


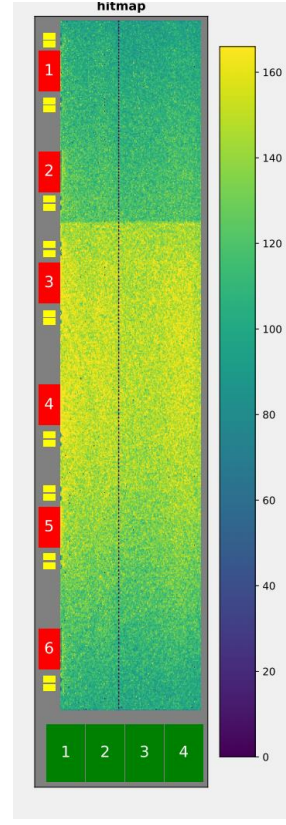
Müller Felix (2017): Characterization and optimization of the prototype DEPFET modules for the Belle II Pixel Vertex Detector.

MATRIX BIASING

^{90}Sr (33MBq)

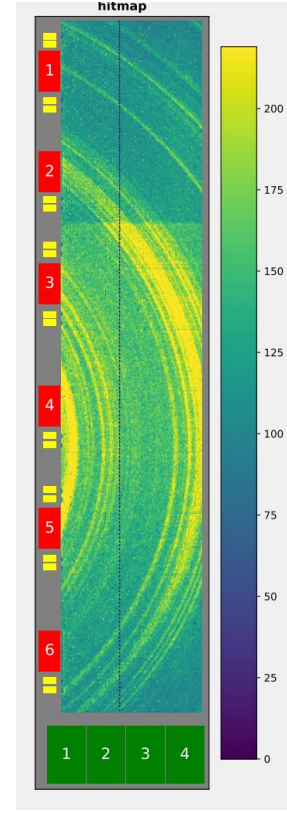
- Optimal bulk depletion
  - Homogeneous pixel response
  - Highest charge collection efficiency





hv: - 51V
drift: - 5V
clear: 3V

good setting



bad setting

hv: - 46V
drift: - 5V
clear: 3V