CHARACTERIZATION PLOTS W59_OB2

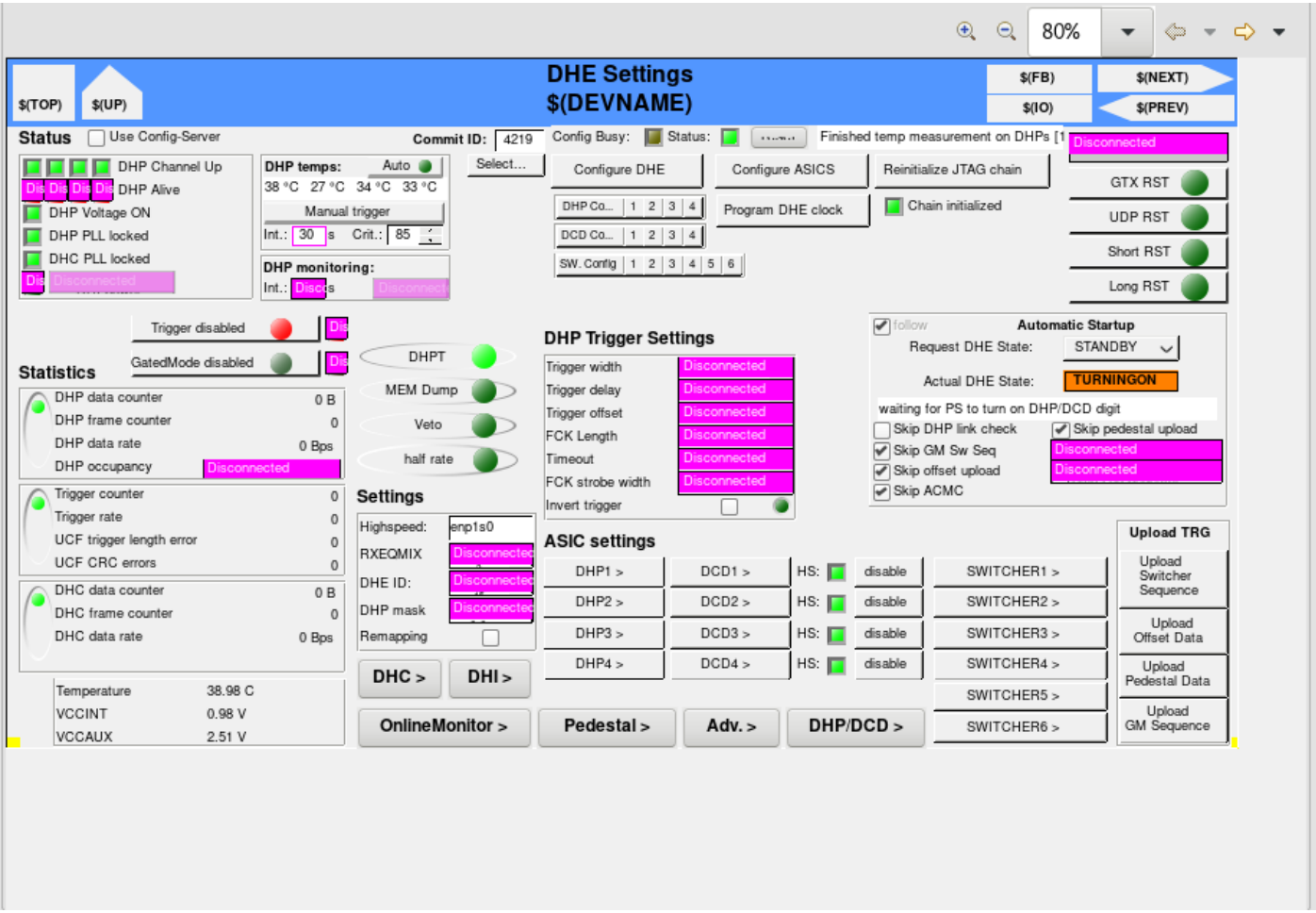
Botho

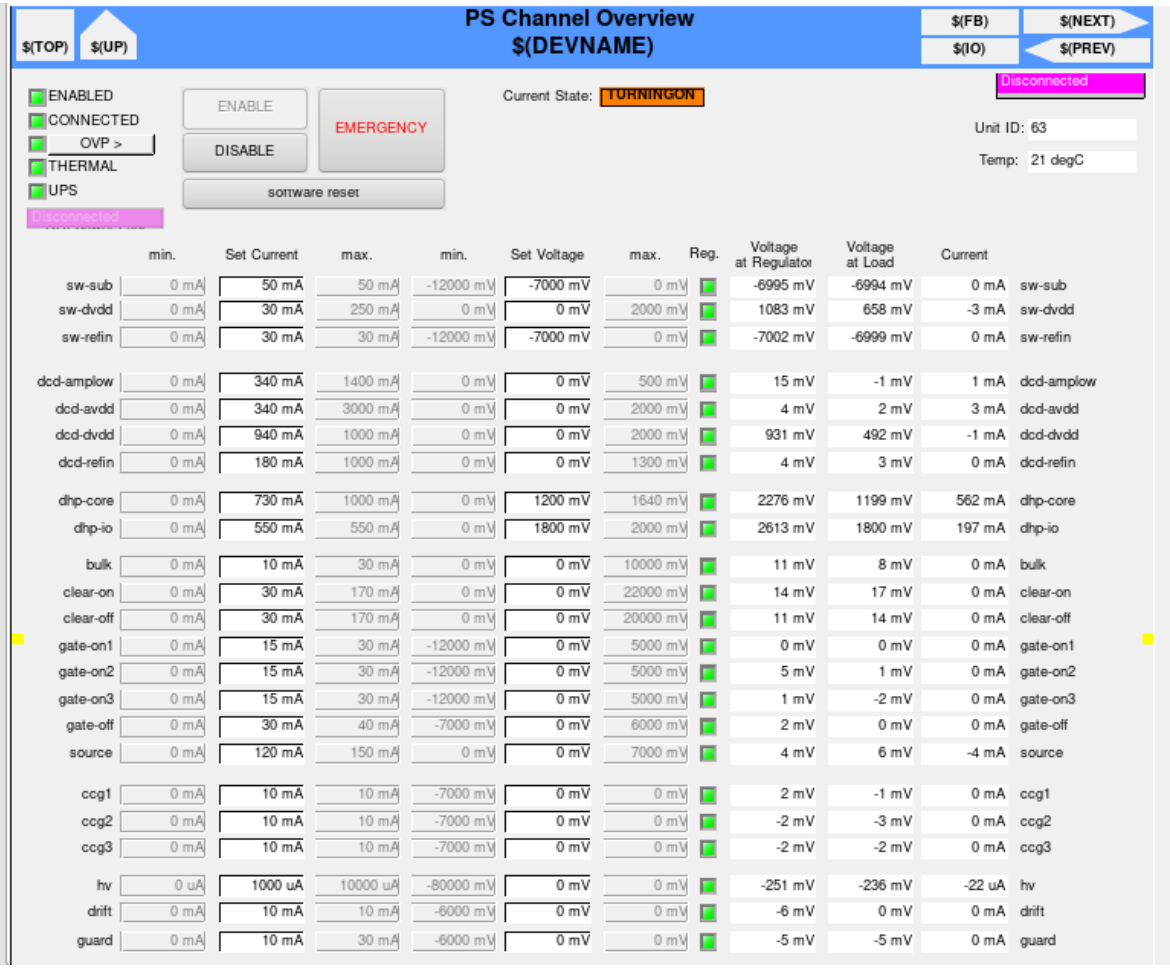
(scans executed with v0.9.2)

First powerup

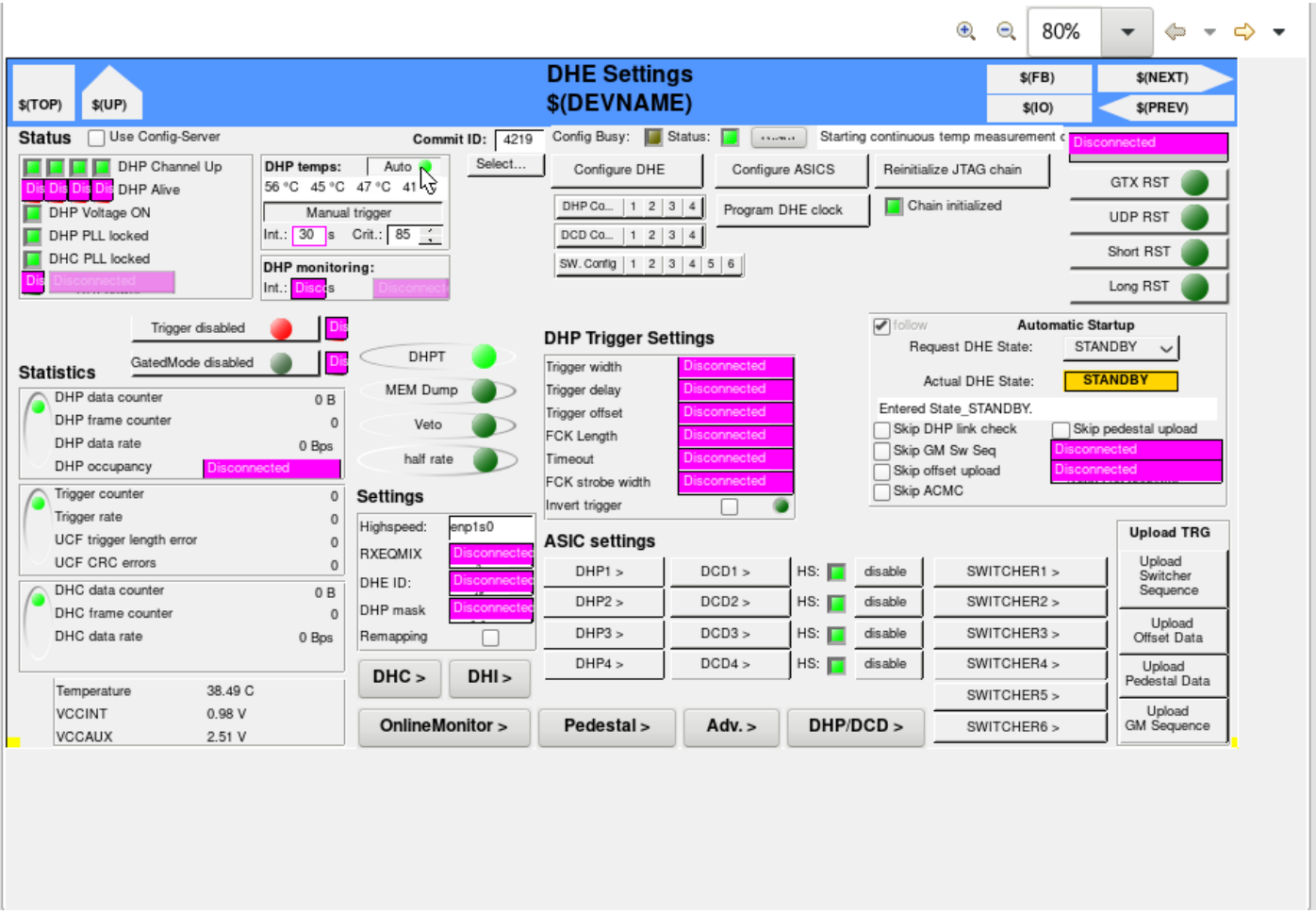
- https://elog.belle2.org/elog/PXD-Mass-Testing/22480

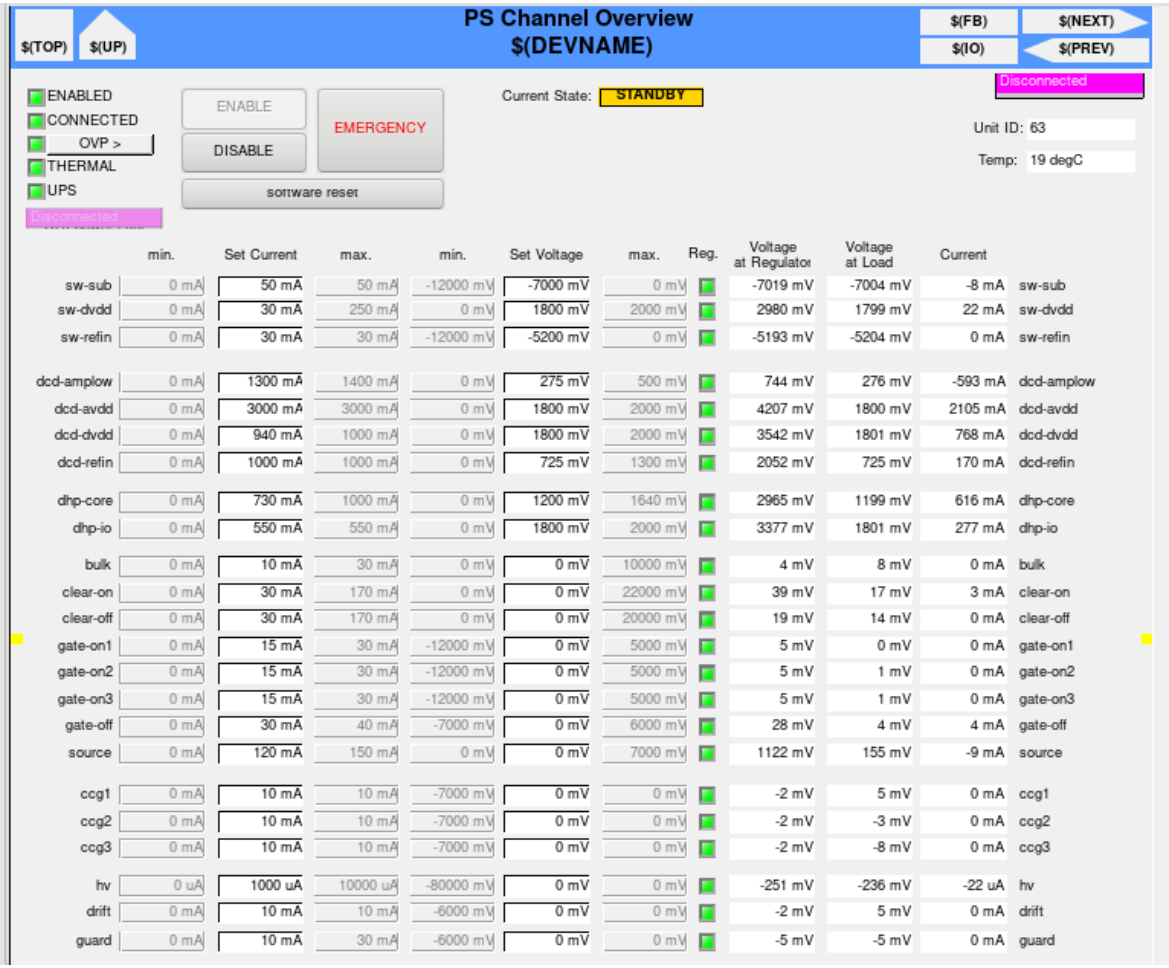
VOLTAGE AND CURRENTS TURNINGON



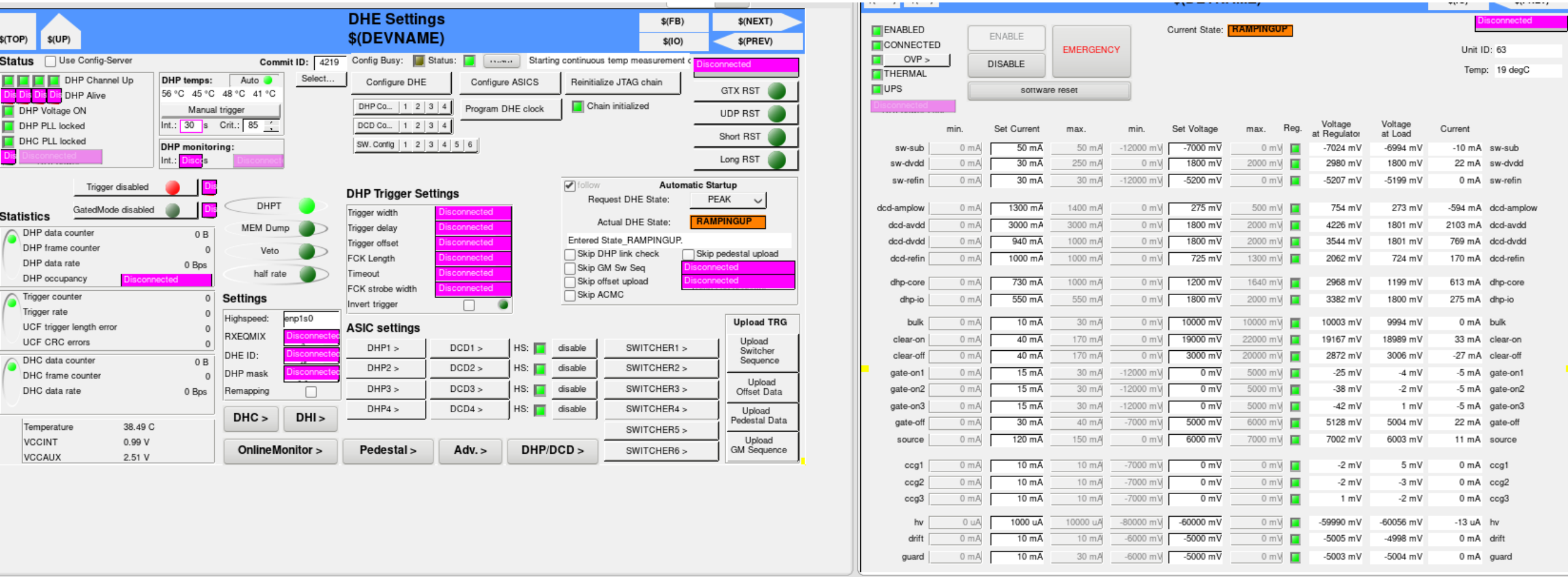


VOLTAGE AND CURRENTS STANDBY

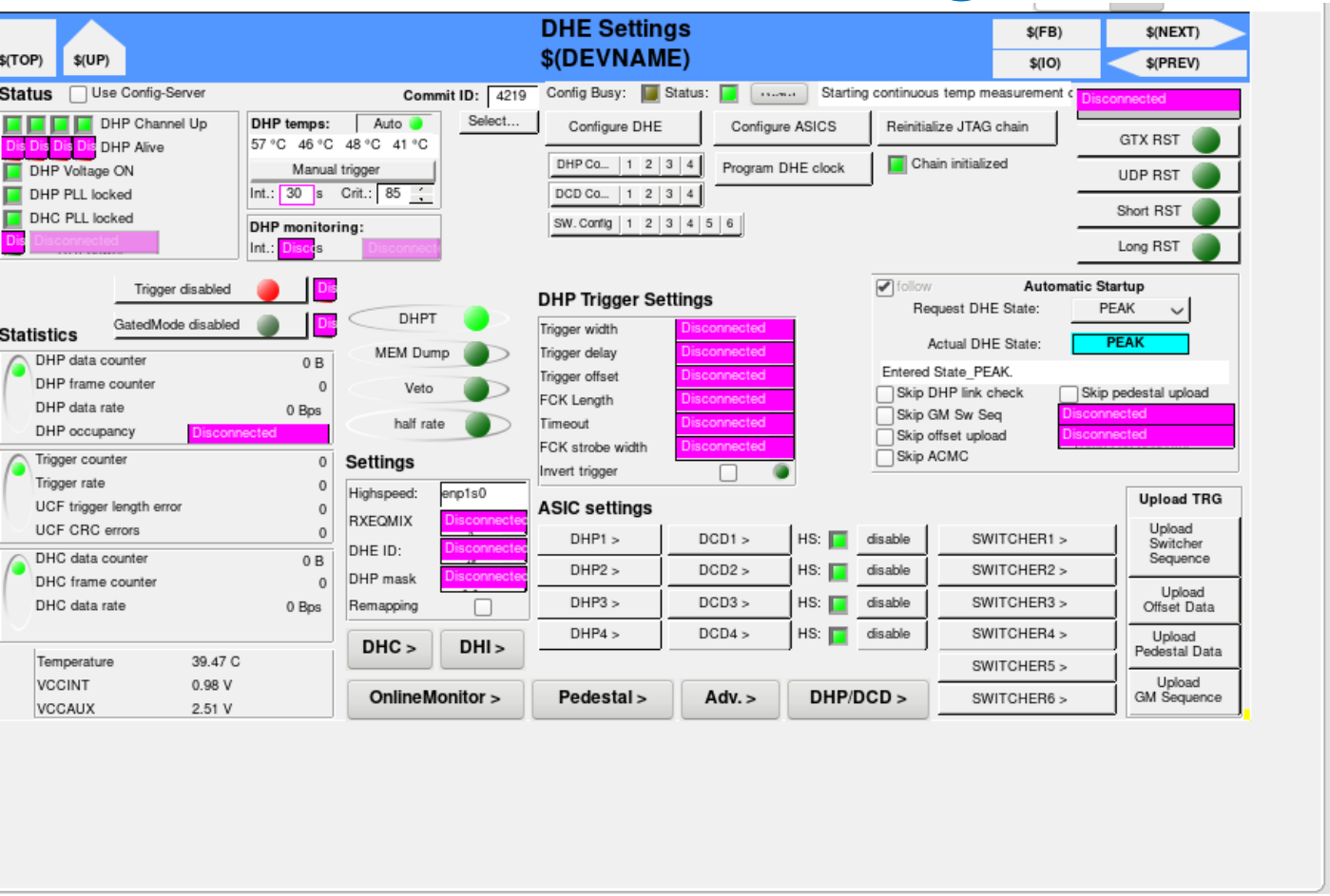


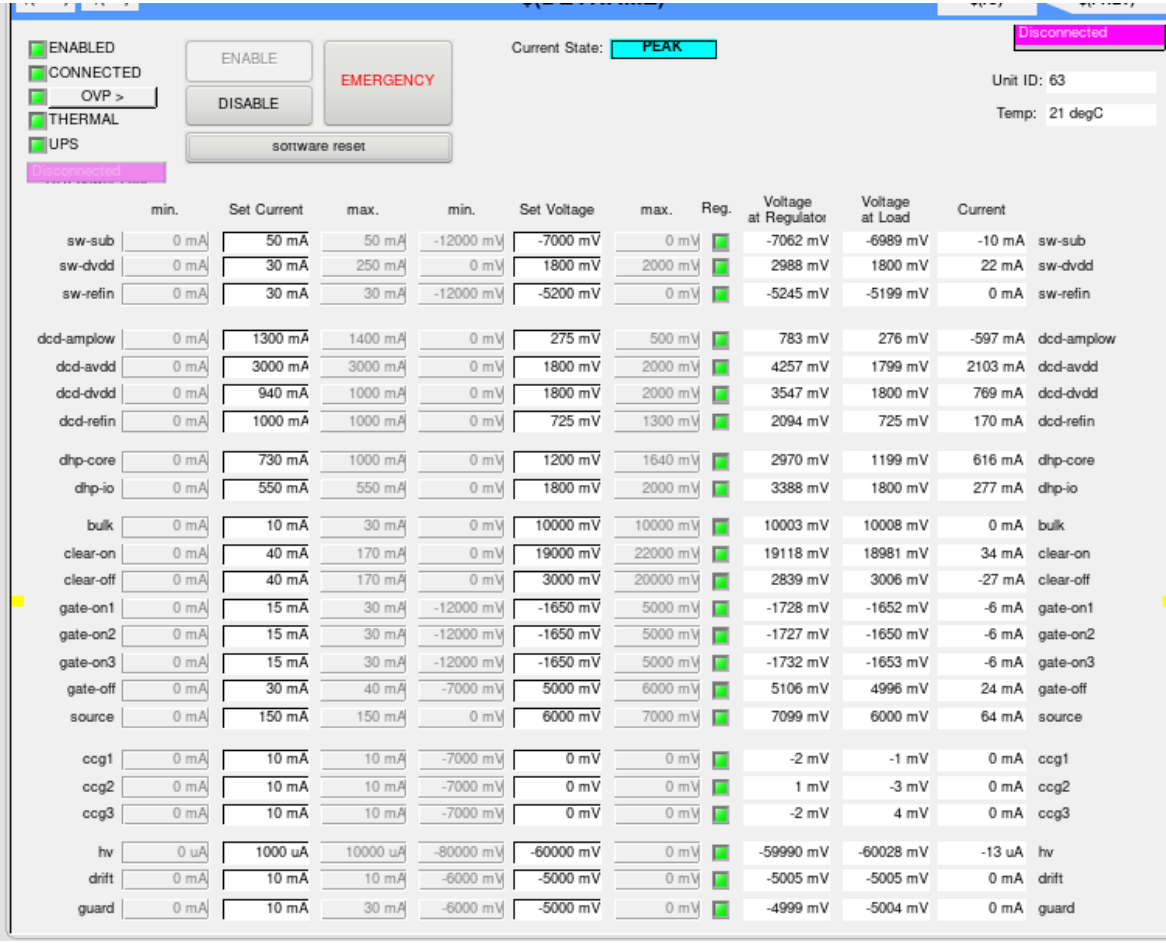


VOLTAGE AND CURRENTS
PEAK gate-on = 0V

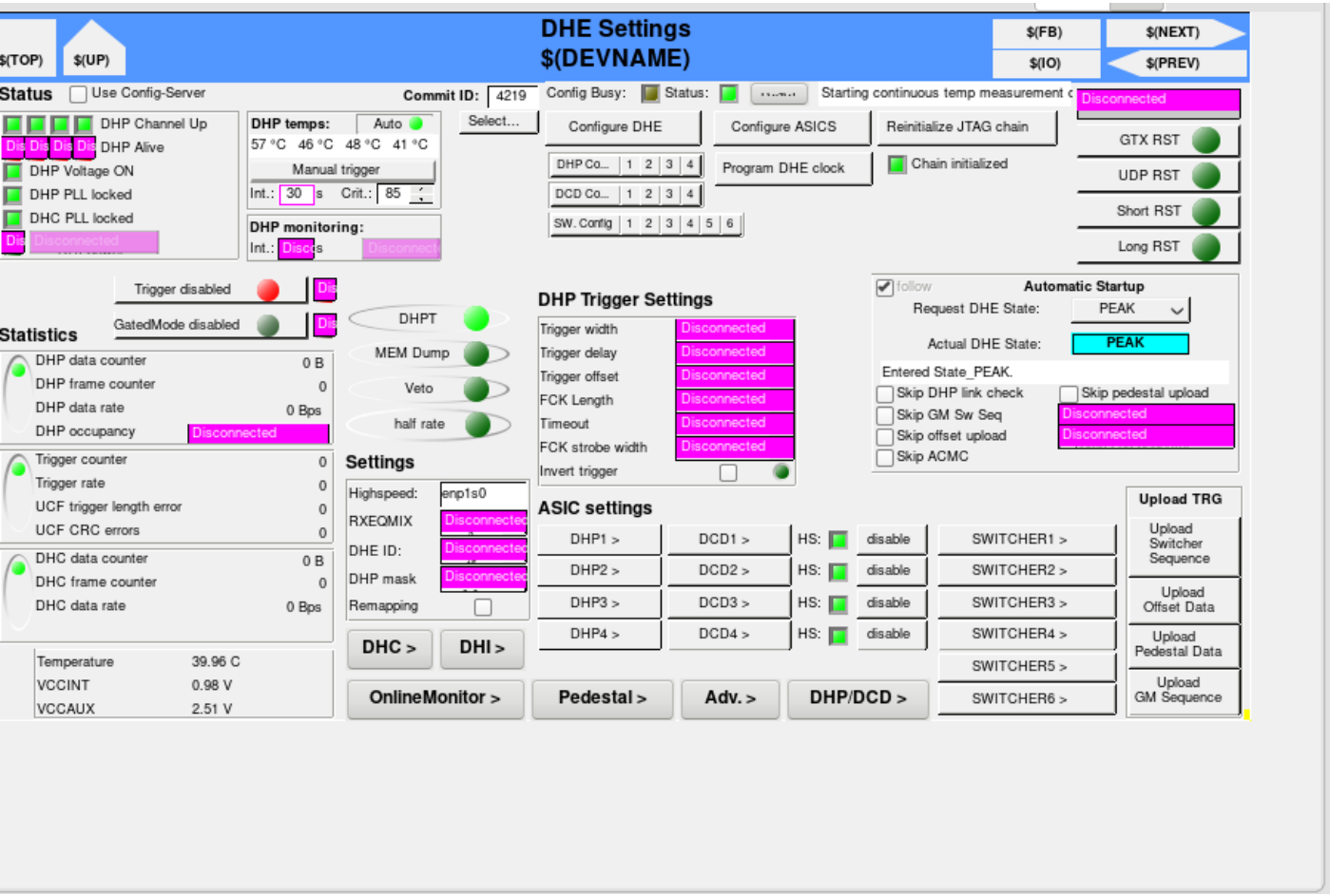


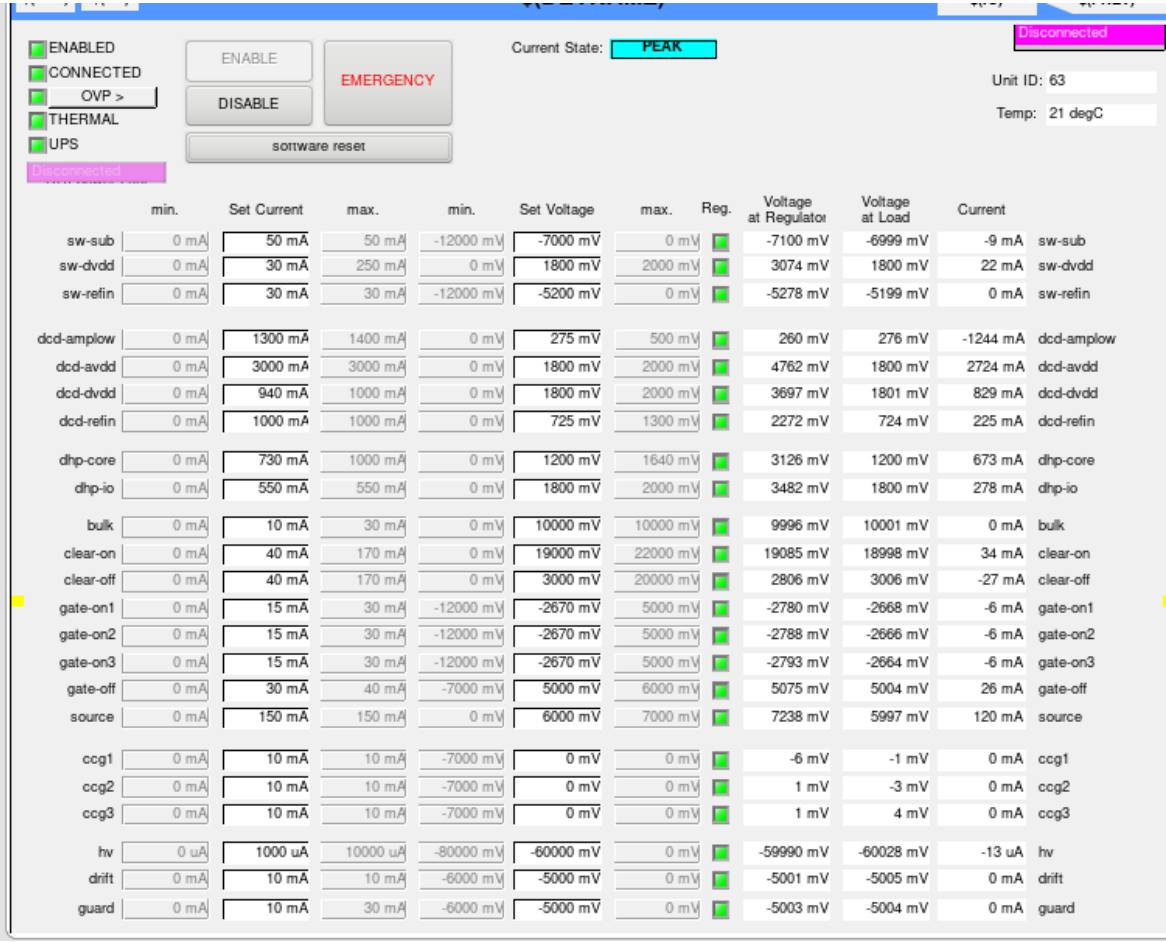
VOLTAGE AND CURRENTS
PEAK gate-on = -1650 V





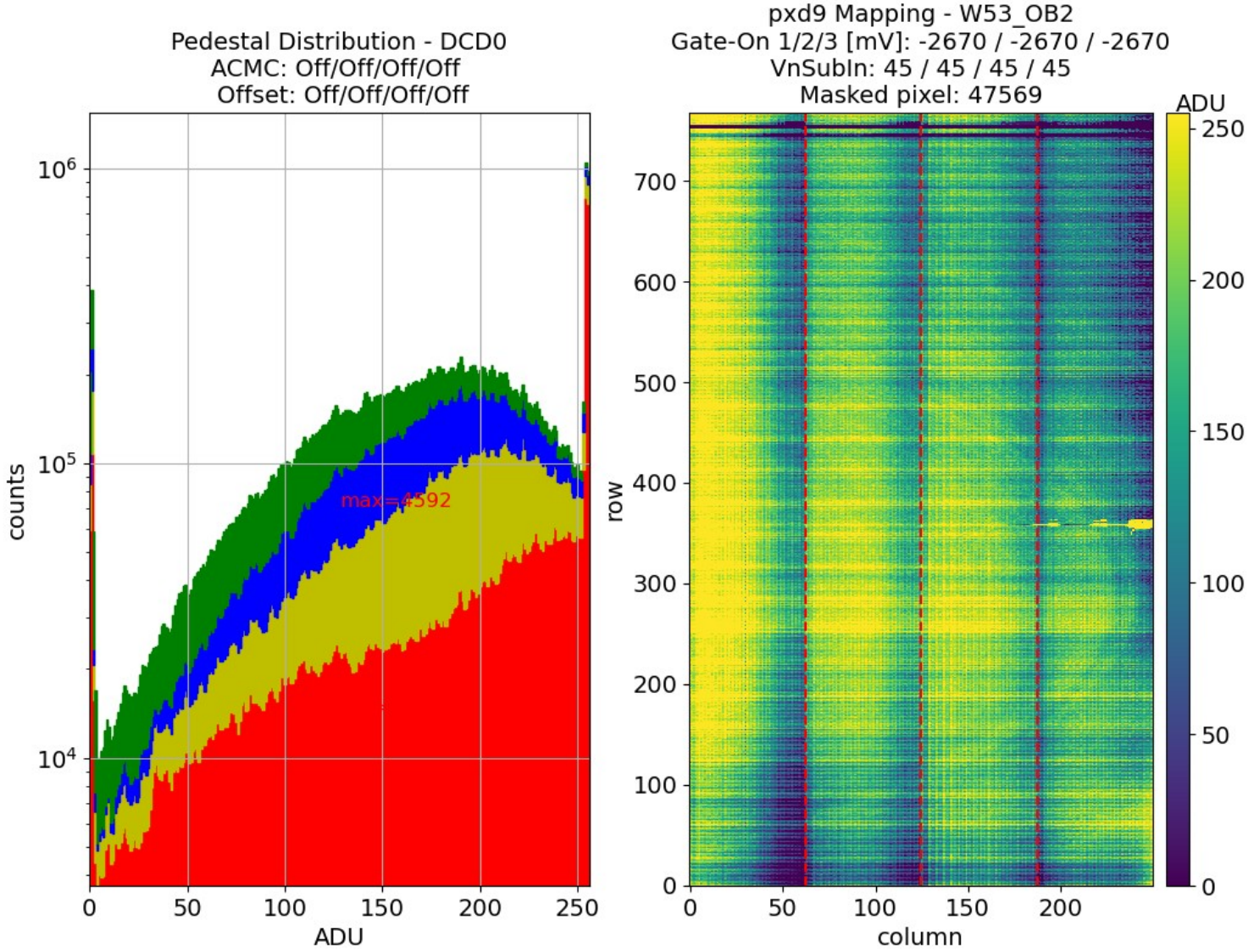
VOLTAGE AND CURRENTS
PEAK gate-on = -2780 V





First pedestals

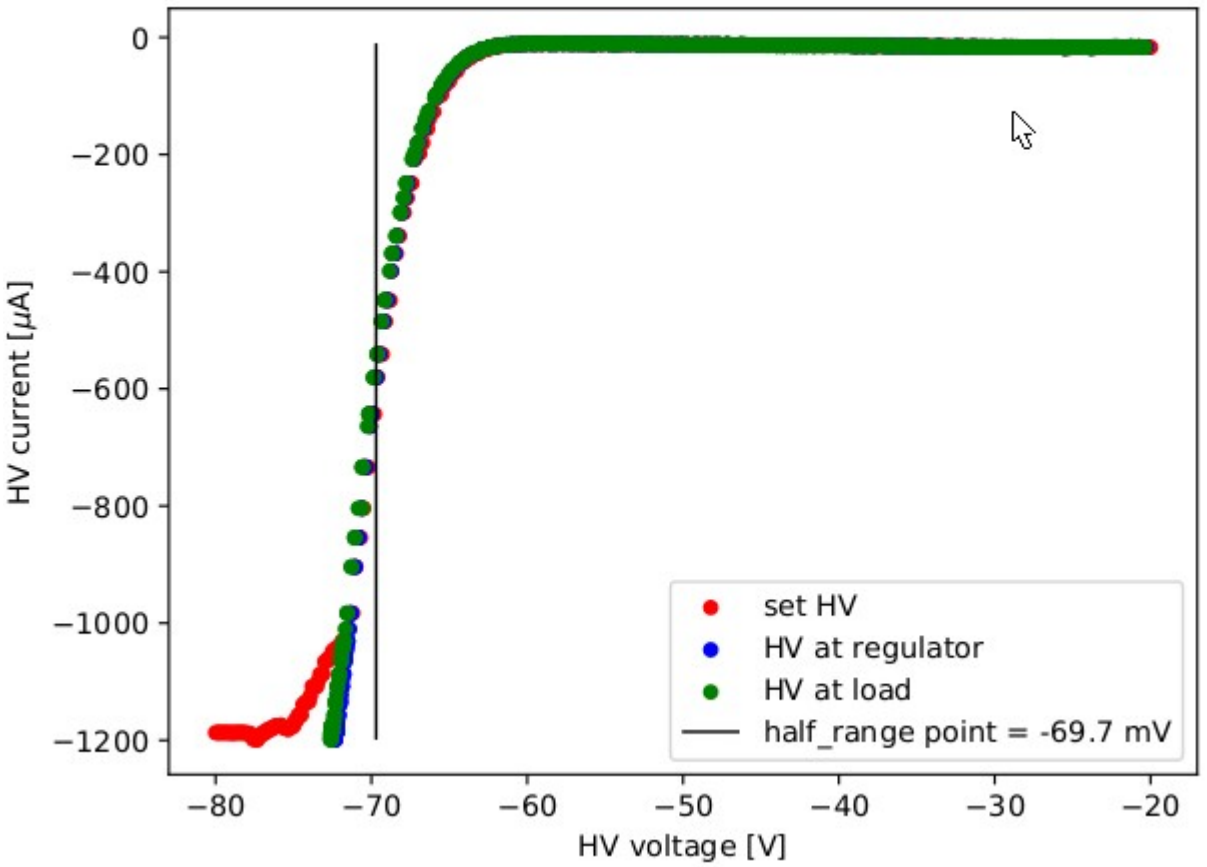
https://elog.belle2.org/elog/PXD-Mass-Testing/22482



- bad looking gates on top
- suspicious behavior at the right edge in the middle
- other than that nice

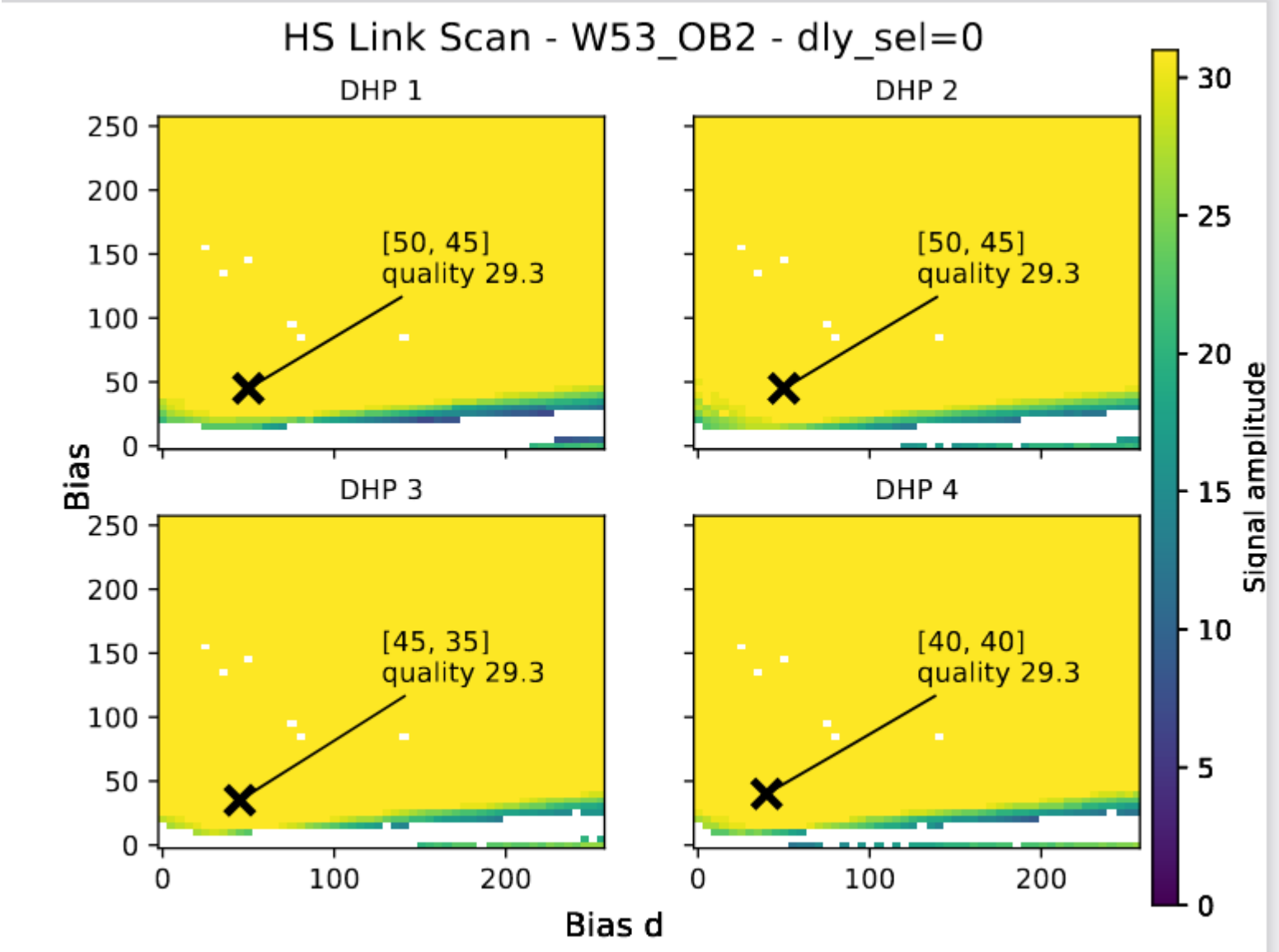
HV IV

https://elog.belle2.org/elog/PXD-Mass-Testing/22486

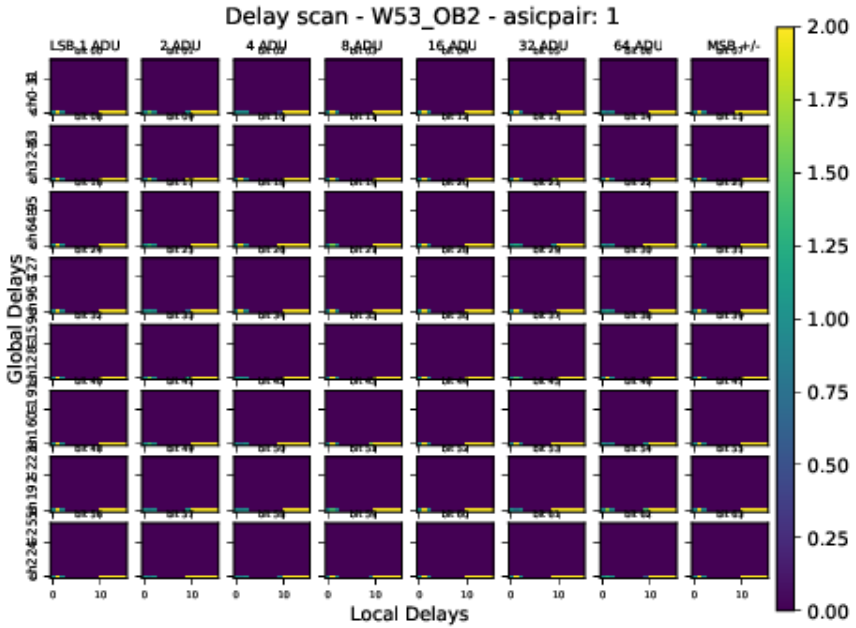


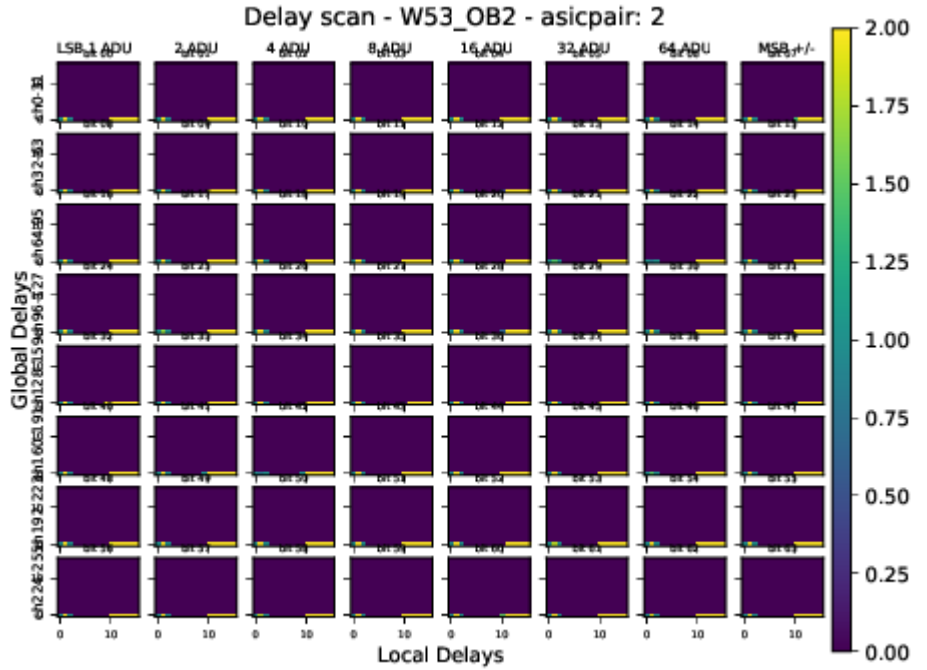
Highspeed link scan

https://elog.belle2.org/elog/PXD-Mass-Testing/22488

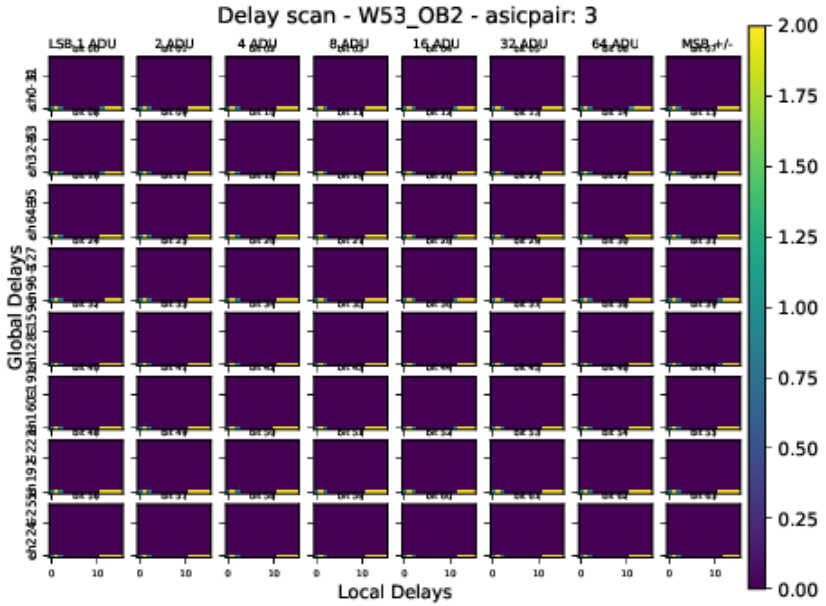


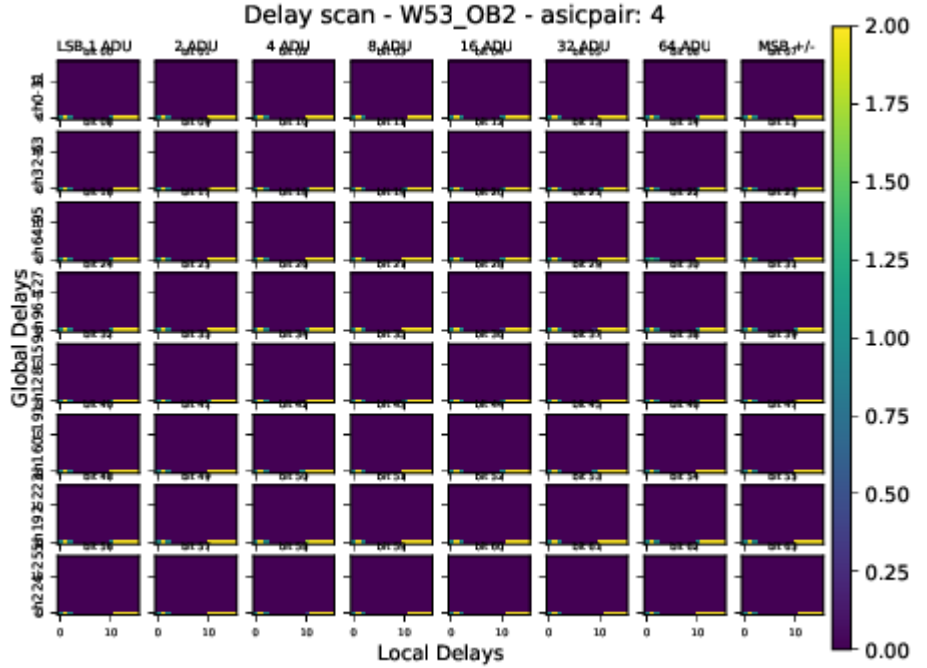
Delay scan





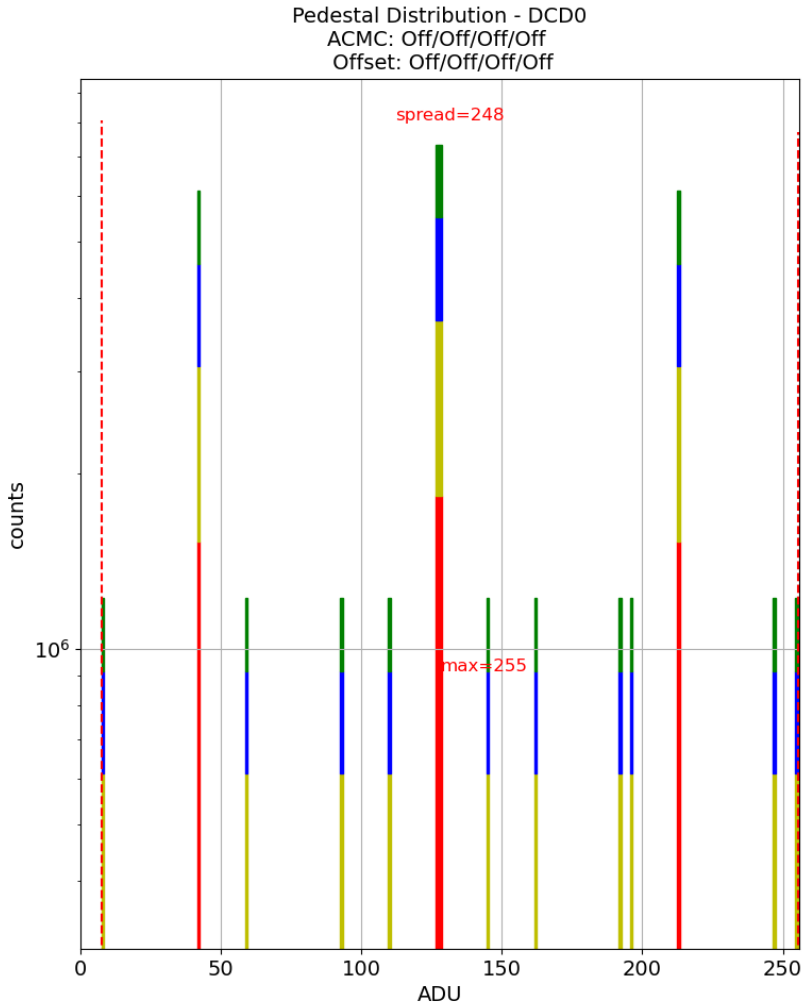
https://elog.belle2.org/elog/PXD-Mass-Testing/22490

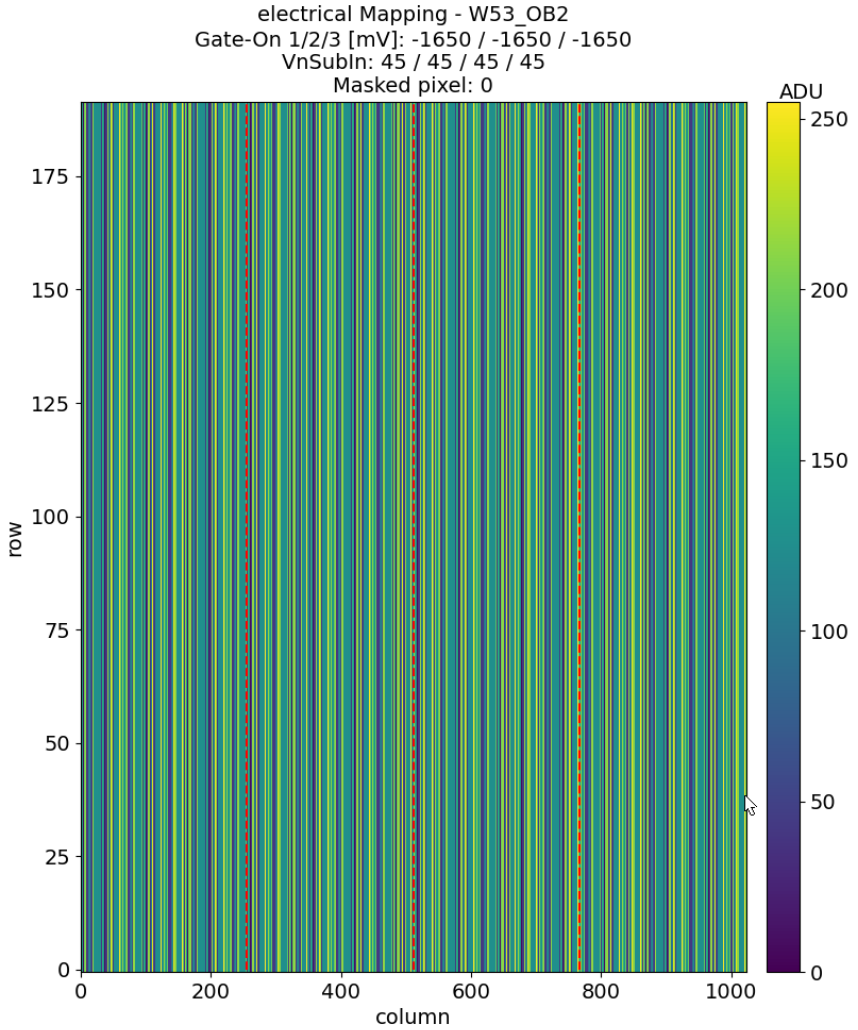




Delay check

https://elog.belle2.org/elog/PXD-Mass-Testing/22494

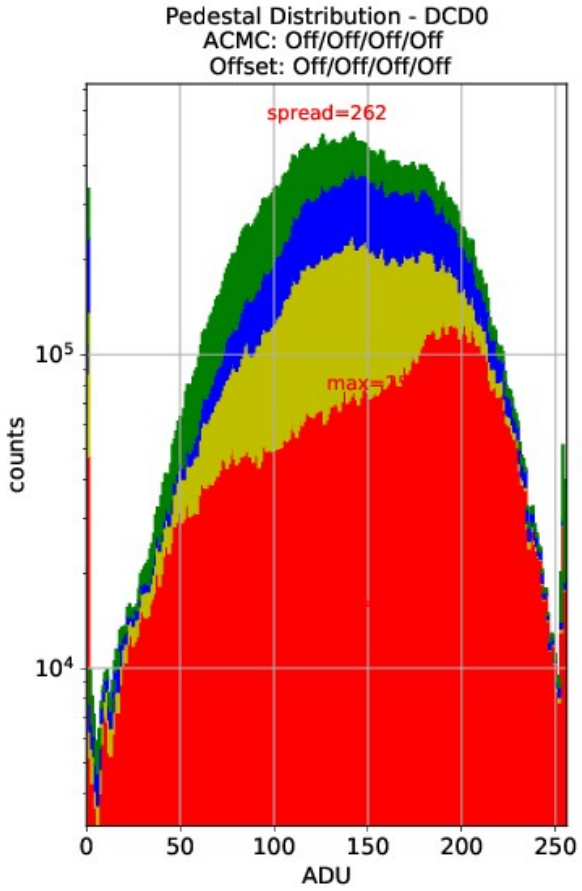


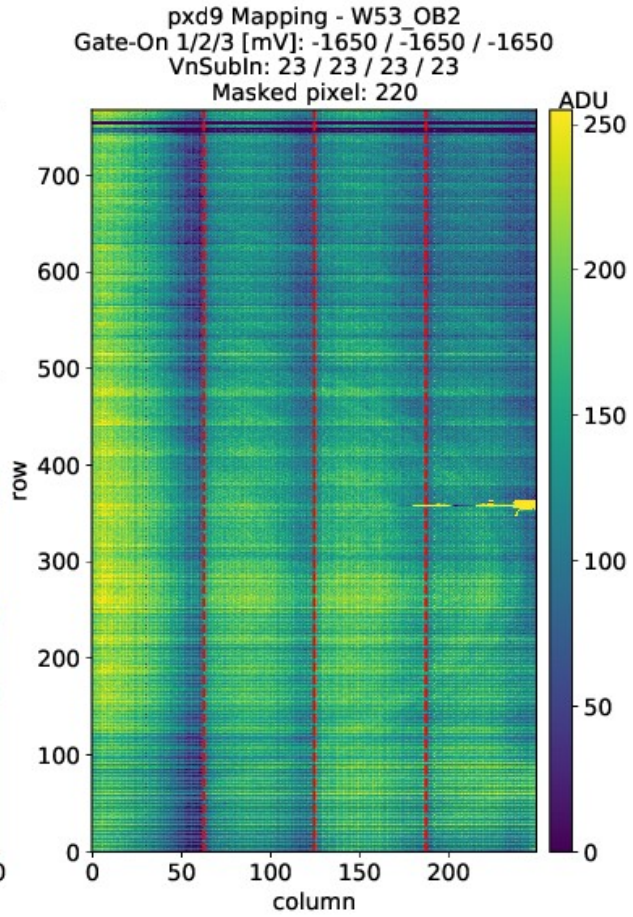


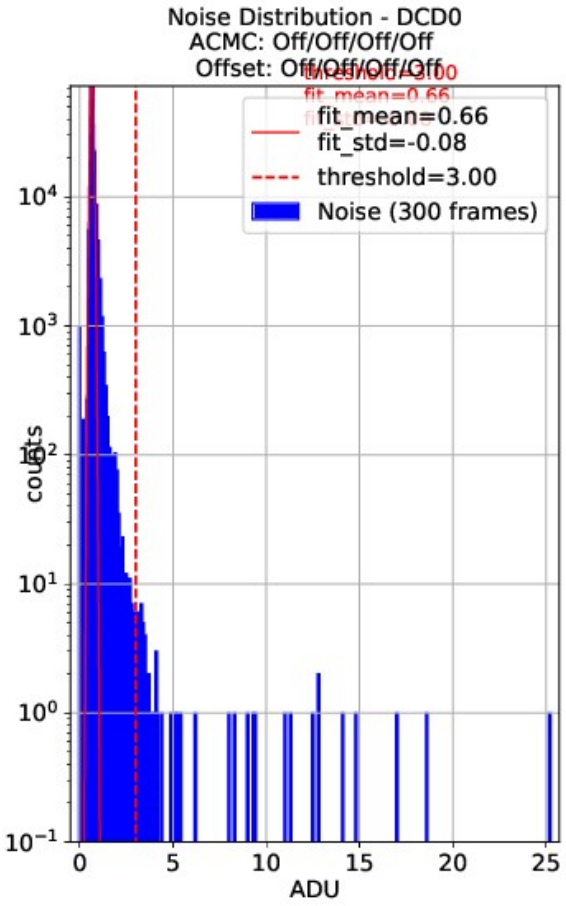
1000 frame centered pedestals

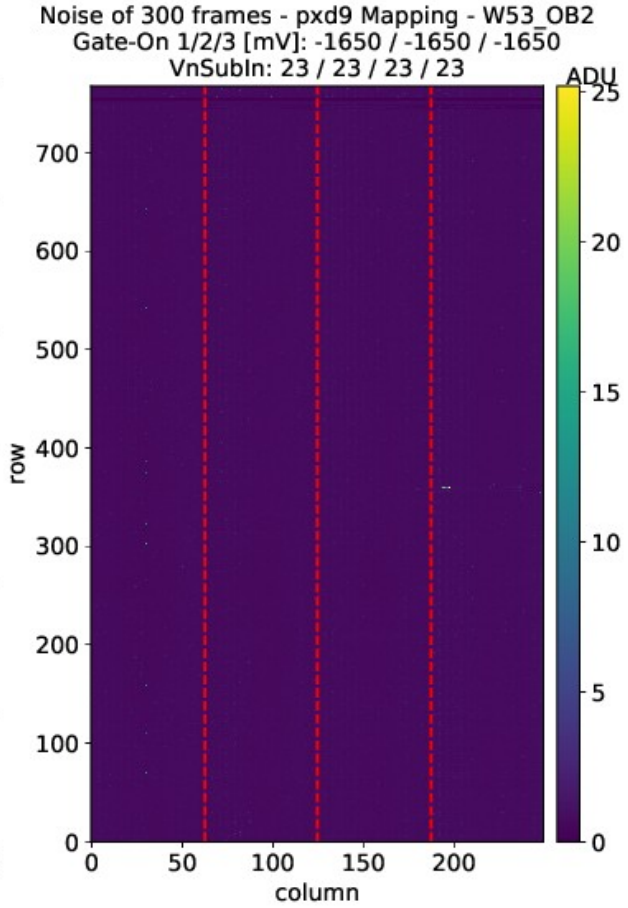
https://elog.belle2.org/elog/PXD-Mass-Testing/22496

new commit with vnsubin=23: commitid 4225









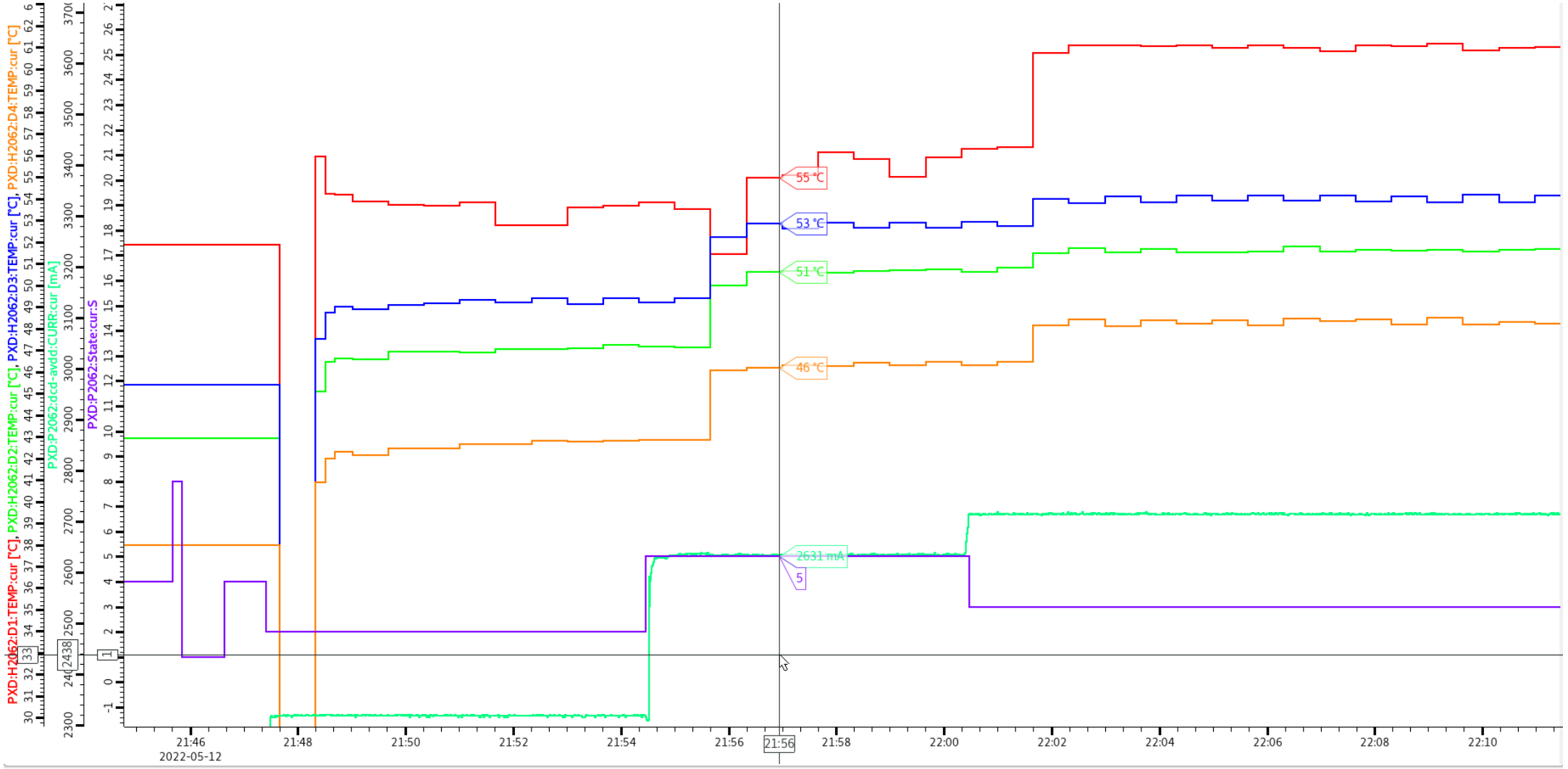
Power Cycle Scan

https://elog.belle2.org/elog/PXD-Mass-Testing/22498

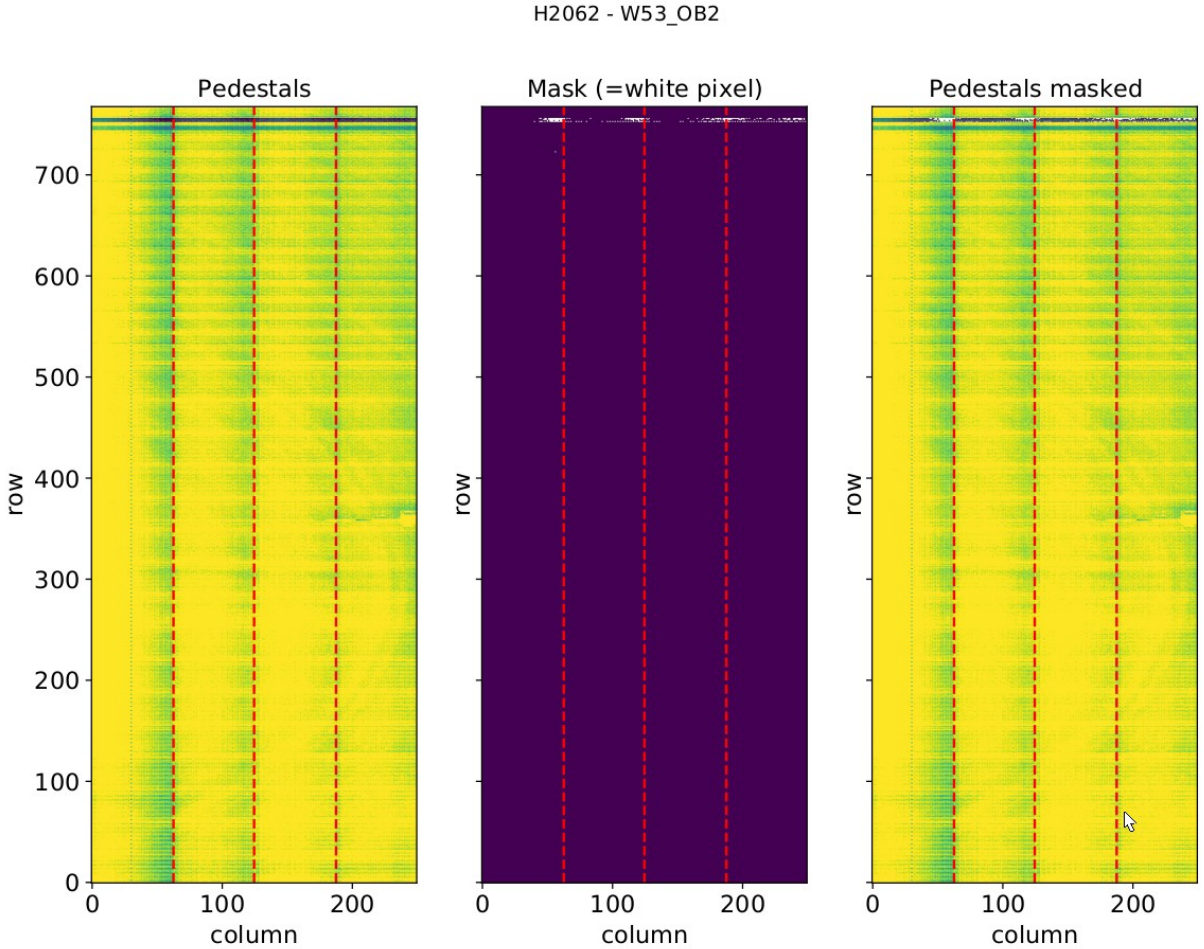
- looks like ACMC was activated in the third cycle or DCDs not correctly switched on?
  - only half dcd-amplow (600 mA)
  - only half dcd-avdd (1400 mA)
- also large pedestal differences between loops 2-3 and 3-4 correspondingly

Temperature scan

https://elog.belle2.org/elog/PXD-Mass-Testing/22499



Dead pixel map



used pedestals with vnsubin 18 (no ACMC)
https://elog.belle2.org/elog/PXD-Mass-Testing/22501

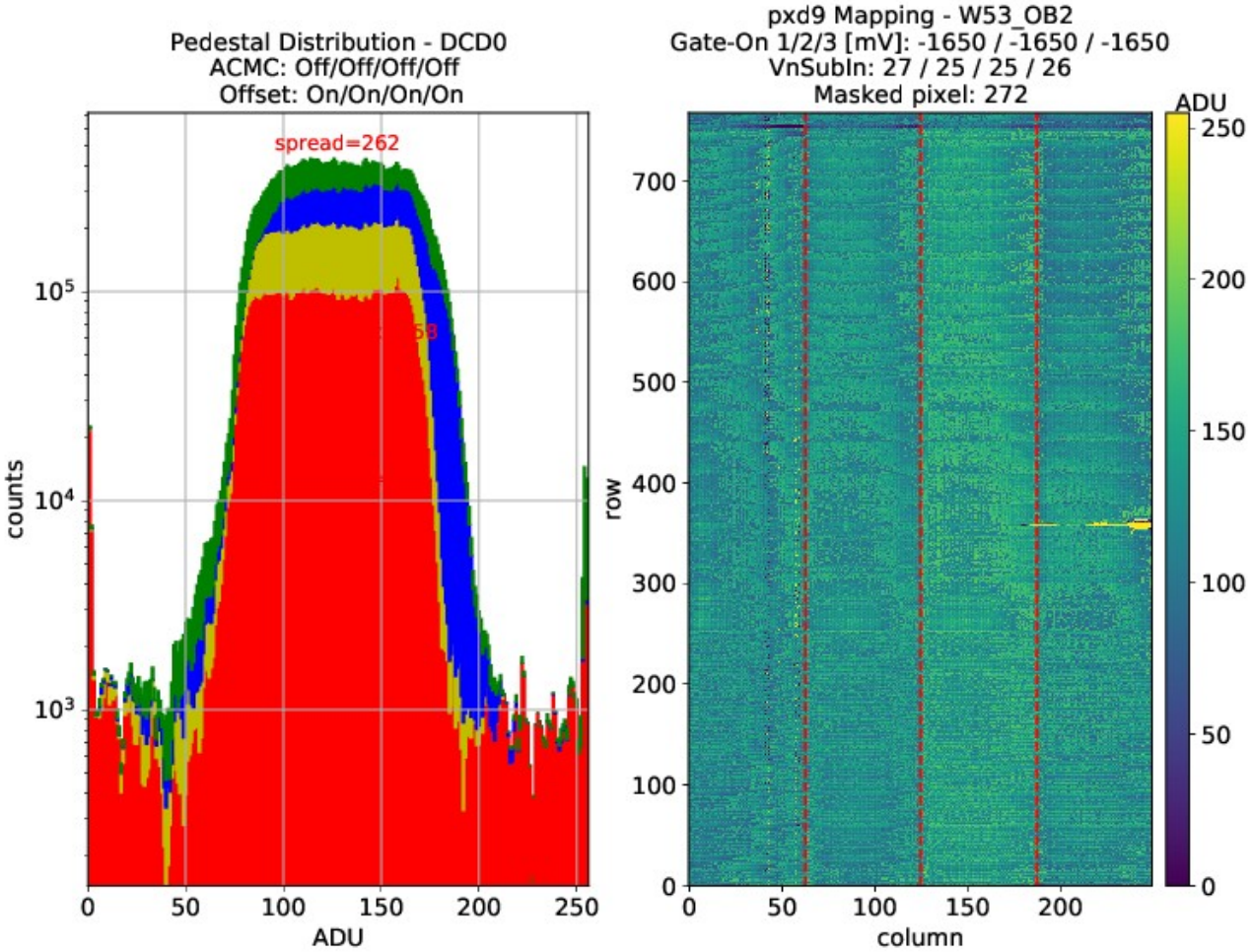
- elog upload fails with following error

```
(py36) [pxd9@silab24 pedestal]$ ./analysis_broken_drains.py -t 20
2022-05-12 22:24:13,714 analysis_broken_drains::<module>    [INFO    ]: Start of Pedestal analysis
2022-05-12 22:24:14,324 analysis_broken_drains::<module>    [INFO    ]: Save mask to /Data5/W53_OB2/pedestal_scan/2022_05_12_014/H2062/pedestal_mask/broken_drains.npy
2022-05-12 22:24:14,696 analysis_broken_drains::<module>    [WARNING]: elog.submitEntry:AttributeError("'elog' object has no attribute 'path'",)
(py36) [pxd9@silab24 pedestal]$ git status -uno
# HEAD detached at v0.9.2
nothing to commit (use -u to show untracked files)
(py36) [pxd9@silab24 pedestal]$
```

Offset scan

start with vnsubin [26, 25, 25, 25]

https://elog.belle2.org/elog/PXD-Mass-Testing/22503

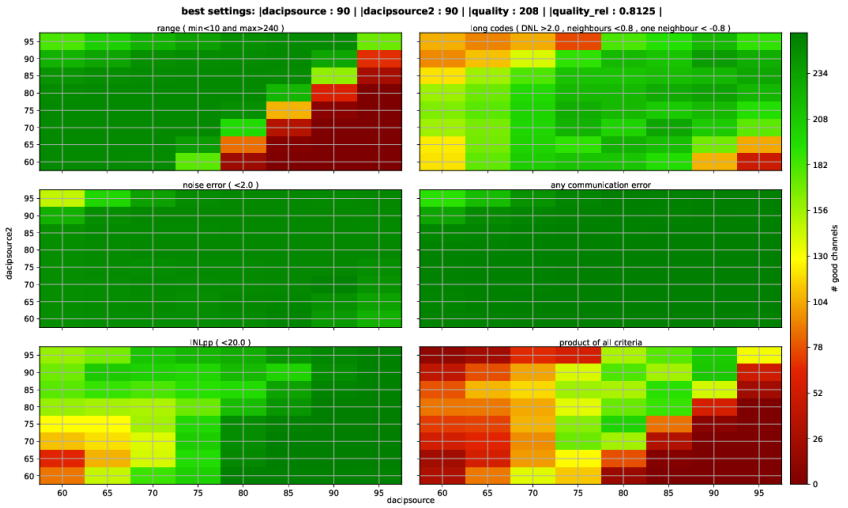


- changed vnsubin to [27, 25, 25, 26]
- commitid 4227
- <- resulting pedestals https://elog.belle2.org/elog/PXD-Mass-Testing/22505
- nice, but some fishy offset lines in right part of leftmost DCD..

ADC scan ipsource-ipsource2

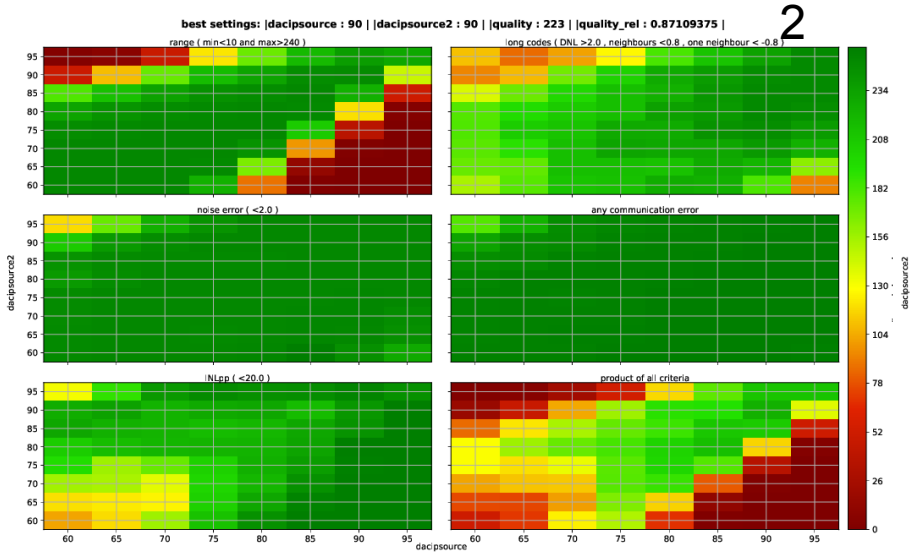
https://elog.belle2.org/elog/PXD-Mass-Testing/22507

1

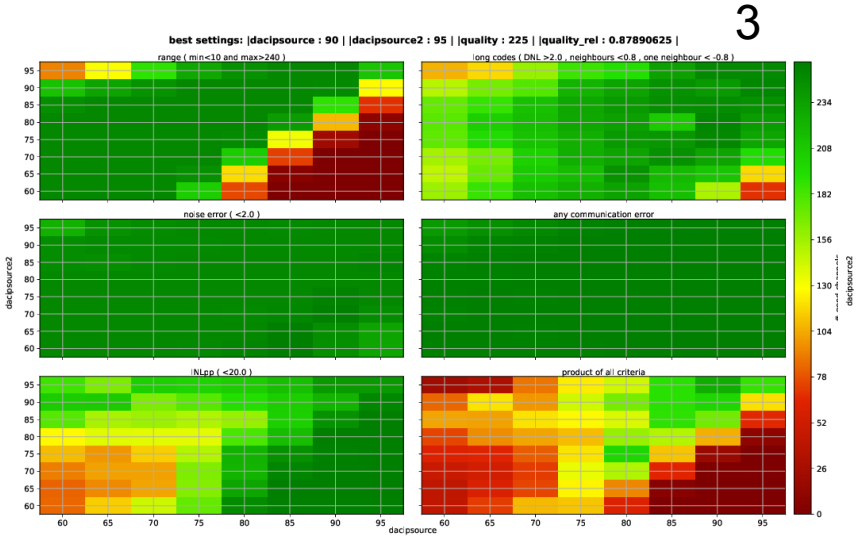


- active_gate = 123
- ips/ips2: [90/90, 90/90, 90/95, 90/80]
- INL: [13, 14, 14, 17]
- grade A channels: [208, 223, 225, 176]
- grade B channels: [40, 27, 25, 74]
- dead channels: [2, 0, 0, 0]
- good 998, dead 2
- it looks like low INL and range criteria are mutually excluding each other

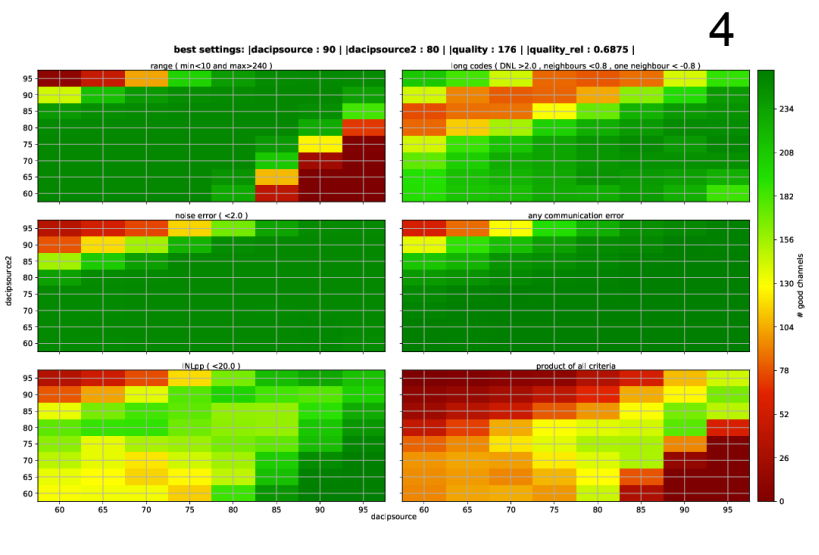
2



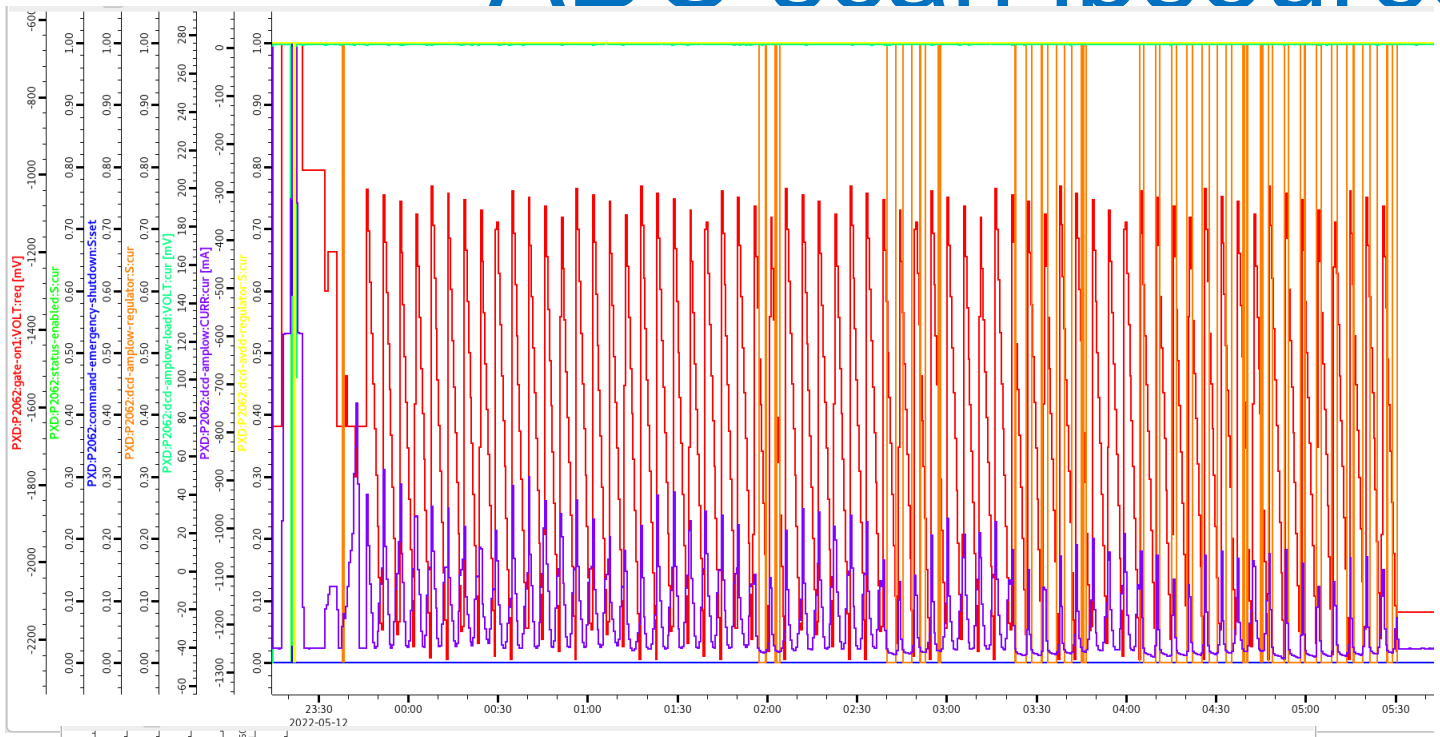
3

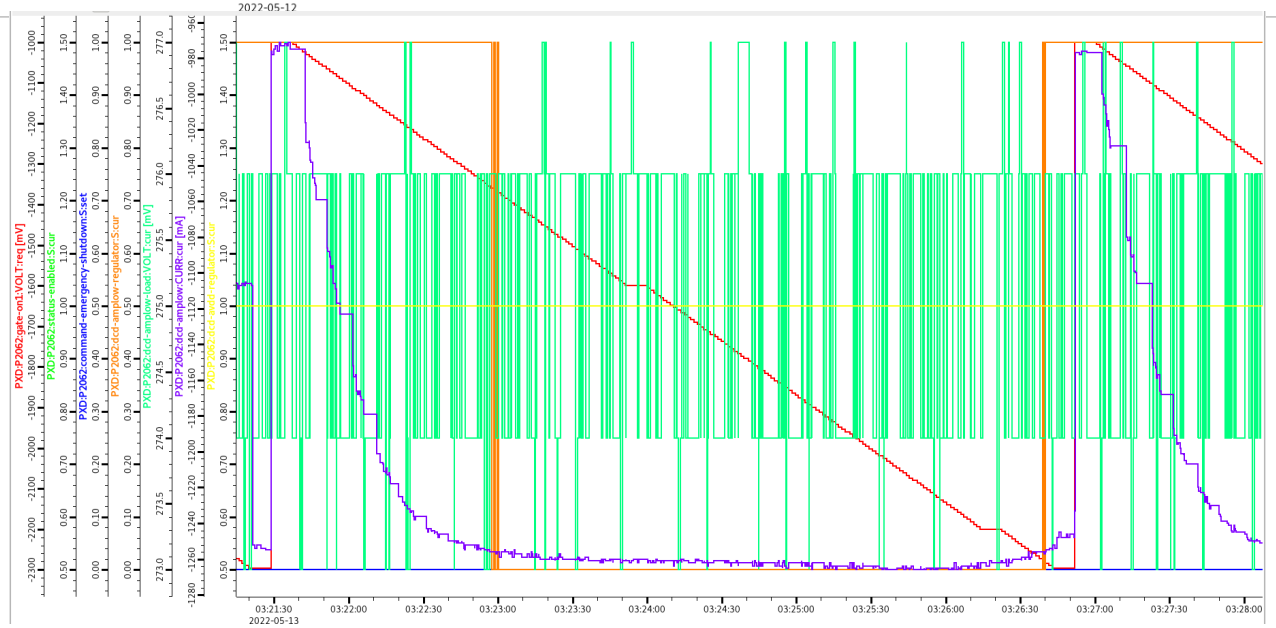


4



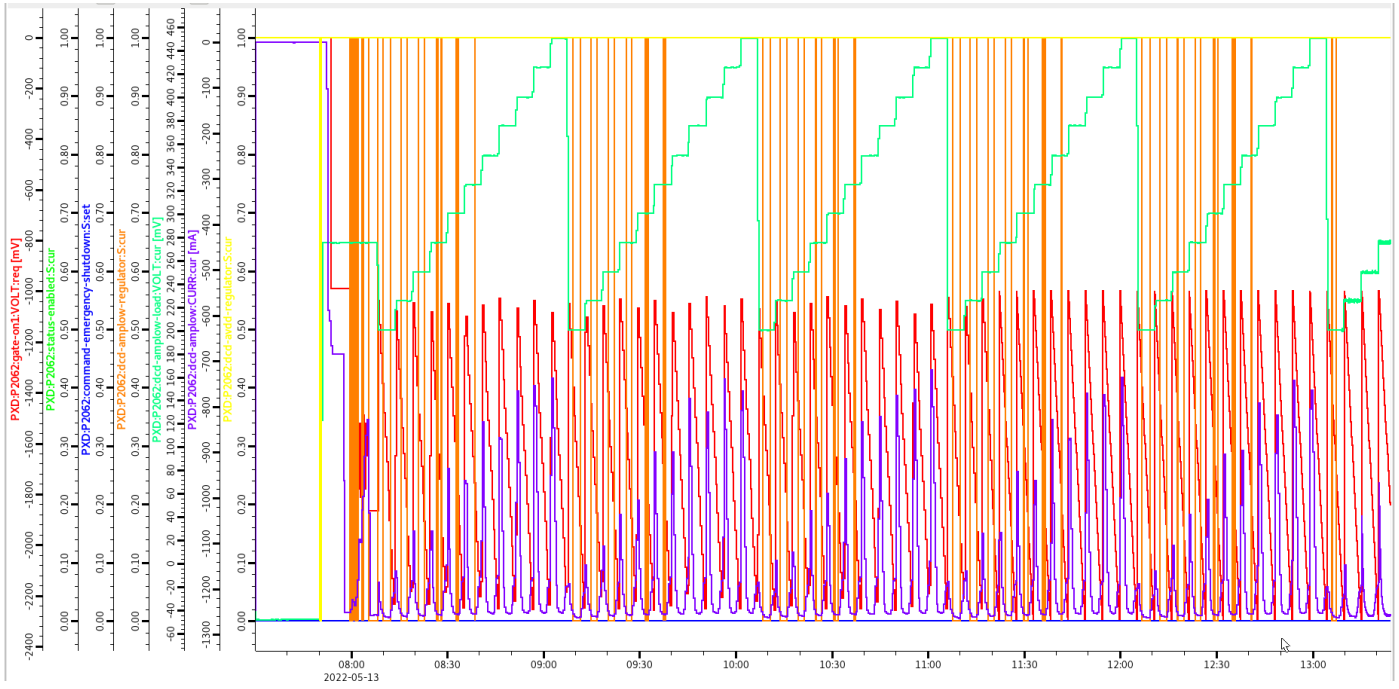
ADC scan ipsource-ipsource2

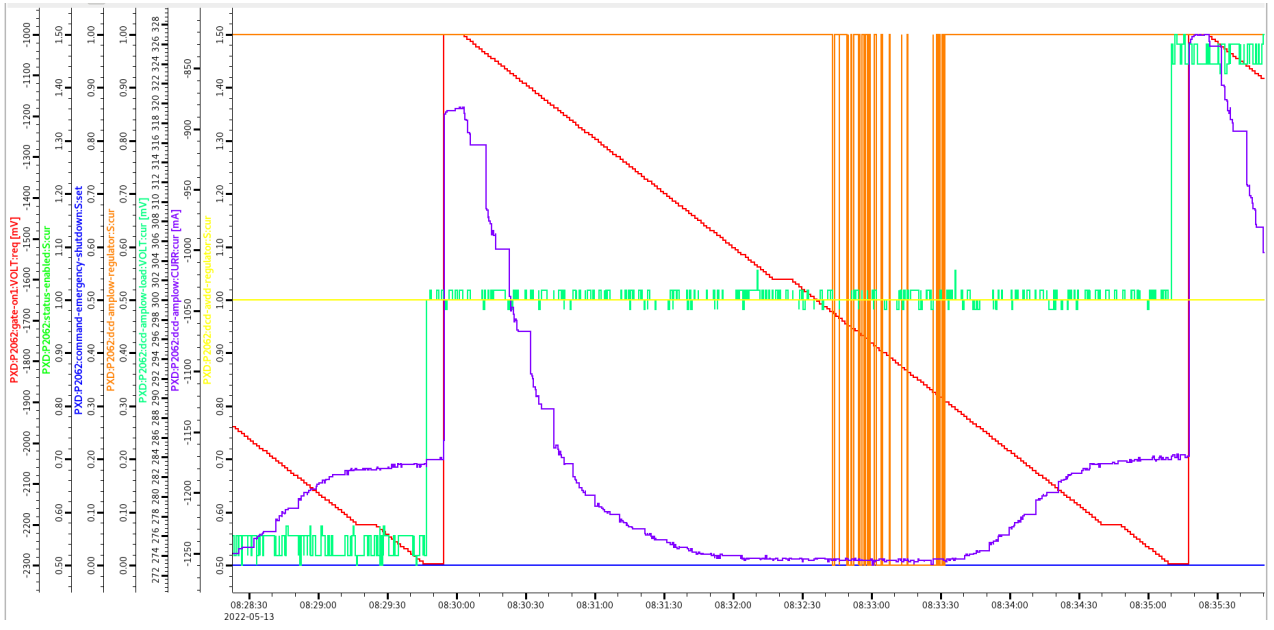




- after the measurement it was seen that the amplow regulator went into cc mode during several curves (orange spikes)
- but the amplow sensed voltage did not seem to be affected

ADC scan refin-amplow

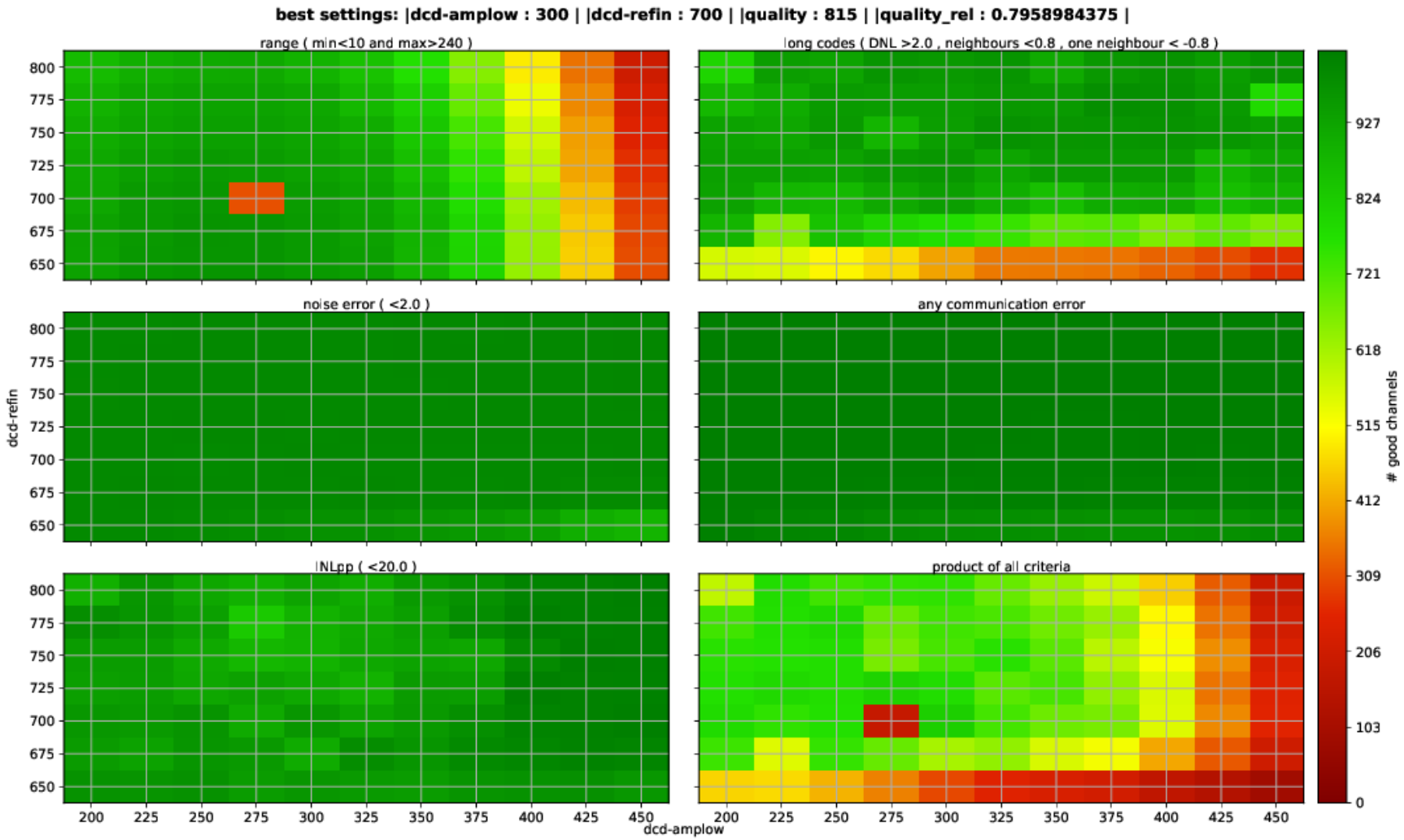




- also during amplow-refin scan the amplow limit was reached
- limit increased to 1400 mA at ~13:10

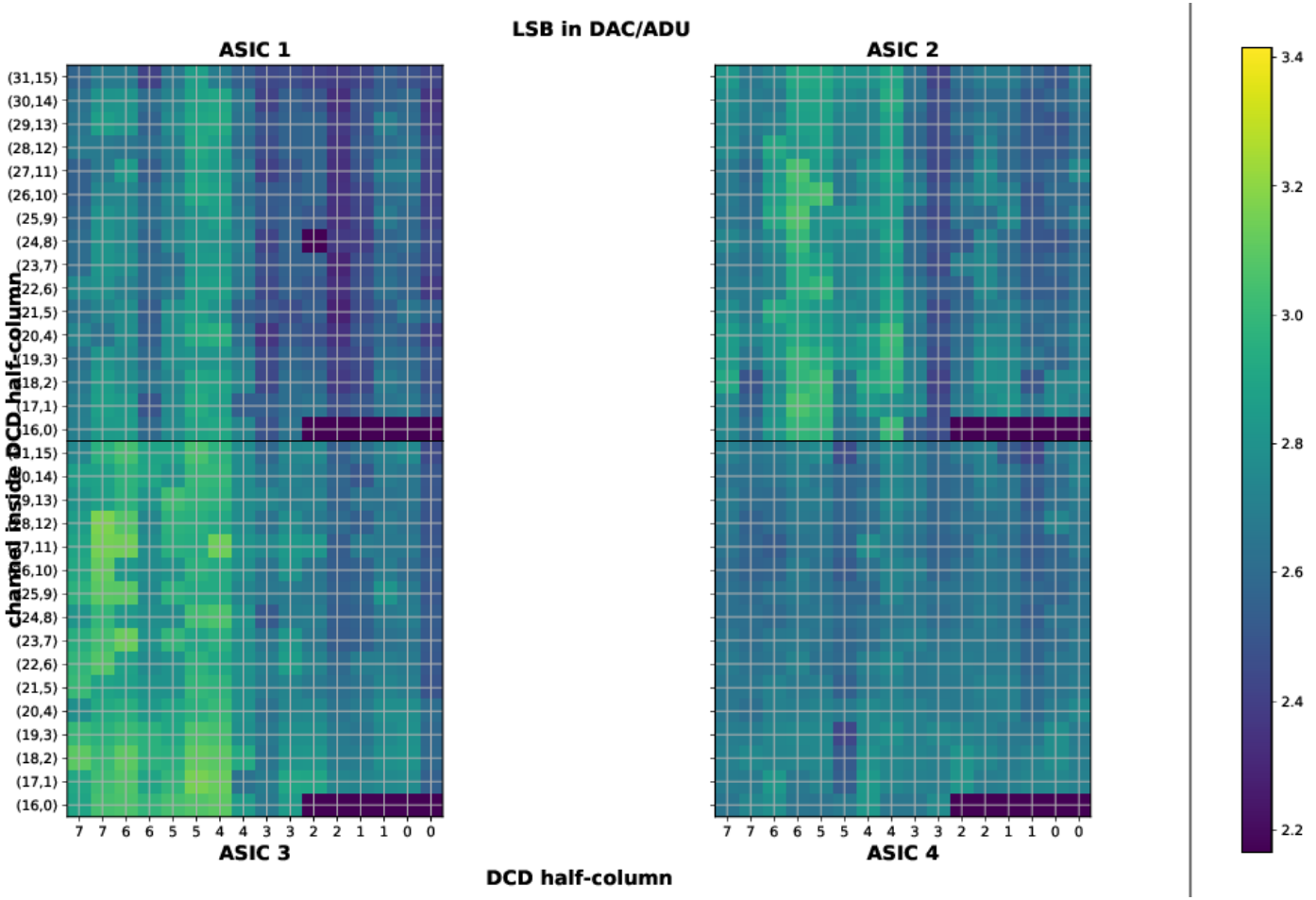
ADC scan refin-amplow

https://elog.belle2.org/elog/PXD-Mass-Testing/22509



ADC scan

ifbpbias https://elog.belle2.org/elog/PXD-Mass-Testing/22511
ipsourcemiddle: https://elog.belle2.org/elog/PXD-Mass-Testing/22513
allchannels working point: https://elog.belle2.org/elog/PXD-Mass-Testing/22515



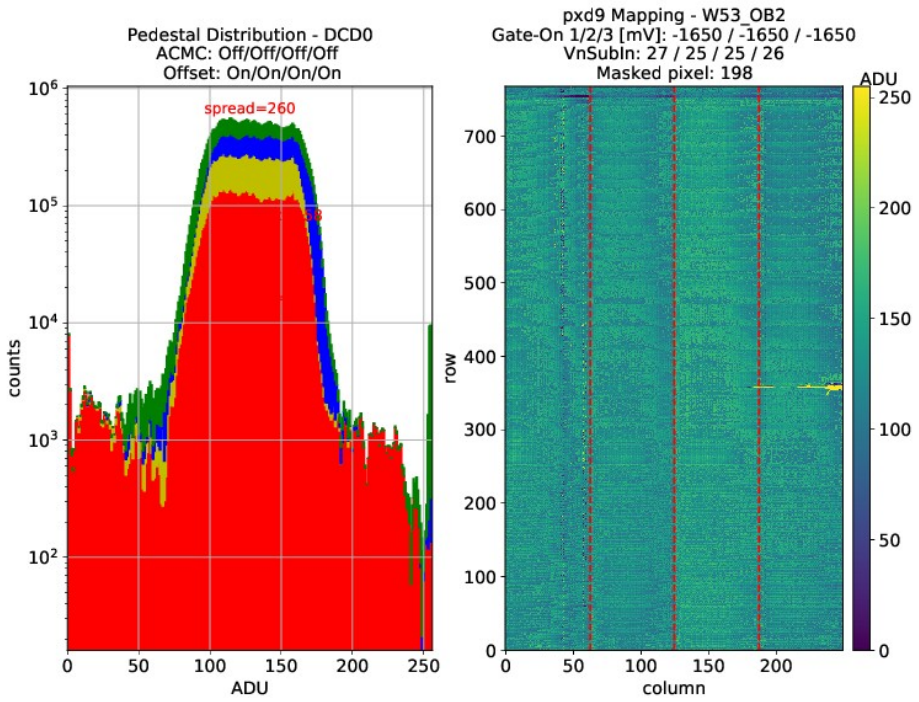

```
recorded channels: 1000
gradeA        channels: 761
gradeB        channels: 234
gradeF (DEAD) channels: 5

median (mean)
INL   : 14.11   (14.68)
noise: 0.91    (0.92)
LSB   : 2.68    (2.70)

Result: alive_channels 99.50 A
Comment: channels total 1000 | good 995
| dead 5
```

Commit update 4231

```
(py36) [pxd9@silab24 adc_curve]$ ./update.py --db -id 4227 -f /Data5/W53_OB2/adc_curve/gate/ipsource-ipsource2/2022_05_12_001/analysis.npy
2022-05-13 20:34:10,394 update::<module>   [INFO   ]: updating configDB commitID 4227 with data from /Data5/W53_OB2/adc_curve/gate/ipsource-ipsource2/2022_05_12_001/analysis.npy
Created new commit #4228
Commit successful

(py36) [pxd9@silab24 adc_curve]$ ./update.py --db -id 4228 -f /Data5/W53_OB2/adc_curve/gate/dcd-refin-dcd-amplow/2022_05_13_002/analysis.npy
2022-05-13 20:35:09,638 update::<module>   [INFO   ]: updating configDB commitID 4228 with data from /Data5/W53_OB2/adc_curve/gate/dcd-refin-dcd-amplow/2022_05_13_002/analysis.npy
Created new commit #4229
Commit successful

(py36) [pxd9@silab24 adc_curve]$ ./update.py --db -id 4229 -f /Data5/W53_OB2/adc_curve/gate/ifbpbias/2022_05_13_001/analysis.npy
2022-05-13 20:35:34,664 update::<module>   [INFO   ]: updating configDB commitID 4229 with data from /Data5/W53_OB2/adc_curve/gate/ifbpbias/2022_05_13_001/analysis.npy
Created new commit #4230
Commit successful

(py36) [pxd9@silab24 adc_curve]$ ./update.py --db -id 4230 -f /Data5/W53_OB2/adc_curve/gate/ipsource_middle/2022_05_13_001/analysis.npy
2022-05-13 20:36:02,128 update::<module>   [INFO   ]: updating configDB commitID 4230 with data from /Data5/W53_OB2/adc_curve/gate/ipsource_middle/2022_05_13_001/analysis.npy
Created new commit #4231
Commit successful
```

Pedestals after power cycle

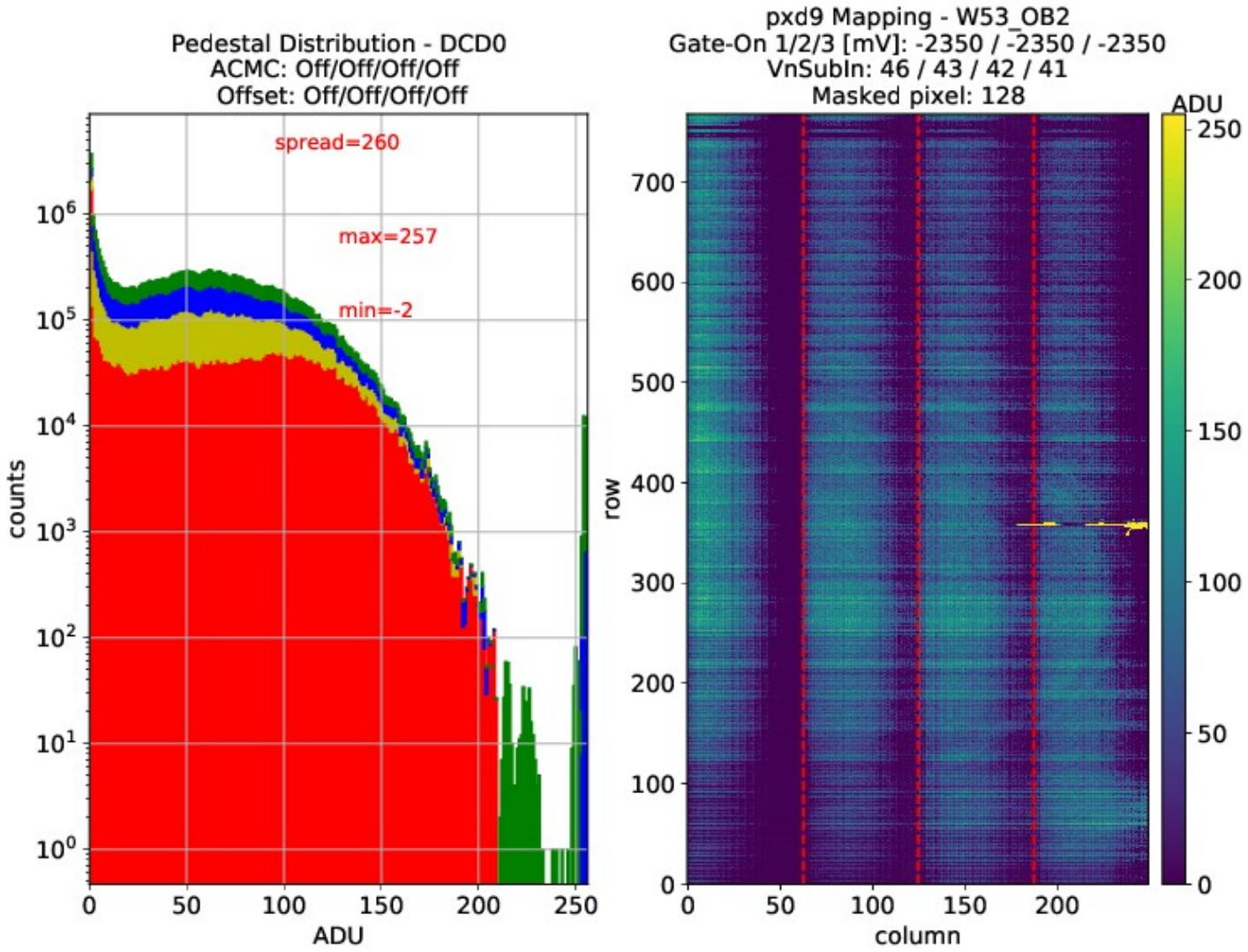
https://elog.belle2.org/elog/PXD-Mass-Testing/22517



Pedestals commit 4232 before offset 2

https://elog.belle2.org/elog/PXD-Mass-Testing/22519

vnsubin = [46, 43, 42, 41]



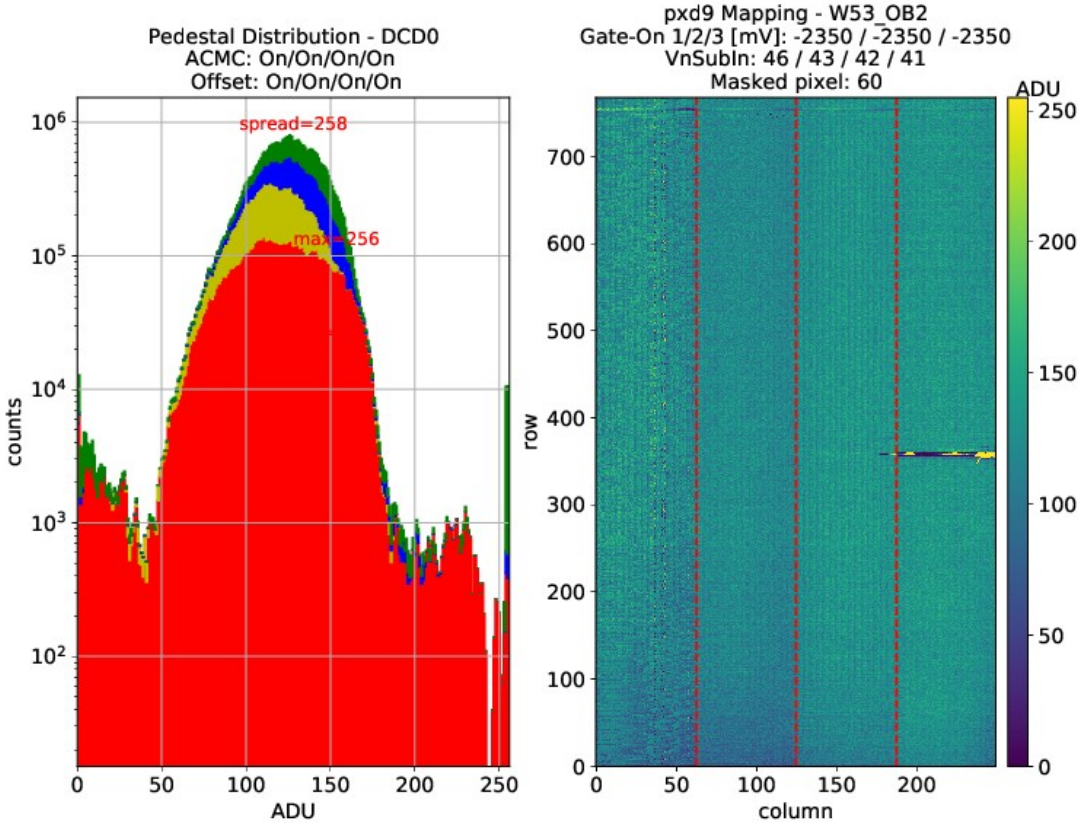
Offsets 2

https://elog.belle2.org/elog/PXD-Commissioning-KEK/20683

adjust vnsubout with ACMC =60,50,50,50 -> commitid 4234

Pedestals with ACMC

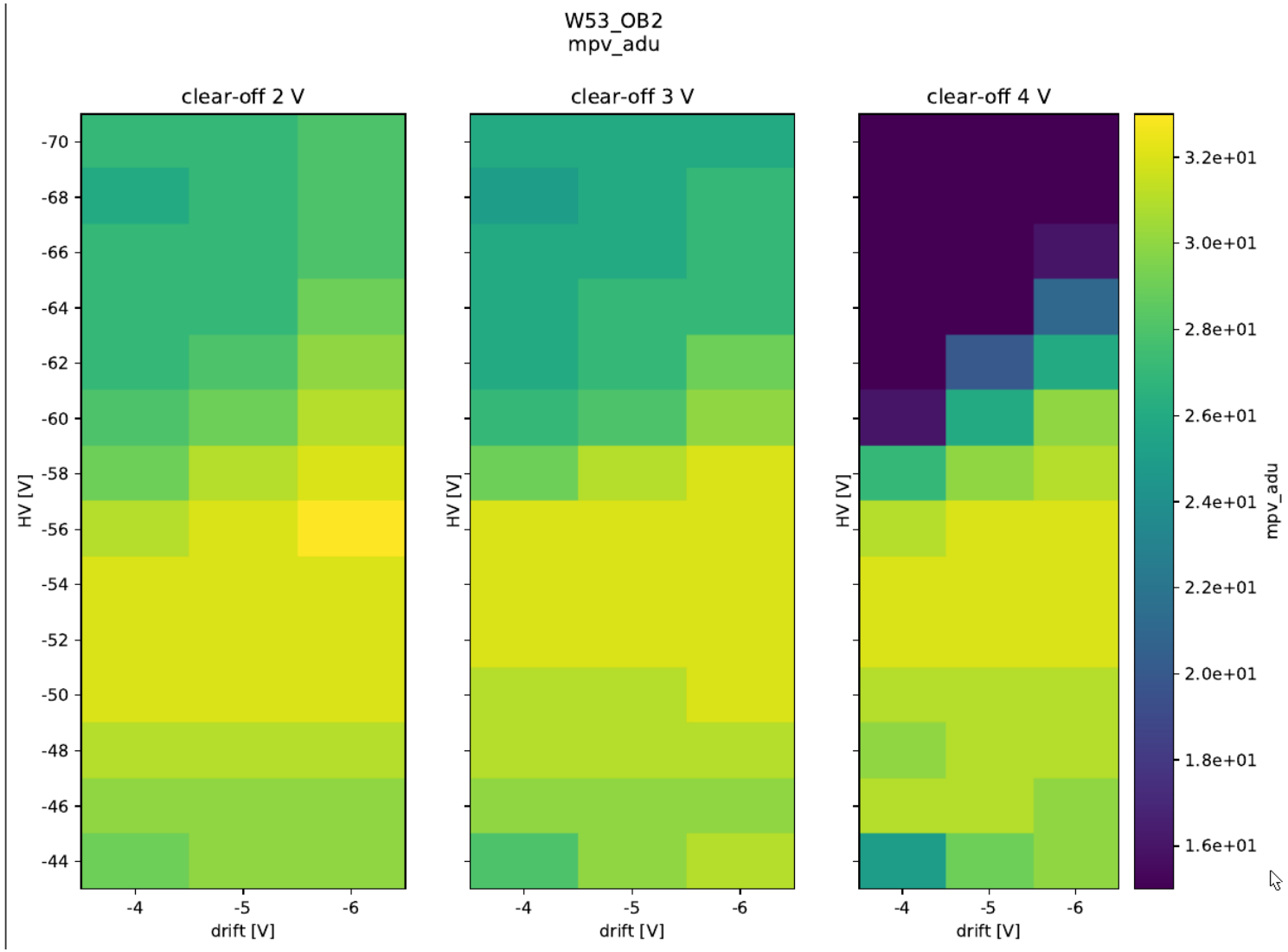
https://elog.belle2.org/elog/PXD-Mass-Testing/22525



- dcd 2,3,4 have ipdac ~11
- dcd 1 has ipdac = 21
- dcd 1 also has suspicious offset lines... coincidence?

Source scan

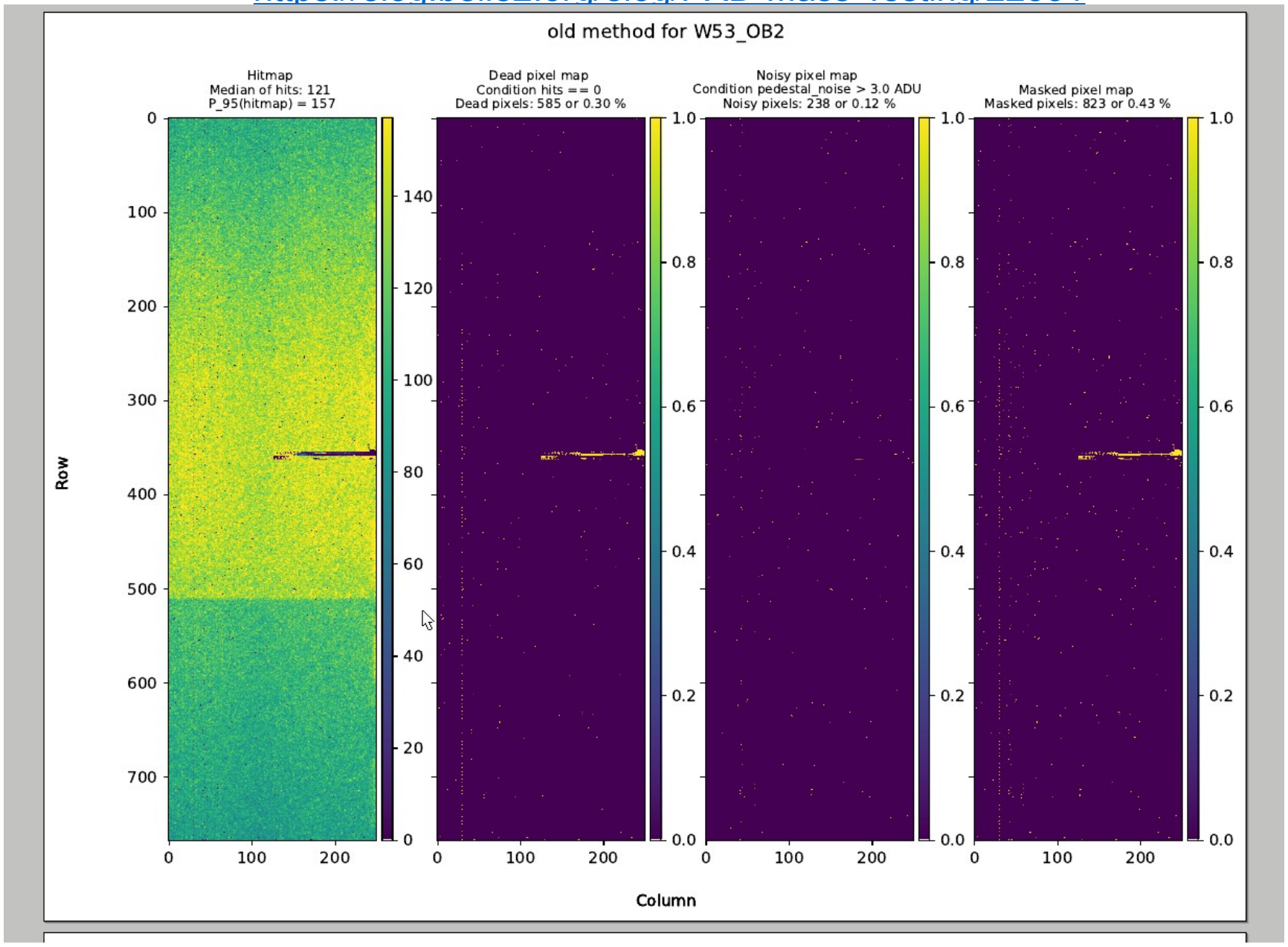
https://elog.belle2.org/elog/PXD-Mass-Testing/22529



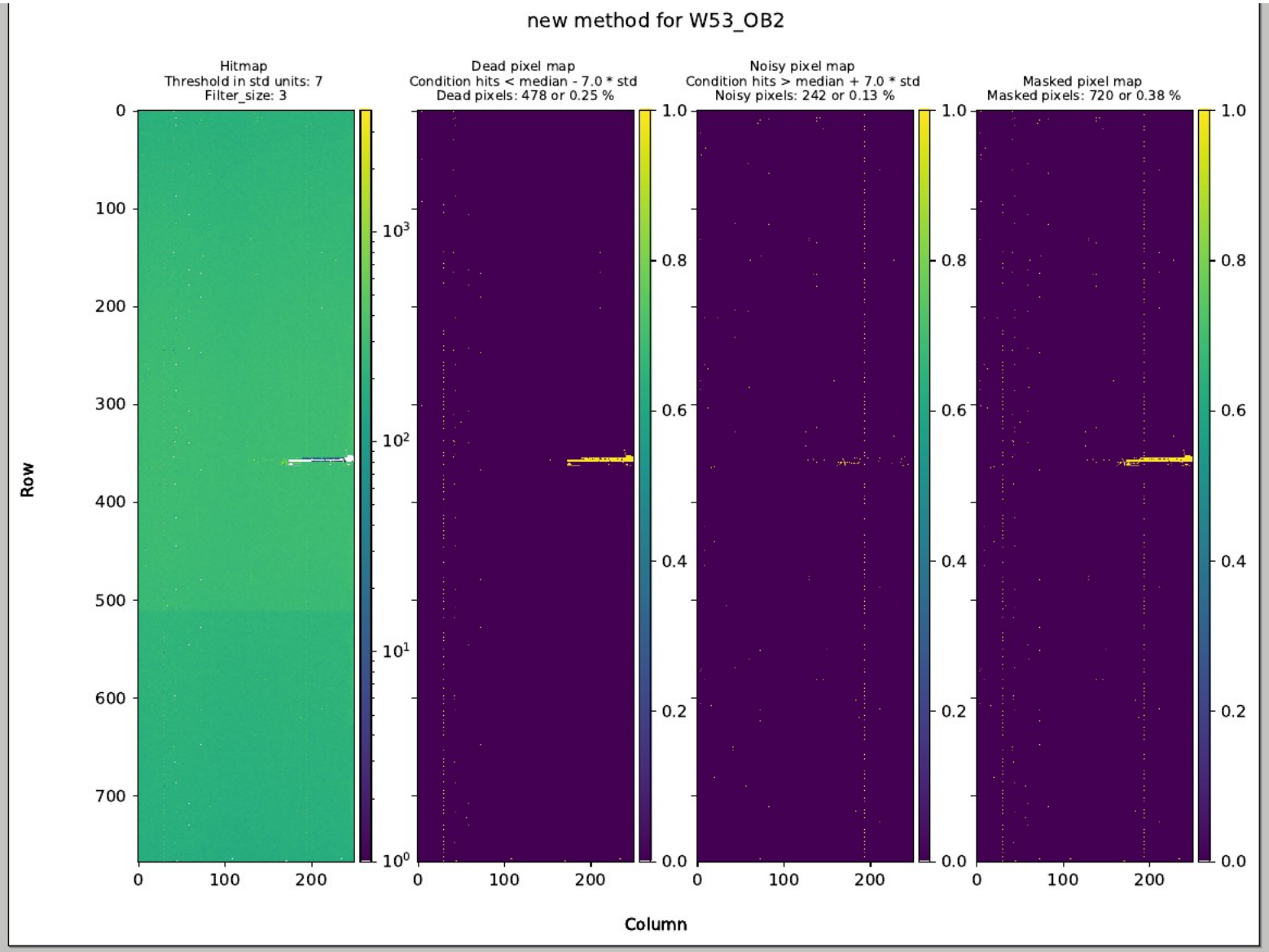
- optimum
  - HV -56 V
  - drift -6 V
  - clear-off 2 V

Source scan best setting

https://elog.belle2.org/elog/PXD-Mass-Testing/22531



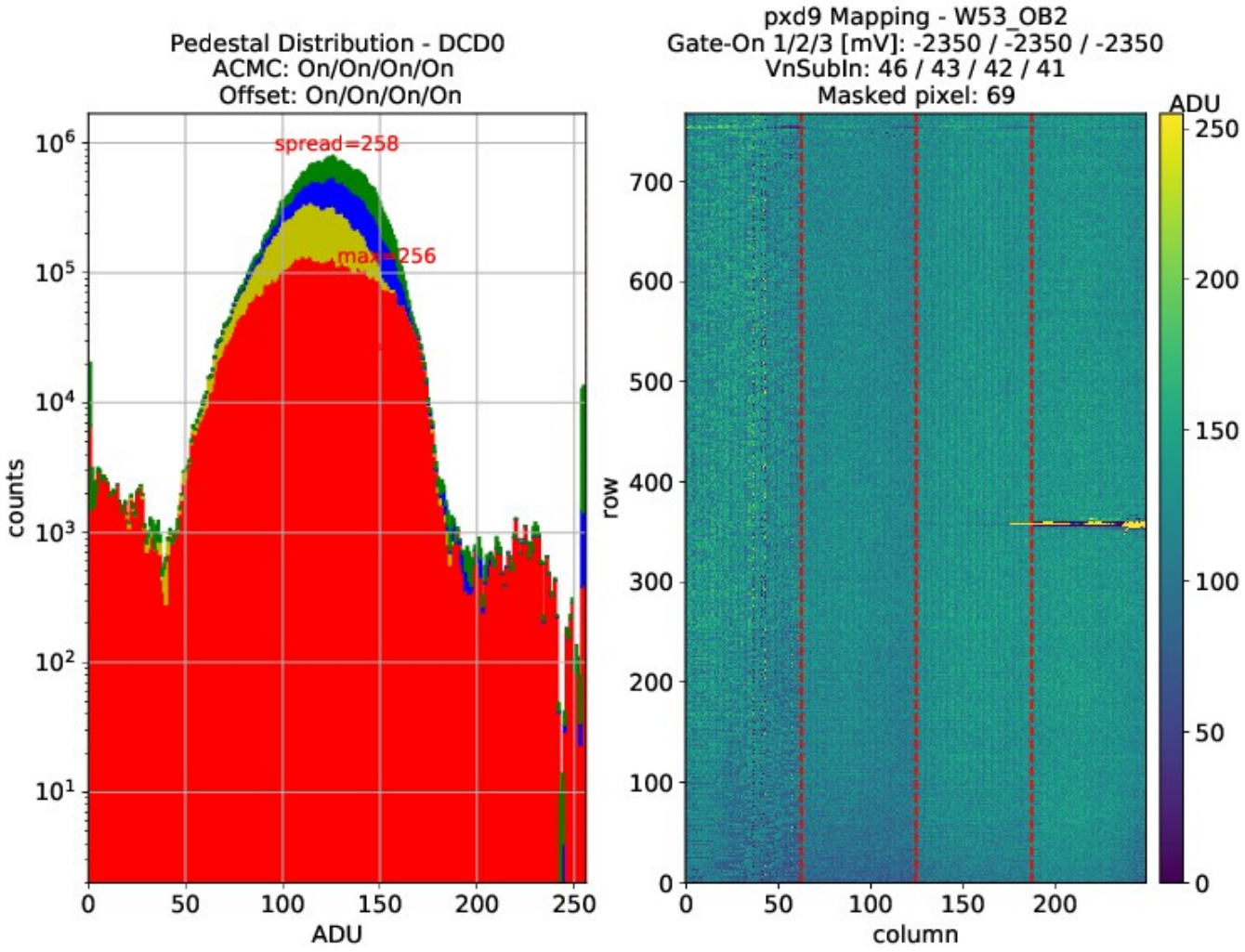
Source scan best setting



- < 0.5 % dead pixels
  -> grade A

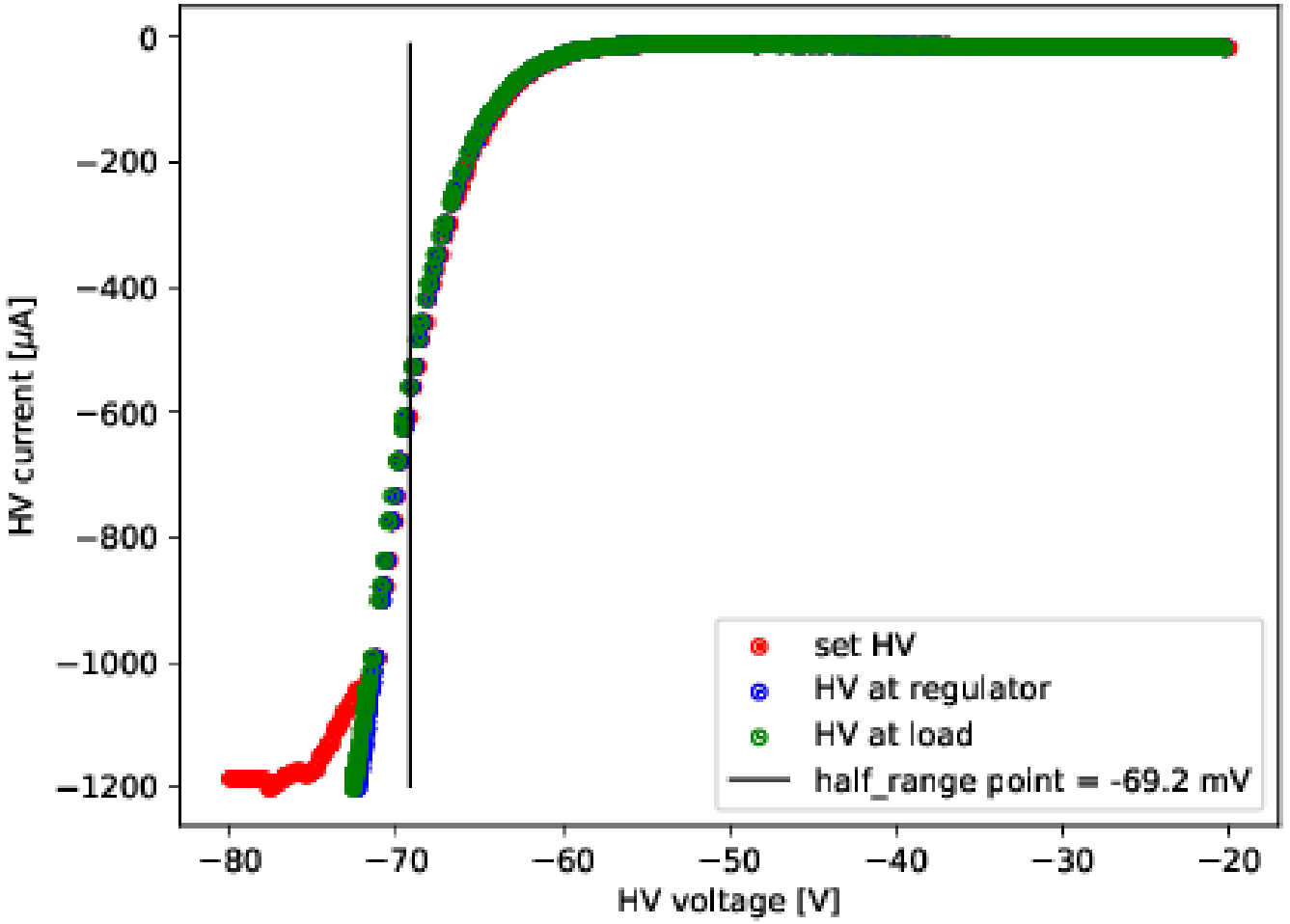
pedestals commit 4235

https://elog.belle2.org/elog/PXD-Mass-Testing/22533



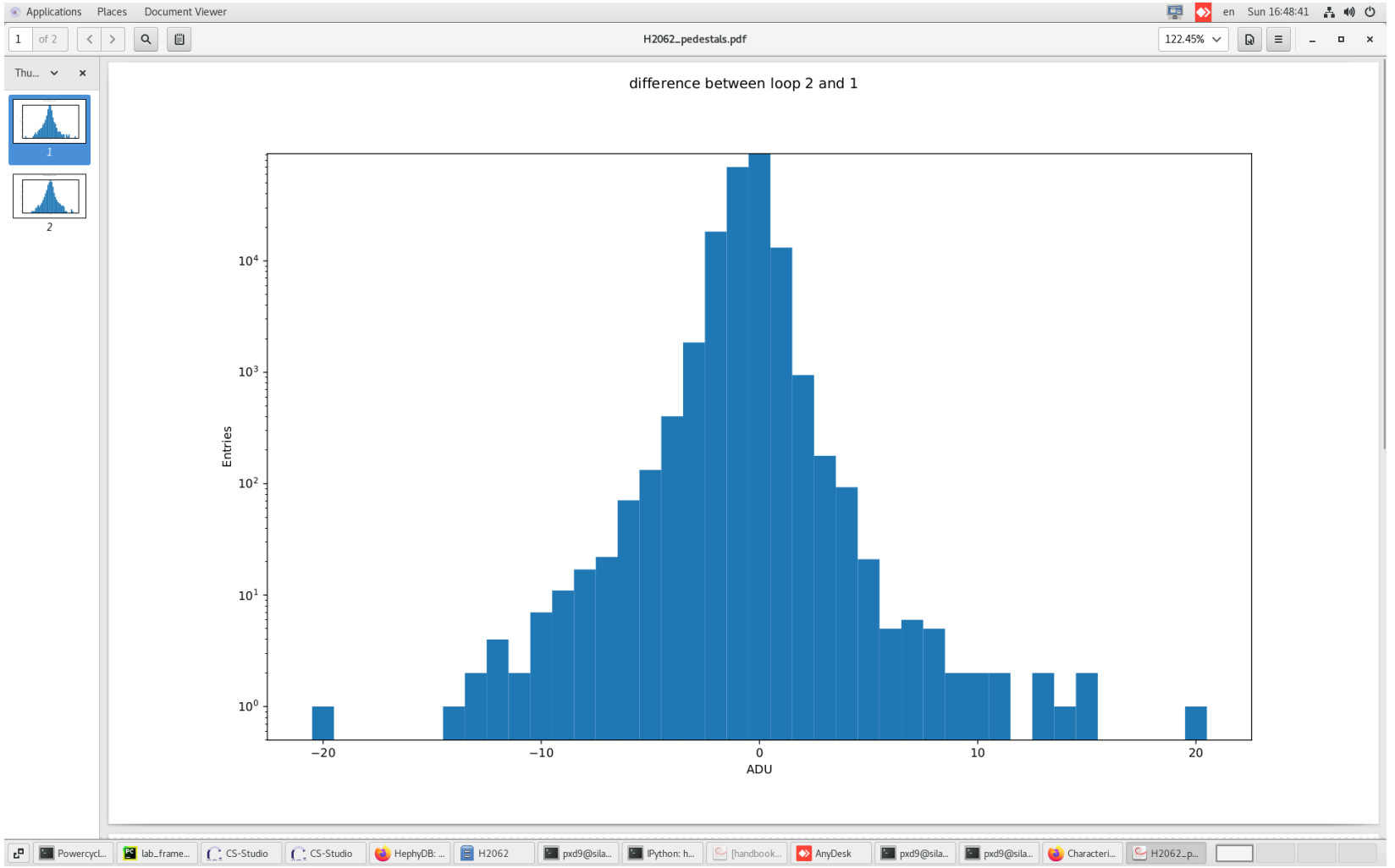
HV IV scan 2

https://elog.belle2.org/elog/PXD-Mass-Testing/22535



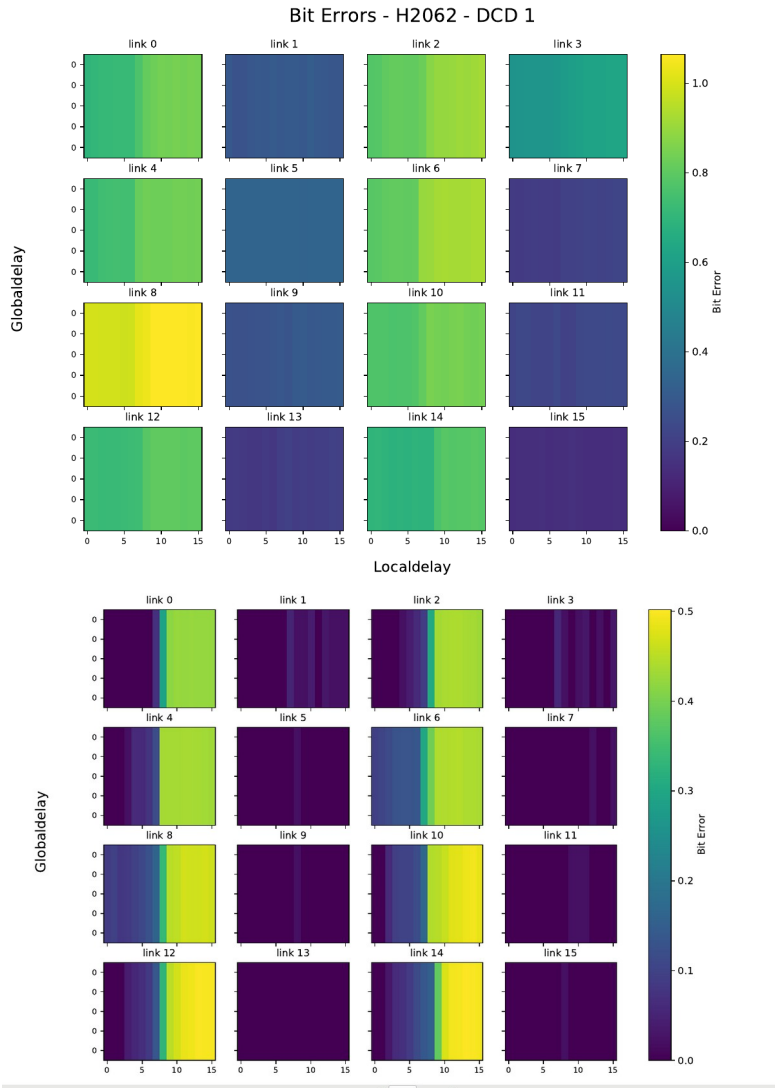
power cycle scan 2

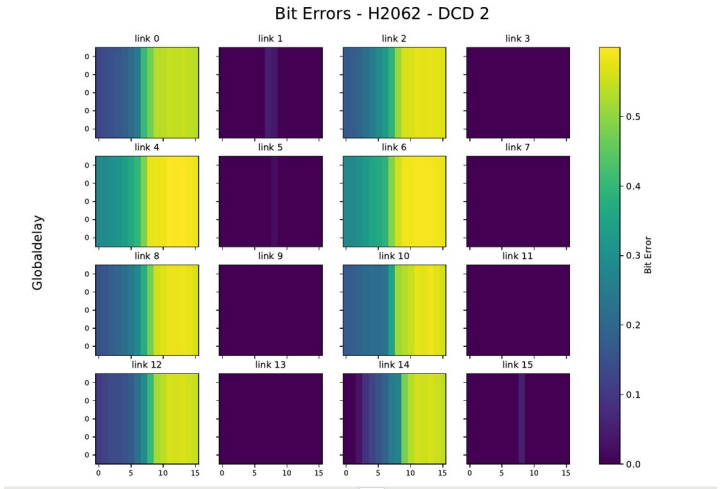
https://elog.belle2.org/elog/PXD-Mass-Testing/22539

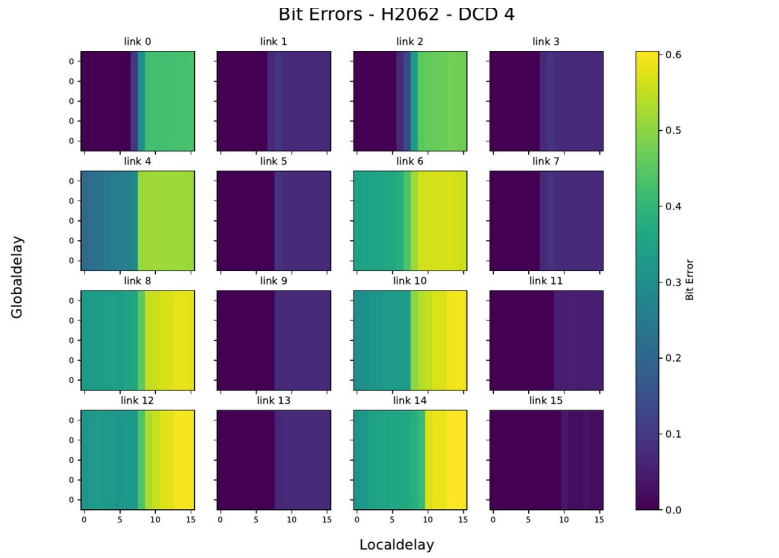


offset delays

stripes1 pattern https://elog.belle2.org/elog/PXD-Mass-Testing/22541



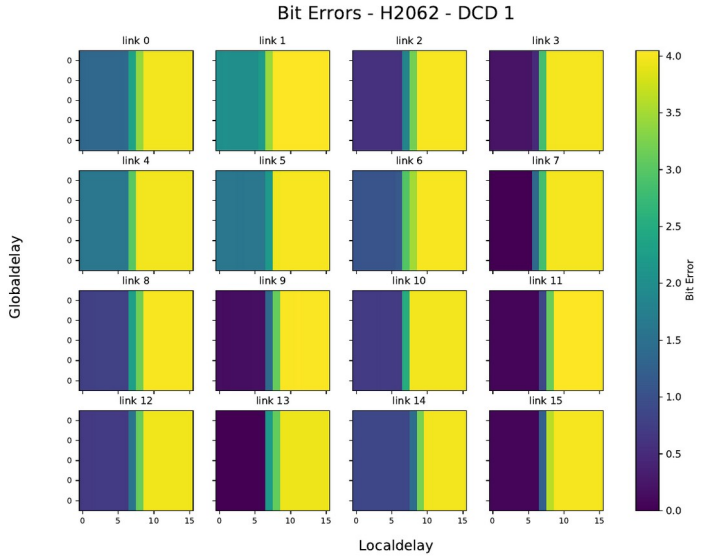


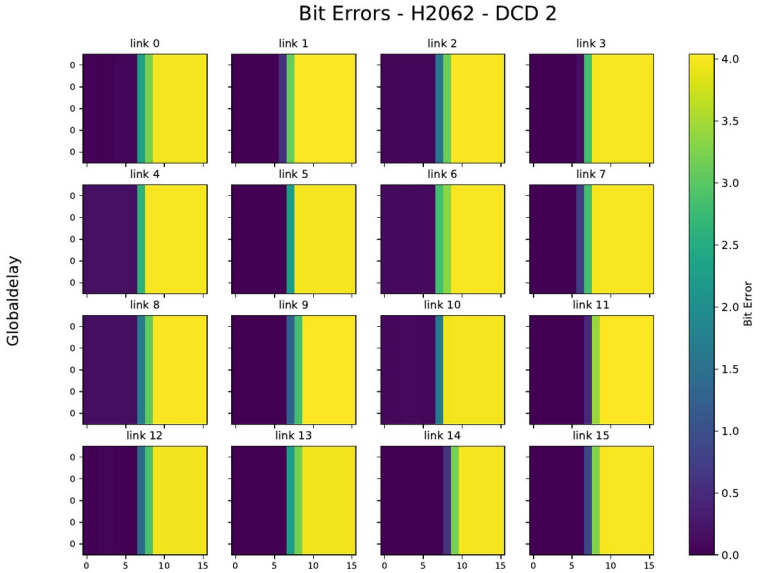


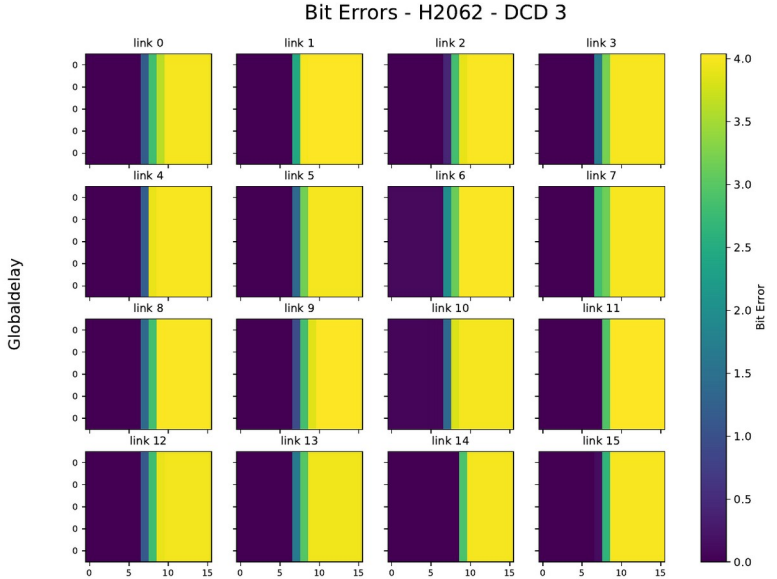
- dcd 1 link 8 looks irregular

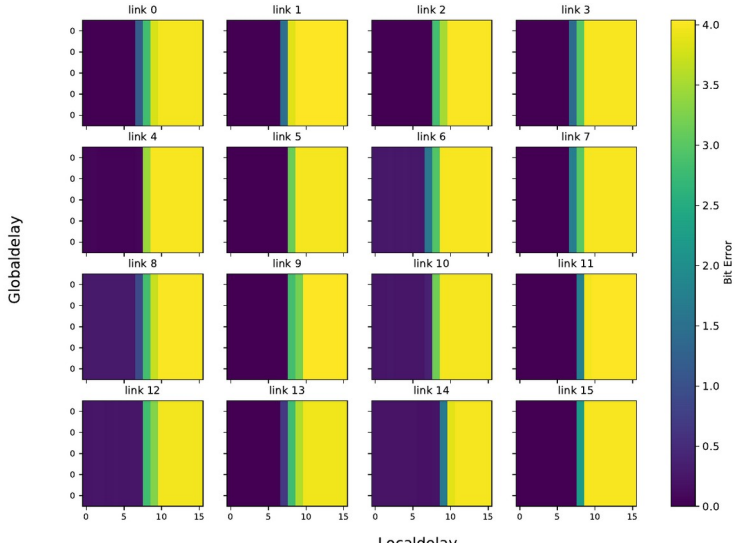
Offset delays

random pattern https://elog.belle2.org/elog/PXD-Mass-Testing/22543









- no strong irregularity in dcd1 link 8?

offset delays

stripes3 pattern: https://elog.belle2.org/elog/PXD-Mass-Testing/22545