MAX PLANCK SEMICONDUCTOR LABORATORY

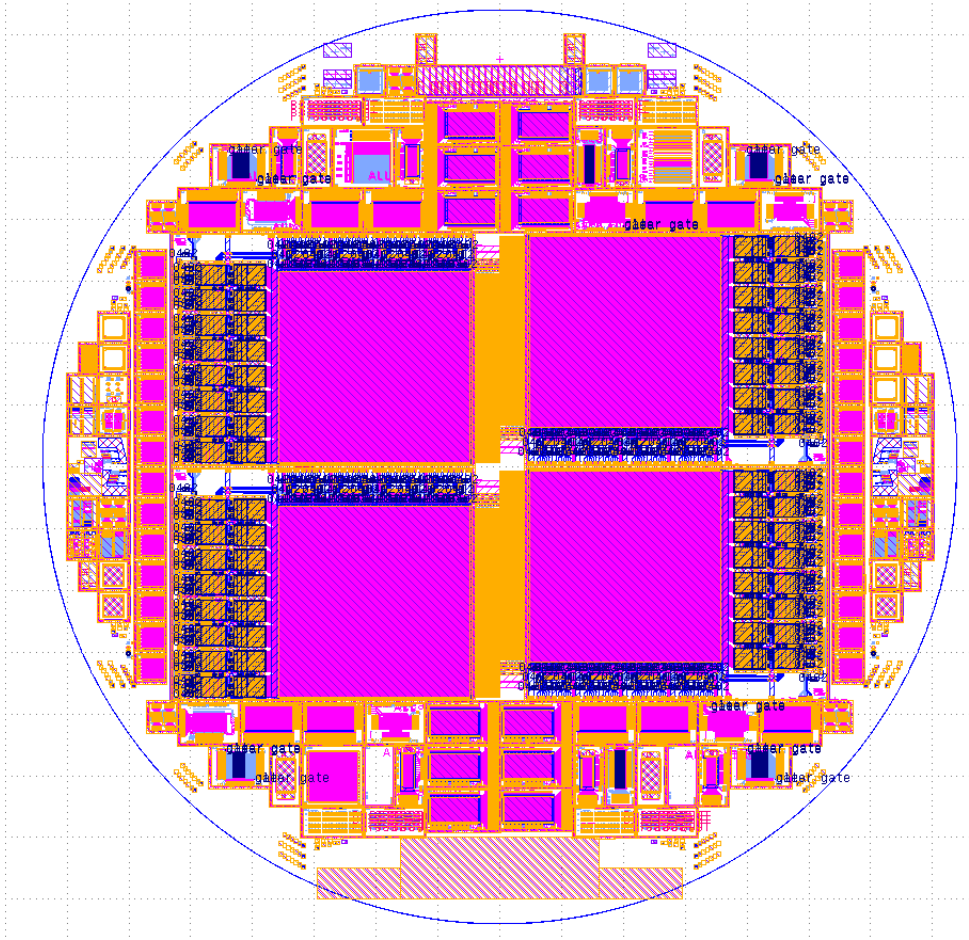
PXD10
WAFER PRODUCTION SUMMARY

Semiconductor Laboratory of the Max Planck Society

Christian Koffmane

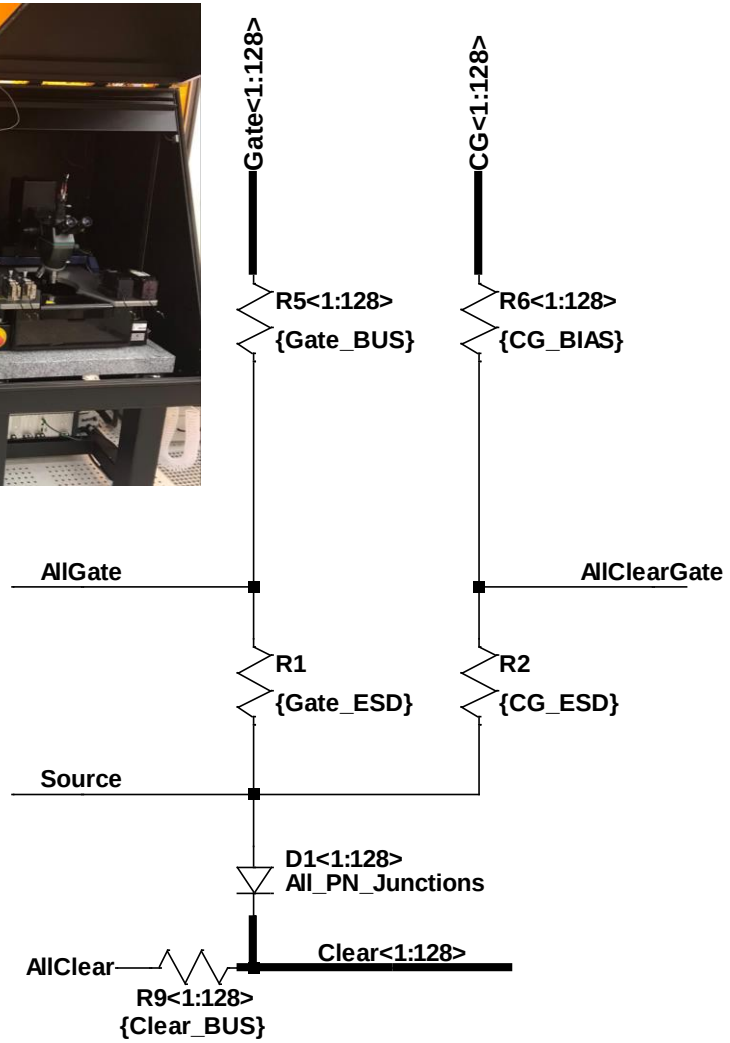
PXD10 PRODUCTION OVERVIEW

- **PXD10-1: Pilot run**
  - 4 wafers (SOI 50 µm, 30 µm, 2 standard wafers)
- **PXD10-2: Test project radiation hardness**
  - 4 wafers (2 SOI, 2 standard wafers)
- **PXD10-3: Production batch**
  - 8 wafers (3 x 30 µm, 5 x 50µm)
  - **wafer level test after al2n**
  - actn mask was applied
    - al2n repair and removing the
  - next is the co3n layer (BCB)



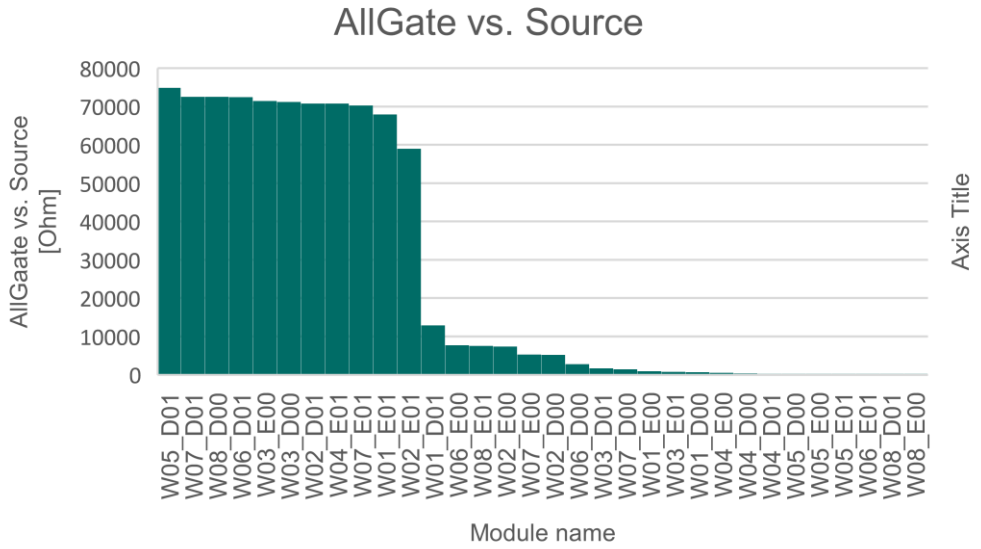
PXD10-3 WAFER LEVEL TEST AFTER ALU2

- **Global Test (2-needle measurements):**
  - **AllClear vs. Source**: integrity of all pn-junctions, Clear voltage sweep [0V:15V], current compliance 10 µA
  - **AllClearGate vs. Source**: integrity of the poly gates (ClearGate and Gate), does not show Gate to Clear shorts but Gate to ClearGate shorts; AllClearGate voltage sweep [-10V:+10V], current compliance 1 mA
  - **AllGate vs. Source**: AllGate voltage sweep [-10V:+10V], current compliance 1mA
  - **AllGate vs. AllClearGate**: AllClearGate voltage sweep [-10V:+10V], current compliance 1 mA
- **Probe Card + 1 automated needle measurements (IV curves)**



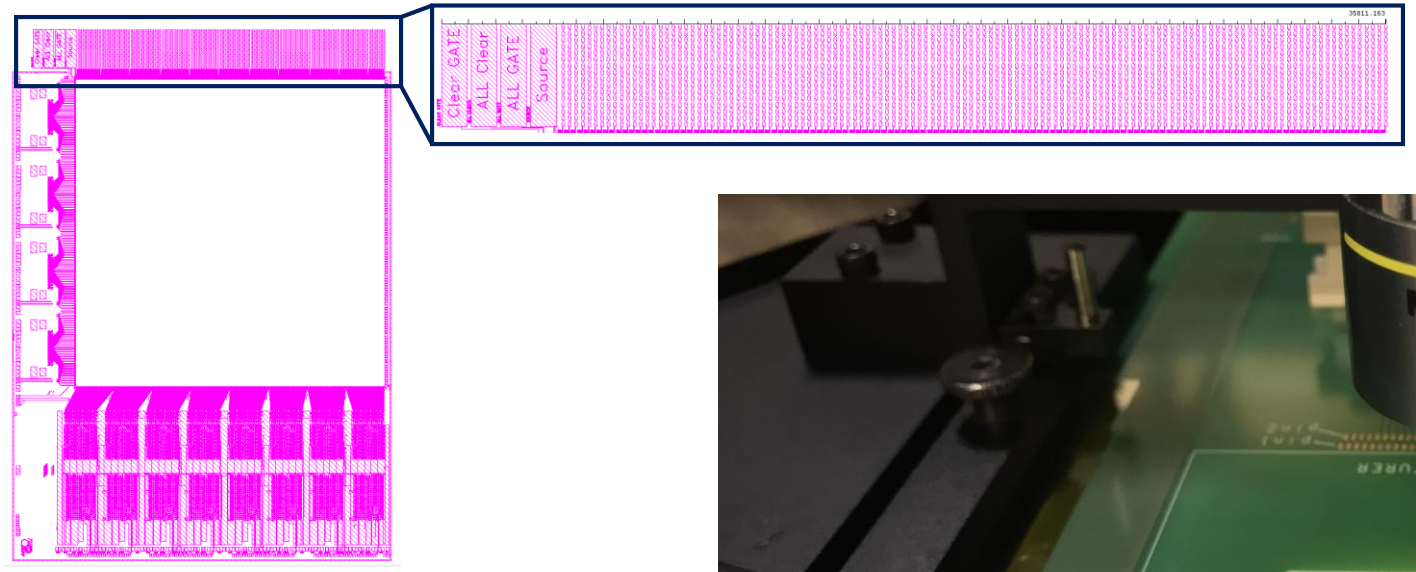
PXD10-3 ALLGATE VS. SOURCE PROBLEM

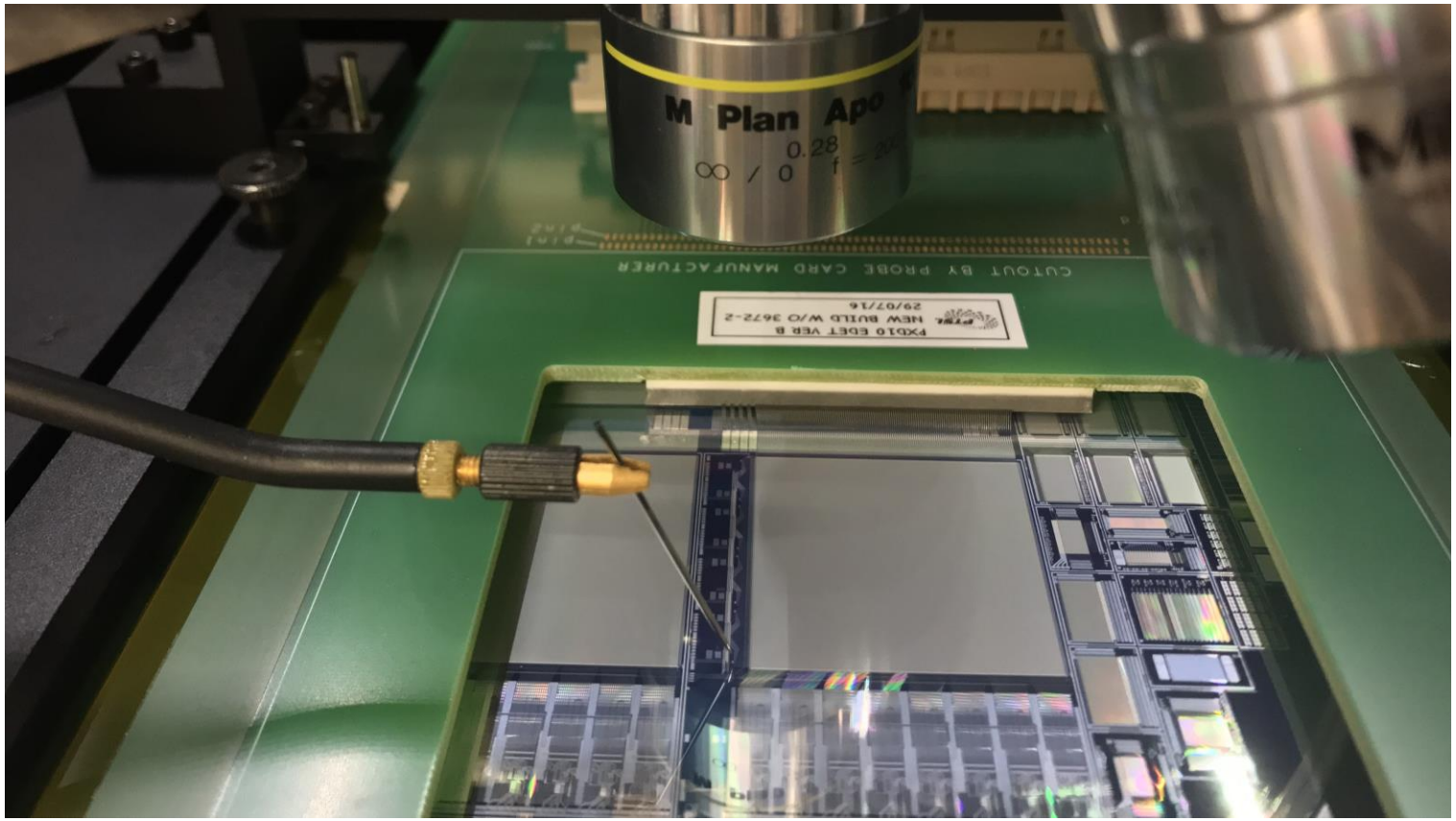
- The first Allgate vs. Source measurement showed 21 faults
- Repeating the measurement w/ biasing Bulk at 10V confirmed that there is no Gate to Source short, but that there are Gate to Drain shorts
  - If there is a Gate to Drain short and the Bulk/Clear not biased, the current flows through the DEPFET from Gate to Source.
  - Appling 10V at the Bulk closes the DEPFETs and reduces the AllGate to Source current significantly
- Drain to Gate are neighboring al2n structures
- Repaired by repeating the al2n mask



PXD10-3 WAFER LEVEL TESTING

Zoom of the DUT pad array





- Using 12 SMUs (Keithly SCS-4200A + 2612B) for bias voltages and Drain current measurements
- Keithley 7002 Switch System to connect the 128 Drain lines to seven SMUs

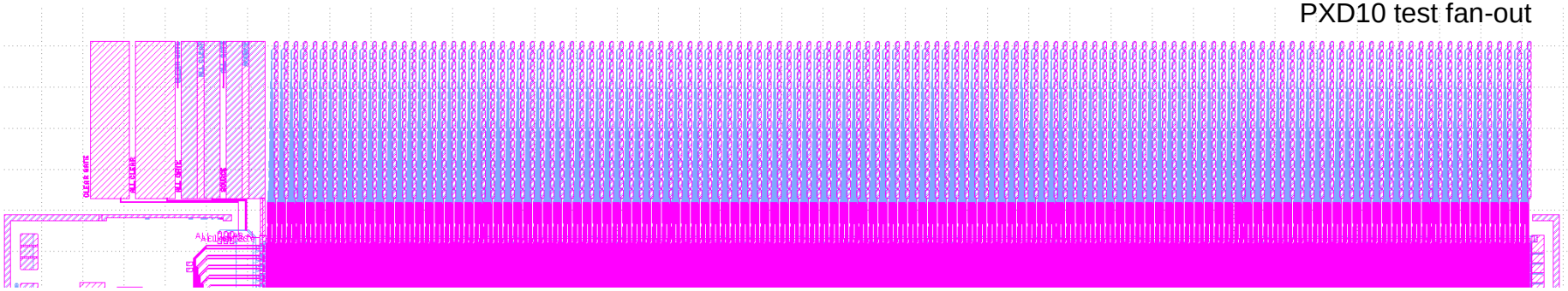
EDET PROBE CARDS

PXD9 test fan-out

Two probe card versions available:

- version A) connects 126 drain lines at one touch down
  - this probe card was used for PXD10-1 and PXD10-2
  - the number 126 comes from the Belle II PXD9 probe card setup (1000 drain lines, 1008 test pads)
  - no changes in the control of the KEITHLEY multiplexer and SMUs necessary
  - but: execute complete probe card test twice in order to test all EDET drain lines (2048)
- version B) connects 128 drain lines at one touch down
  - this probe card was used for PXD10-3, 16 touch downs to contact all drain lines

PXD10 test fan-out

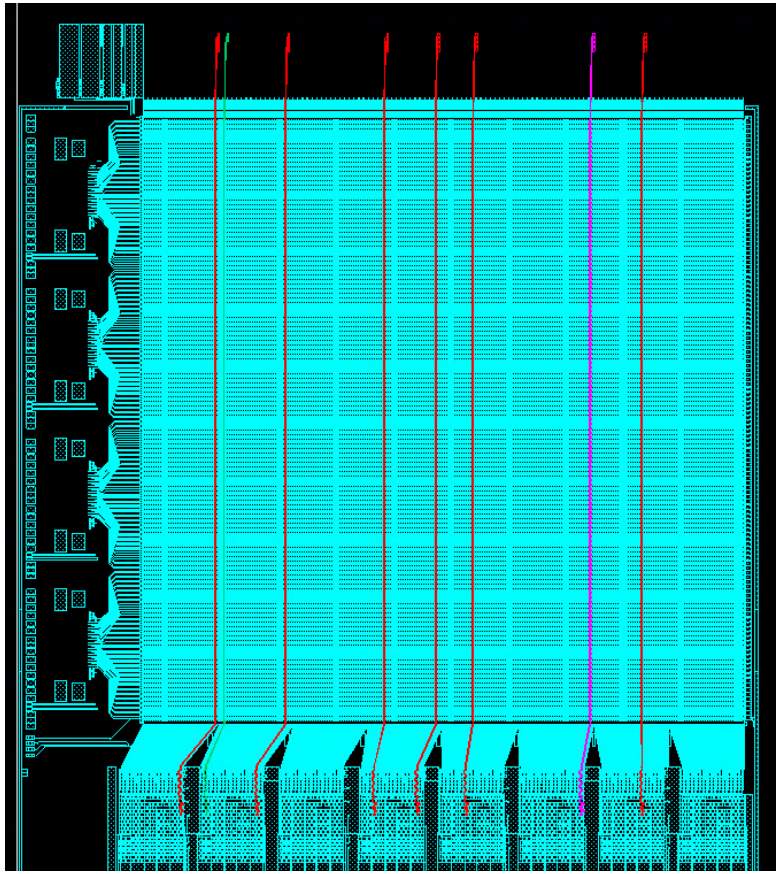


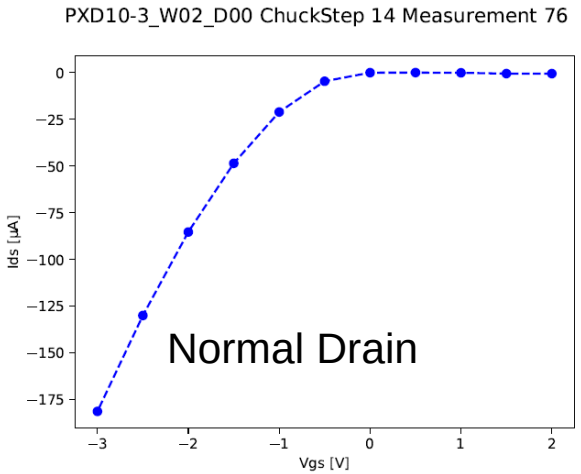
EDET PROBE CARDS

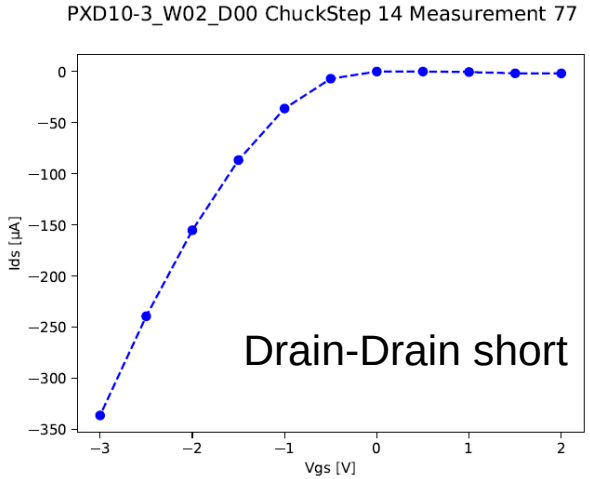
Changes applied to operate probe card 2:

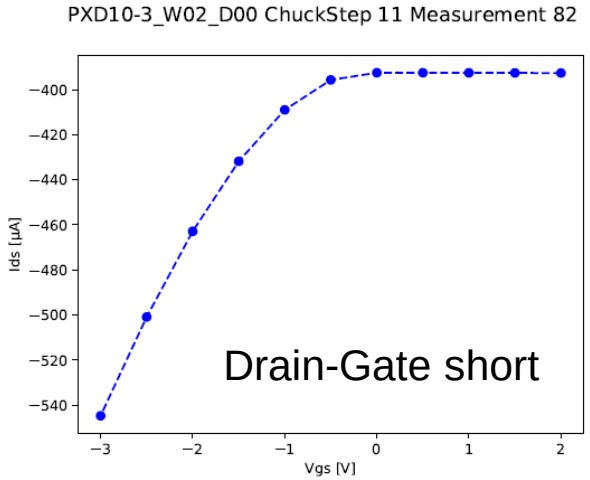
- Connect the additional signal lines to the KEITHELY 7002 Switching system
- Add additional measurement in the KETHLEY 4200A-SCS measreuement
- Change the data analysis (from MATLAB to Python)

PXD10-3 W02 D00







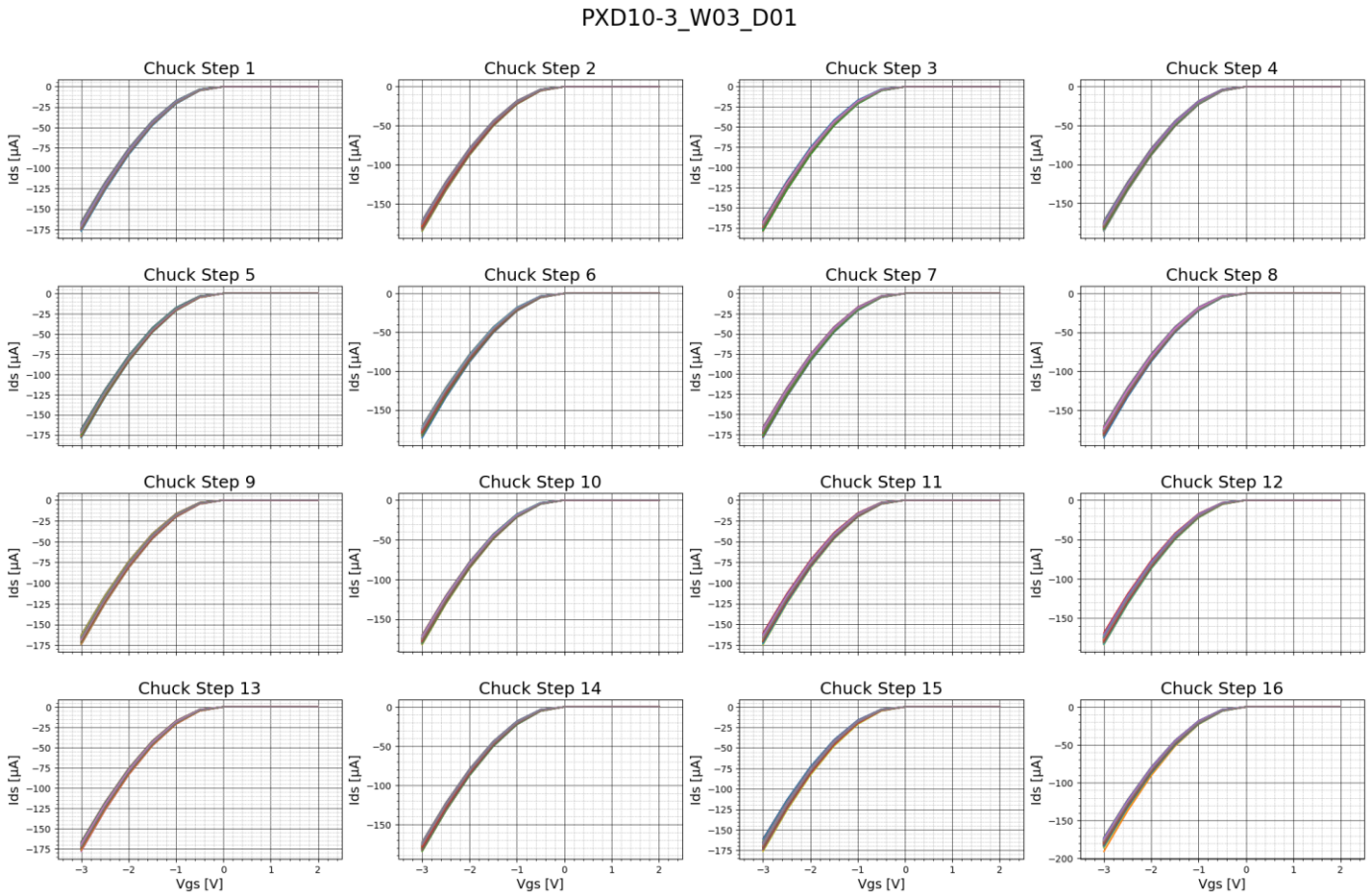


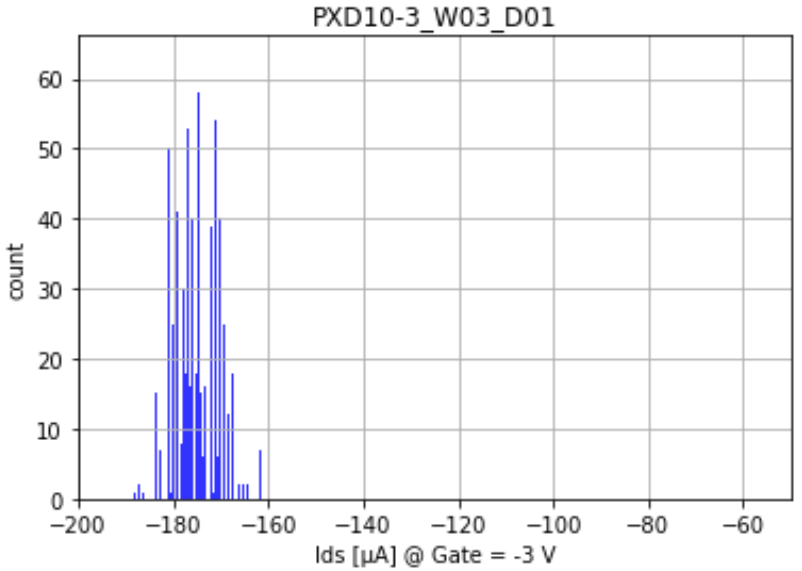
mark_HighCurrentDrains_PXD10-3_W02_D00.il

```
leMarkNet('(21580.0 51795.0) ?markNetColor "Y1")
leMarkNet('(32140.0 51795.0) ?markNetColor "Y1")
leMarkNet('(23500.0 51795.0) ?markNetColor "Y1")
leMarkNet('(29500.0 51795.0) ?markNetColor "Y1")
leMarkNet('(13900.0 51795.0) ?markNetColor "Y1")
leMarkNet('(18940.0 51795.0) ?markNetColor "Y1")
leMarkNet('(10300.0 51795.0) ?markNetColor "Y1")
leMarkNet('(21580.0 52035.0) ?markNetColor "Y1")
leMarkNet('(32140.0 52035.0) ?markNetColor "Y1")
```

Generated Skill script to highlight Drain lines in Cadence Virtuoso

DRAIN CURRENT DISTRIBUTION





- **Ids max = -191 µA**
- **Ids min = -163 µA**
- **DCD gain 3.3 → range ~140 µA**
- **DCD gain 11 → range ~41 µA**

SUMMARY PXD10-3 WAFER LEVEL TESTING

- 1 module fails due to low ohmic Clear to Source short
- 2 modules have interrupted Drain lines (one mainly outside the matrix region)
- 5 modules have an increased Clear current (up to 30 µA at 10V)
- 5 modules need a repair (removing or cutting the Drain line: 4 x only one Drain line will be removed – 0.05% of the pixels, 1 x six Drain lines will be removed)
- 19 modules passed all tests without any problems (11 x 50 µm SOI, 8 x 30 µm SOI).

Wafer	DUT	Global Test	IV Test	Comment	Repair
1	D00	PASS	FAIL	49 OPEN mainly between matrix and test pads	none
	D01	PASS	PASS	PASS	
	E00	PASS	FAIL	136 OPEN	none
	E01	FAIL	PASS	17 µA Clear current at 10 V, Ids at positive Gate voltage	none
2	D00	FAIL	FAIL	AllGate-Source test shows too low resistance, four Drain to Gate SHORTs, one Drain to Drain SHORT	remove four complete Drain lines, cut two Drain lines before DCD input
	D01	PASS	FAIL	one Drain to Source SHORT	cut Drain line before DCD input
	E00	FAIL	PASS	Clear-Source test break down at 7 V, Clear current < 1 µA in IV test at 10 V	none
	E01	PASS	FAIL	Drain to ClearGate SHORT	remove one Drain line completely
3	D00	PASS	PASS		
	D01	PASS	PASS		
	E00	PASS	PASS		
	E01	PASS	FAIL	seven Drain to Source SHORTs	cut Drain lines before DCD input
4	D00	PASS	PASS		
	D01	FAIL	FAIL	SHORT (Clear/Source)	none
	E00	PASS	PASS		
	E01	PASS	PASS		
5	D00	PASS	PASS		
	D01	PASS	PASS		
	E00	PASS	PASS		
	E01	PASS	PASS		
6	D00	PASS	PASS		
	D01	FAIL	PASS	1.3 µA Clear current at 10 V	none
	E00	PASS	PASS		
	E01	PASS	PASS		
7	D00	PASS	PASS		
	D01	FAIL	PASS	1.9 µA Clear current at 10 V	none
	E00	PASS	PASS		
	E01	PASS	FAIL	one Drain to Source SHORT	cut Drain lines before DCD input
8	D00	PASS	PASS		
	D01	FAIL	PASS	30 µA Clear current at 10 V	none
	E00	PASS	PASS		
	E01	PASS	PASS		

HERZLICHEN DANK FÜR IHRE AUFMERKSAMKEIT

Bei Fragen wenden Sie sich gerne an:

Halbleiterlabor der Max-Planck-Gesellschaft

Christian Koffmane

Otto-Hahn-Ring 6

81739 München

Tel.: +49 (0)89 839400-59

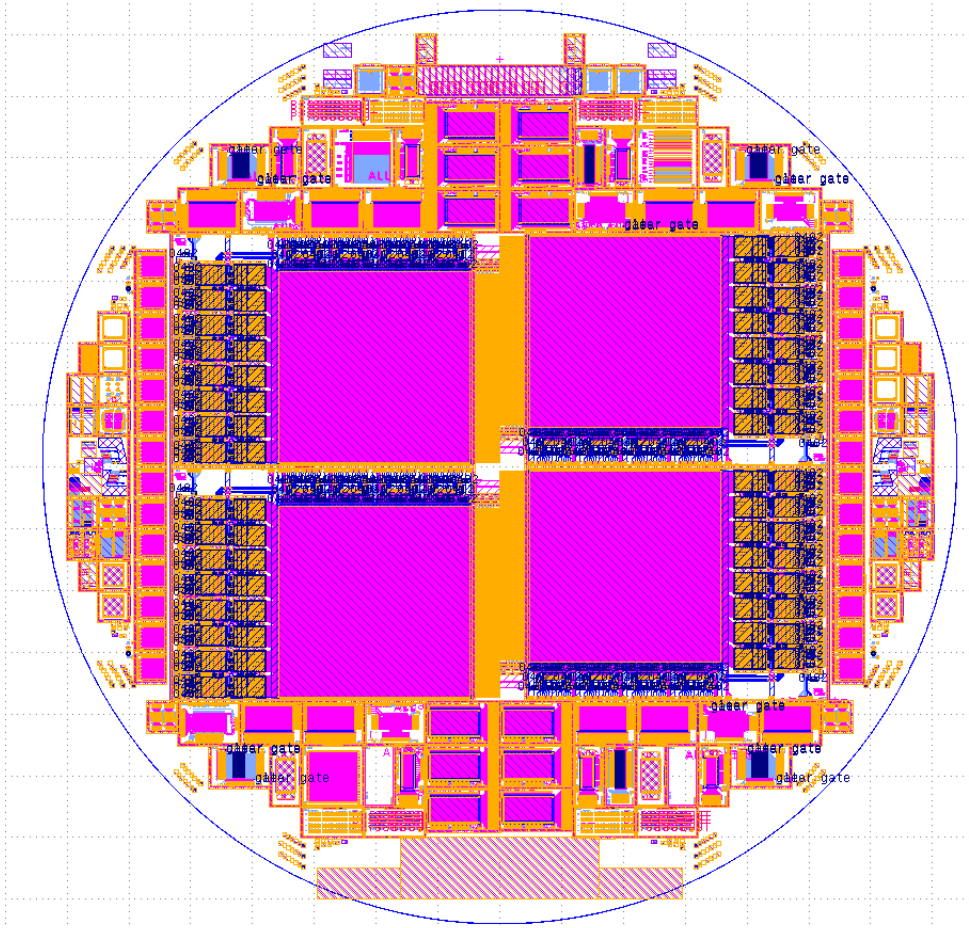
Fax: +49 (0)89 839400-11

E-Mail: hll-info@hll.mpg.de

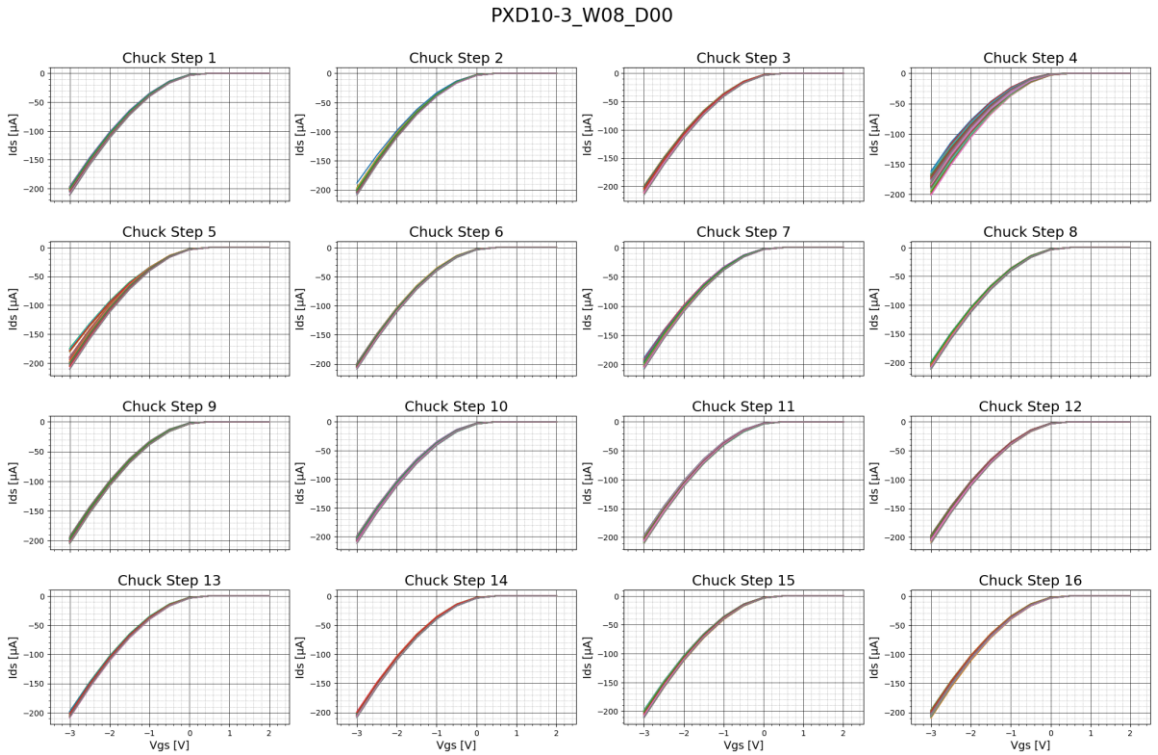
Internet: www.hll.mpg.de

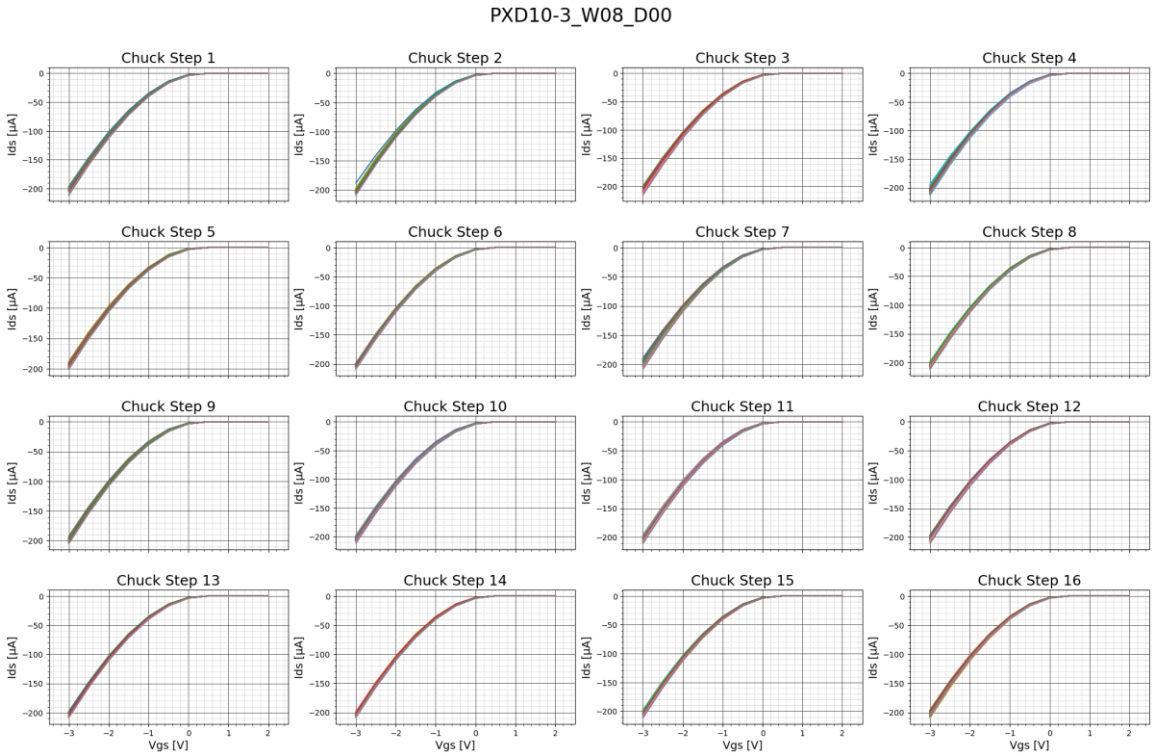
PXD10-1

- Processing started in 2015, ATG flying prober measurements in 2017
  - pol1n and pol2n plasma etched
- 4 wafers (SOI 50 µm, 30 µm, 2 standard wafer)
- 3 EMCM wafer (SOI ~30 µm)
- Wafer contain a variety of small matrices (32 x 256 pixels) and four large sensors (512 x 512 pixels)
- The large sensors integrate the routing for the control and read-out ASICs (DMC or DHP, DCD and Switcher)
- first assembled EMCM tested in June 2020



DRAIN CURRENT DISTRIBUTION





- **Chuck steps 4 and 5 repeated**

PXD10-3 W01 D00

- 49 open drain lines
- 14 due to disconnected test pads
- No shorts