

Signal resolution and dynamic range

# A SHORT REMINDER...



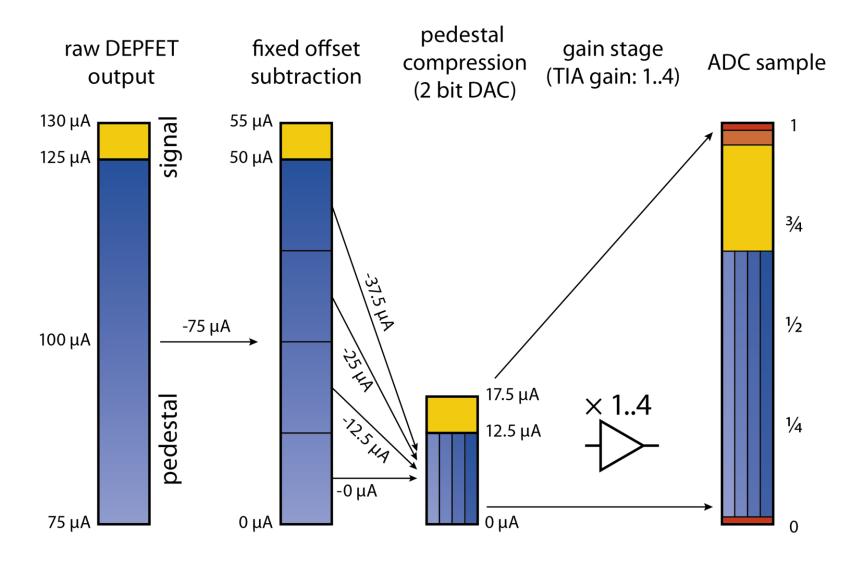
# Signal resolution and dynamic range

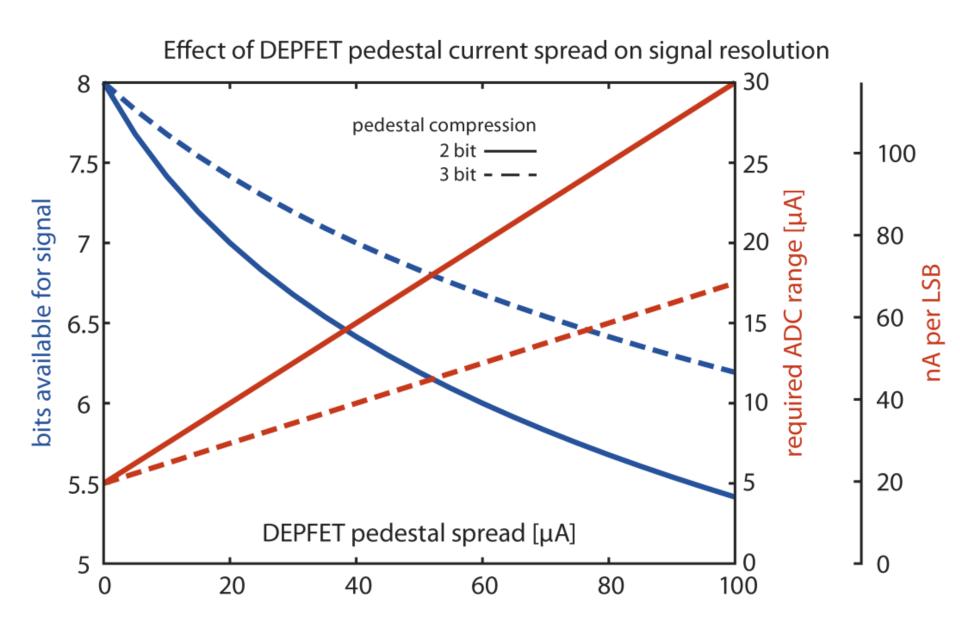
- What signal resolution can we expect just from the ASICs?
- Try realistic scenario and include (most) error sources
  - DEPFET pedestal spread
  - DCD nonlinearities
  - Electronic Noise
  - Numerical errors

#### We have

- Signal: ≈ max 10000 e<sup>-</sup> → gq ≈ 0.5nA/e<sup>-</sup> → 5μA maximum Signal
- Pedestals: @100μA average; large area, irradiation
  → 50μA variation (+/- 25μA)
- DCDb with 2bit DAC for "pedestal range compression"
- DCD2 ADC range up to 24μA (from my own measurements)
- ... multiple sources of errors...

# DCDb dynamic range concept





# To consider...

common mode noise needs to fit in too!

ganged pixels? → double range!

#### Common mode noise

- ... is mostly a system aspect
- can be avoided/reduced by careful design
- As an example:

DEPFET's 
$$g_m \approx 50 \mu S = \frac{\partial I_{out}}{\partial V_{in}}$$

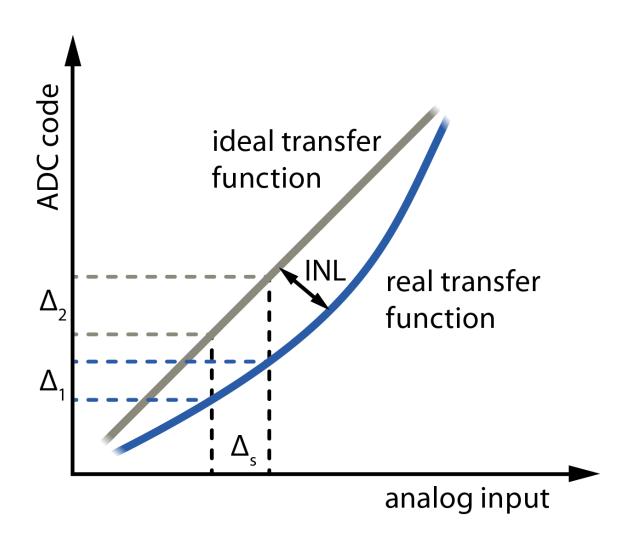
← from our previous scenario 1LSB ≈ 70nA

a change of 1.4mV on Gate-ON will cause 1LSB of 'common mode'

... and that's why we need low output impedance of the PDN ...

# **DCD** nonlinearities

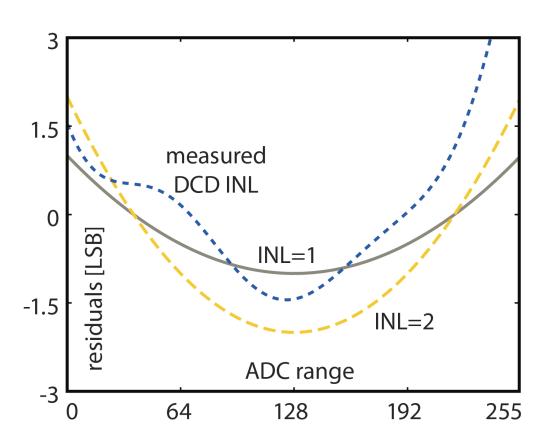
- Do we need to correct for these?
- Can we even correct after DHP calculations? Original values needed!



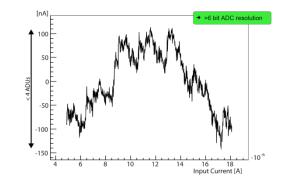
# Nonlinearities...

Typical picture:

 Measured INL smoothed! (DCD2)



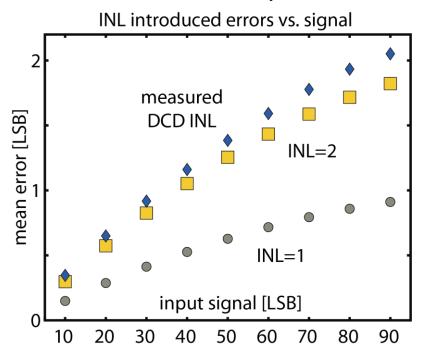
• The real picture (see Jochen's talk)

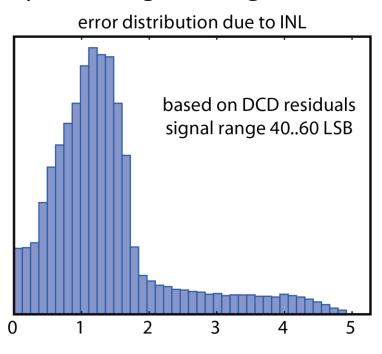


### Nonlinearities...

# ... and their effect

Introduced errors depend on INL shape and signal range





- Expect 1LSB of additional systematic error
- Correctable?
  Only if you calibrate and common mode is low

#### To summarize...

- We effectively digitize signals with 6bit resolution
- This leaves us 4.5 bits of real information!