



Data Handling Processor v0.1

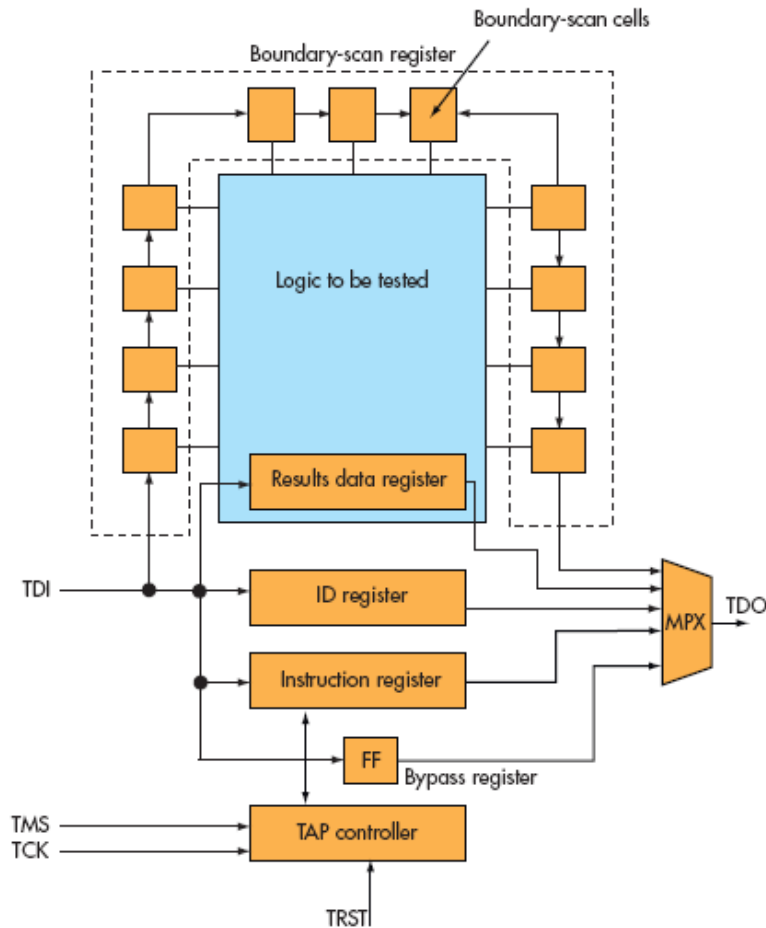
First Test Results

Tomasz Hemperek

DHP01 Overview

- ▶ **Technology**
 - ▶ IBM 90nm – 9 metal layer
 - ▶ 1.2 core / 1.8 IO voltage
- ▶ **Interface**
 - ▶ 32 (4x8) 400 MHz inputs from DCD (HSTL18)
 - ▶ LVDS control signals (clock, trigger, sync)
 - ▶ CMOS JTAG
 - ▶ Hi-speed CML output
- ▶ **Internal Blocks**
 - ▶ Common mode correction
 - ▶ Pedestal subtraction (static and dynamic*)
 - ▶ Zero suppression (threshold)
 - ▶ Channel framing and serialization
 - ▶ DCD offset correction
 - ▶ Raw data storage up to (2048 rows)
 - ▶ Sequencer for switcher
 - ▶ Configurable delays
 - ▶ Clock generation (PLL)
 - ▶ Configurable trigger latency (up to 1024 rows)
 - ▶ Slow control (JTAG)
 - ▶ ADC & DAC

Slow control - JTAG



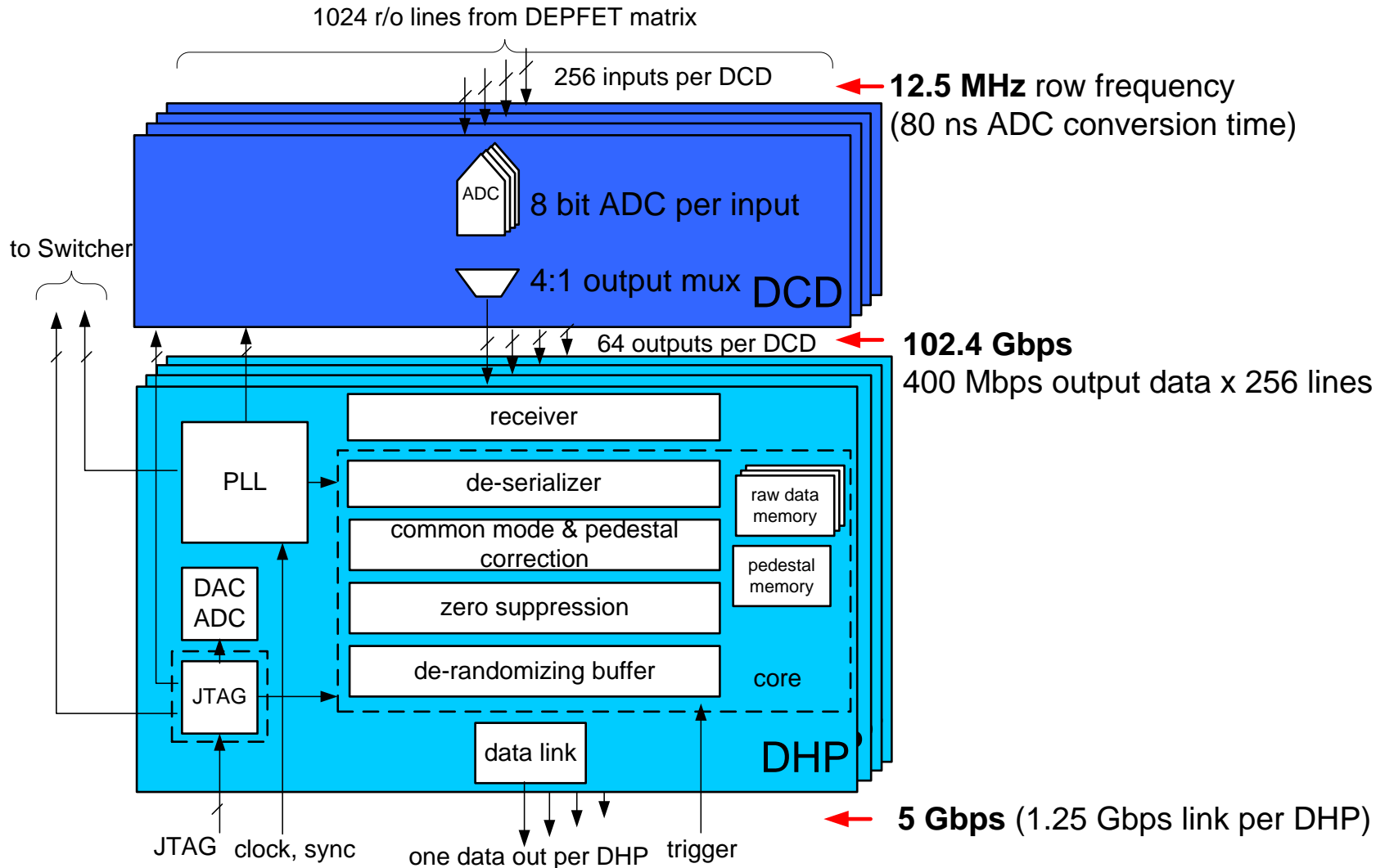
▶ Boundary scan

- ▶ EXTEST
- ▶ SAMPLE
- ▶ PRELOAD
- ▶ INTEST

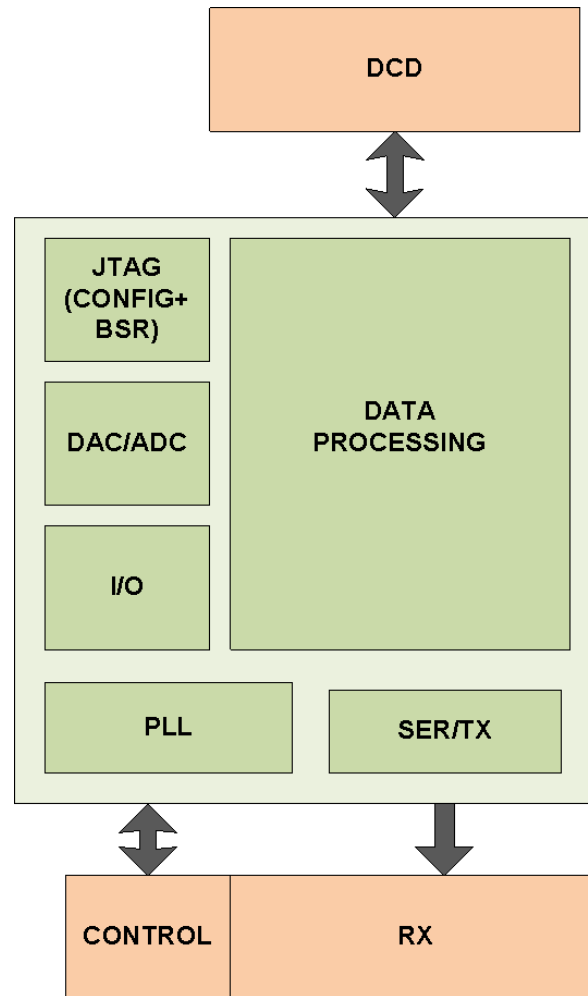
▶ Configuration

- ▶ BYPASS
- ▶ IDCODE
- ▶ USERCODE
- ▶ ADC
- ▶ BG
- ▶ CORE_READBACK
- ▶ CORE_REG
- ▶ DAC
- ▶ DACENC
- ▶ GLOBAL_REG
- ▶ MEM_ADDRESS
- ▶ MEM_DATA
- ▶ OFFSET_MEM_ADDR
- ▶ OFFSET_MEM_DATA

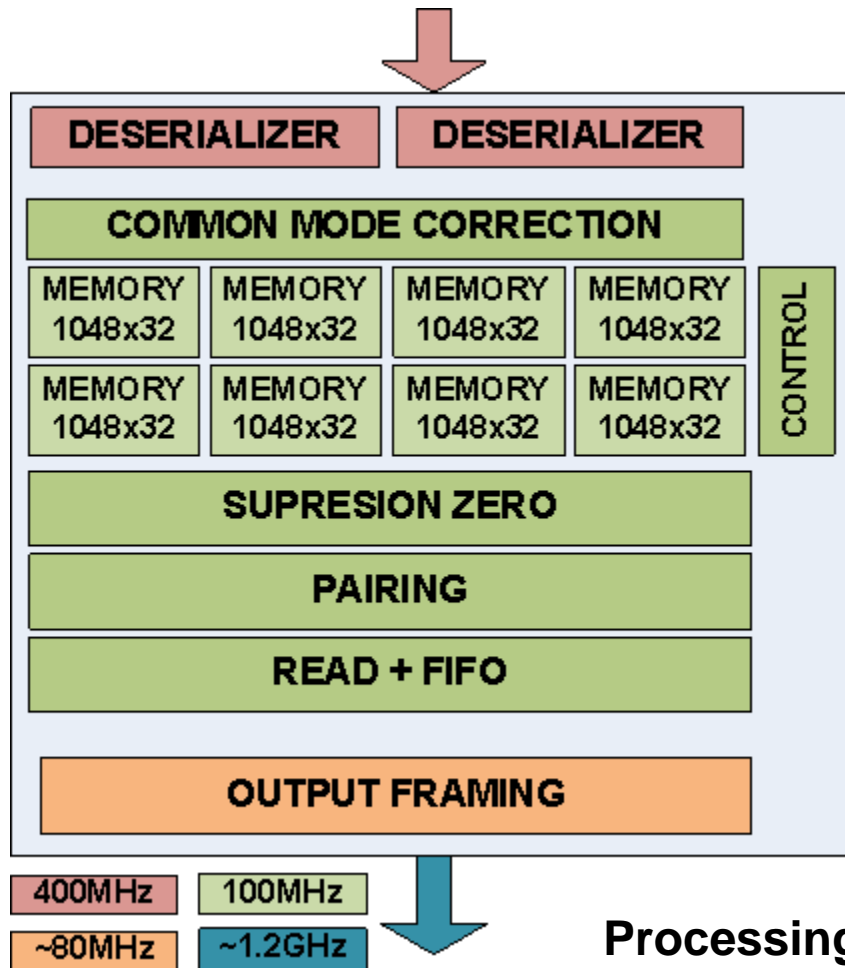
DHP – Signal Rates & Data Flow



DHP Overview



DHP Processing



- Deserializer (1 to 4)
- Common mode correction
- Buffering for latency
- Pedestal correction
- Hit Pairing
- Readout
- Output framing

Processing algorithms are very simple in current version and need to be adjusted

Operating modes

- ▶ **MEMORY ACCESS**

Allows to access memory block through JTAG interface for pedestal and offset correction.

- ▶ **RAW DATA RECORD**

Storing raw data to memory (support for trigger).

- ▶ **RAW DATA SEND**

Sending through fast output link all memory contents.

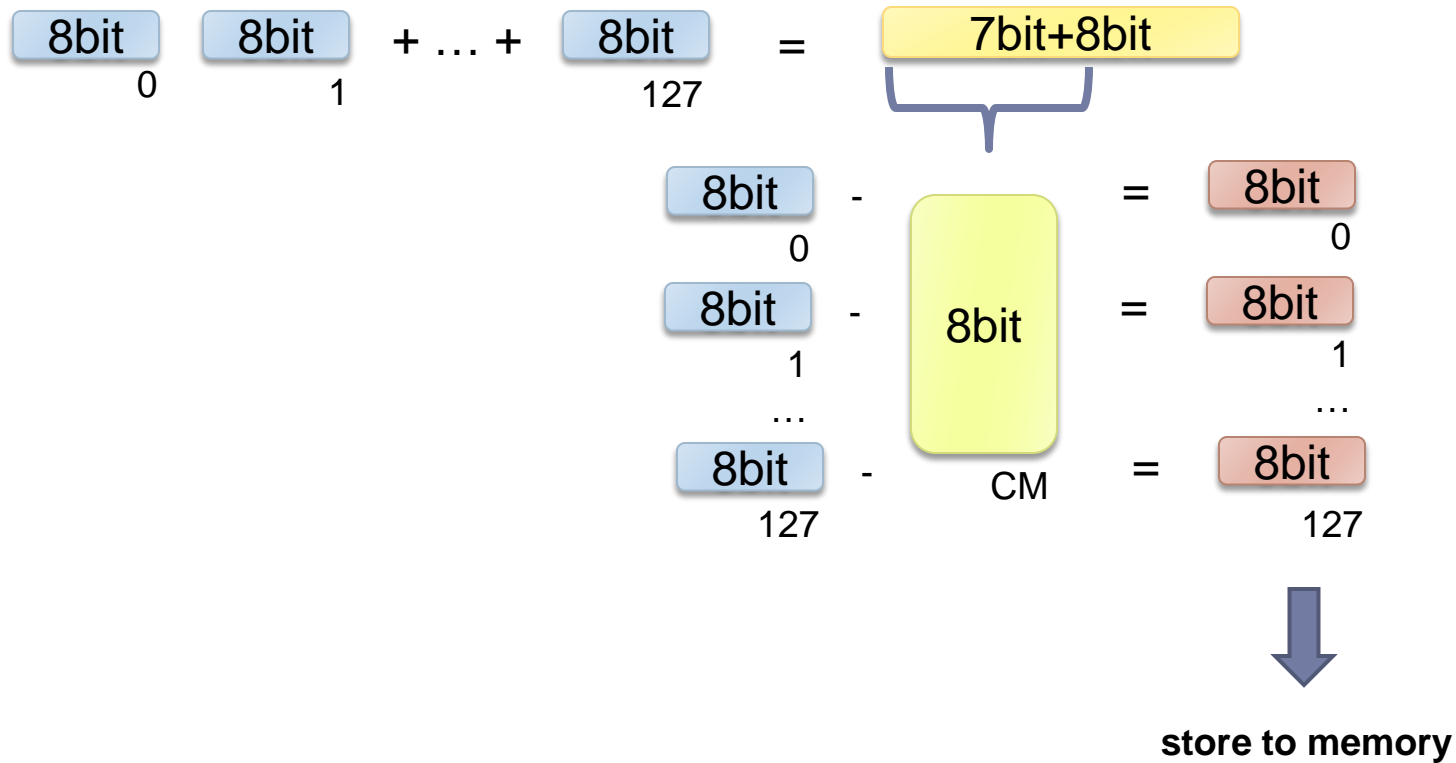
- ▶ **AQUISITION**

Normal operation mode where data are going through all processing stages. Support for trigger and latency buffering.

- ▶ **TEST**

Like AQUISITION but new data are not being recorded.

Common mode

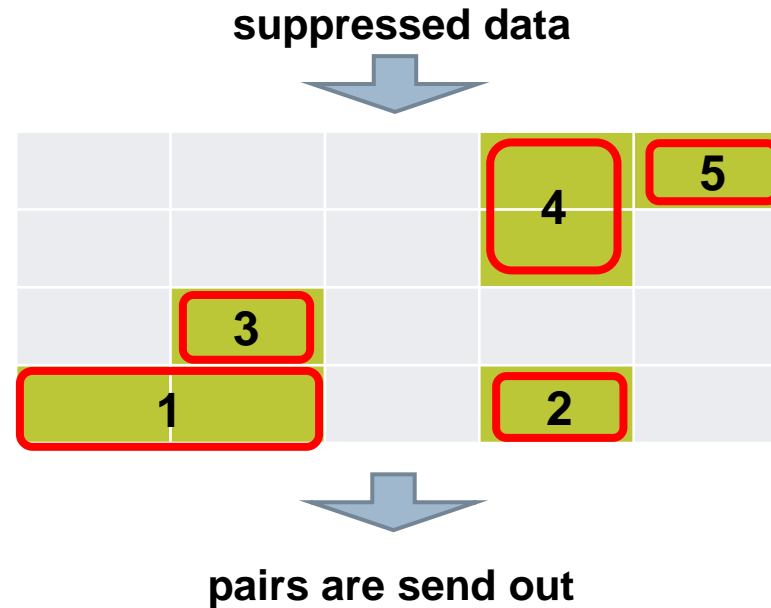


► Pedestal subtraction



Hit Pairing

- ▶ Parallel pair search (2 rows at a time)

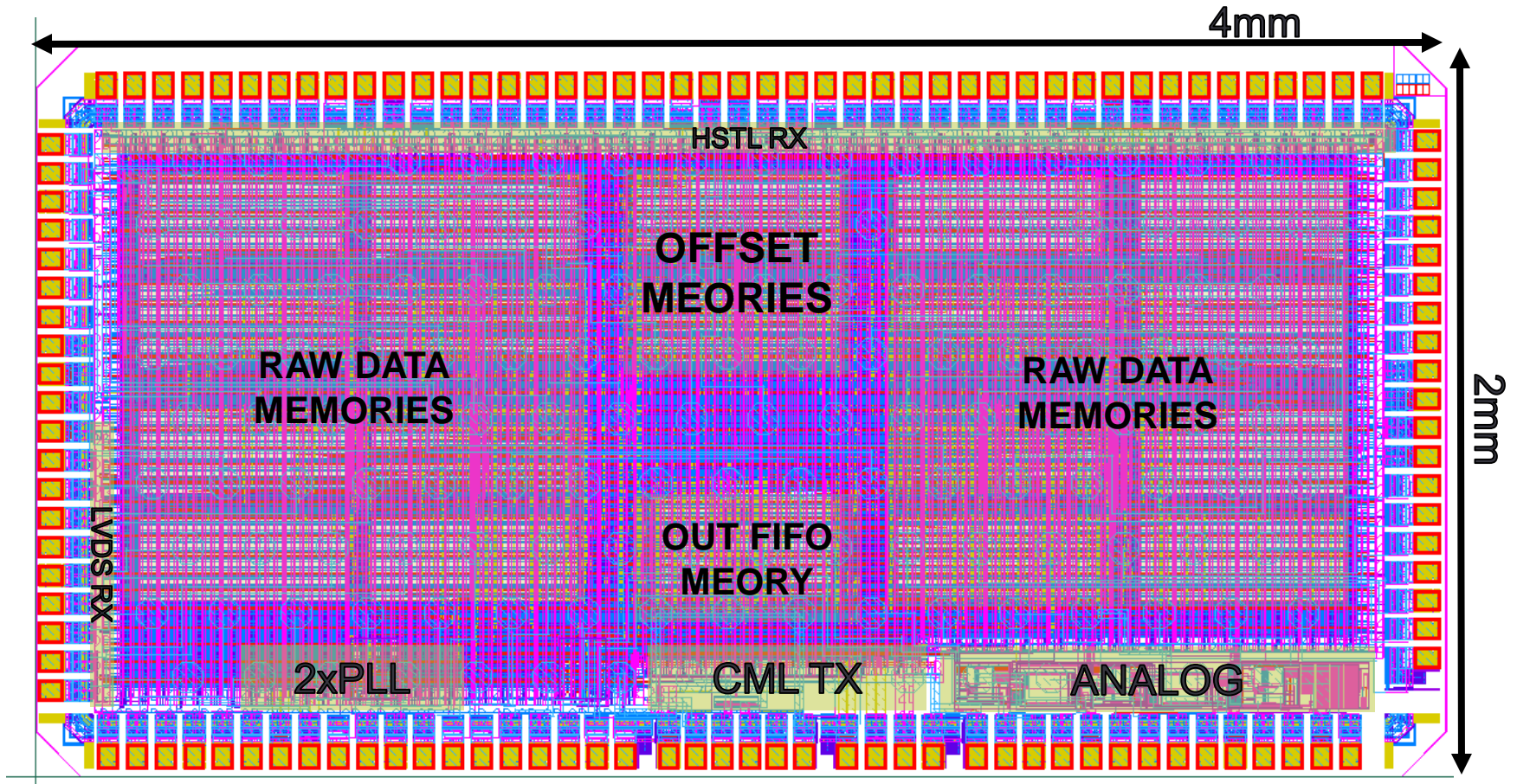


- ▶ Output data format (24 bits)

column	row	orientation	val 0	val 1
5 bit	10 bit	1 bit	8 bit	8 bit

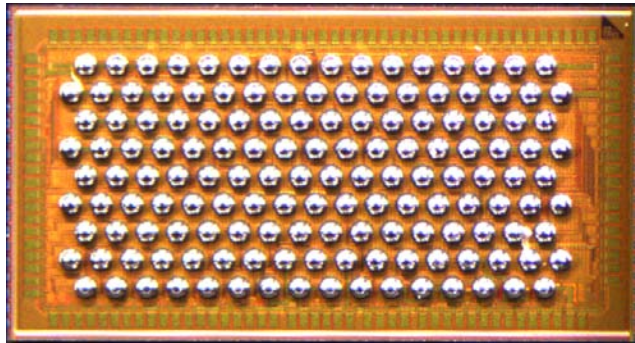
DHP01 - Layout

- ▶ Prototype with 32 input chip

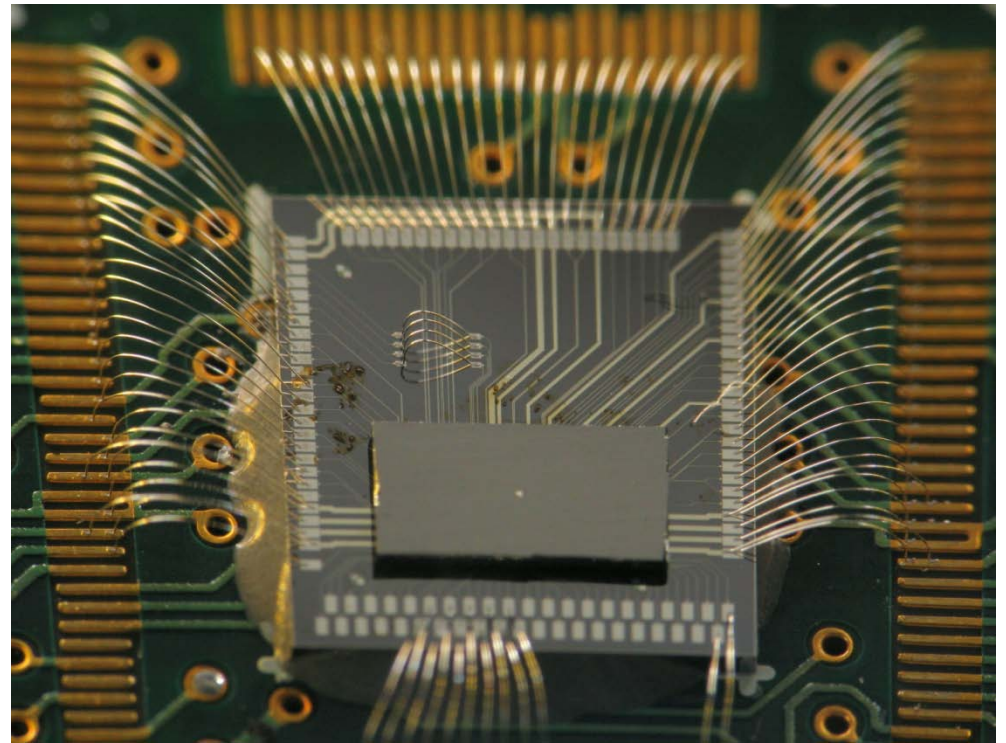
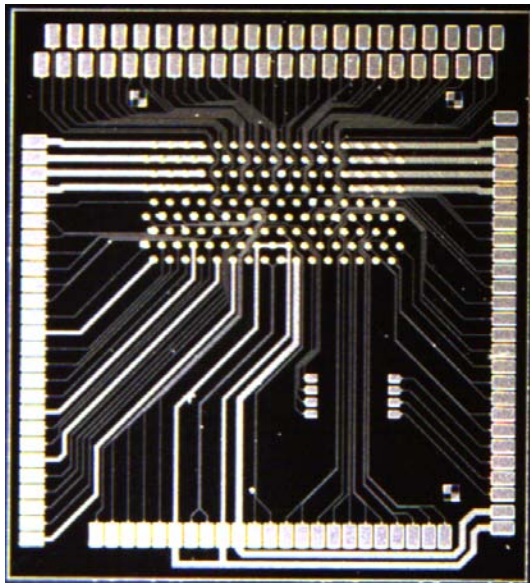


~5.5mln transistors

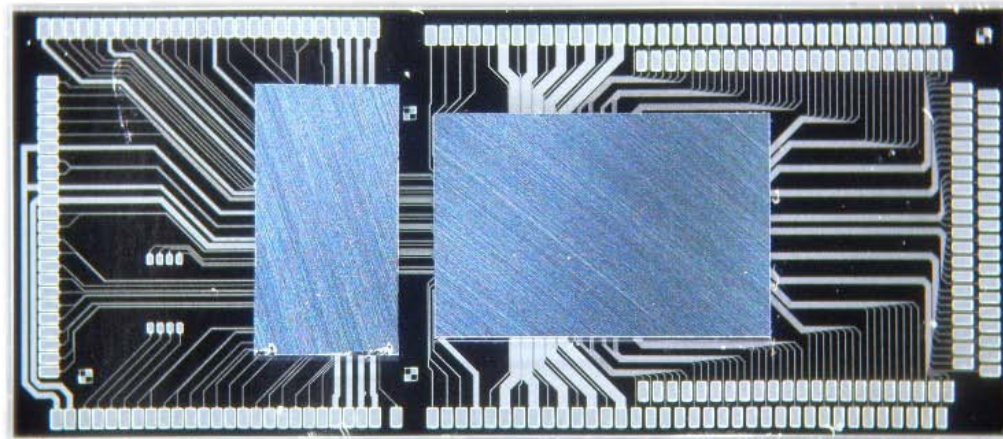
DHP01 – Bump bonding



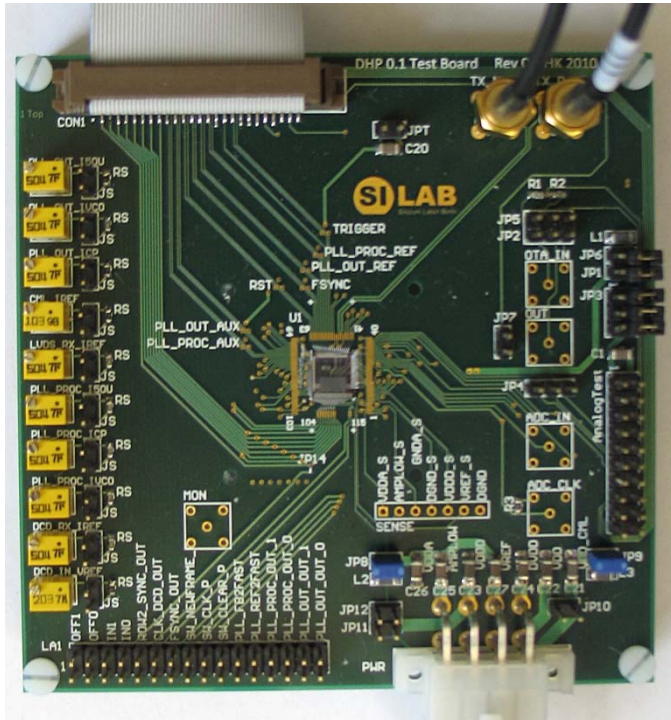
+



DHP01 + DCDB



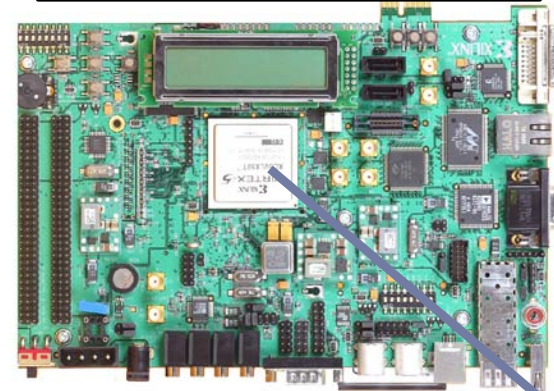
Test Setup



**GPIO
SMA/Coax**



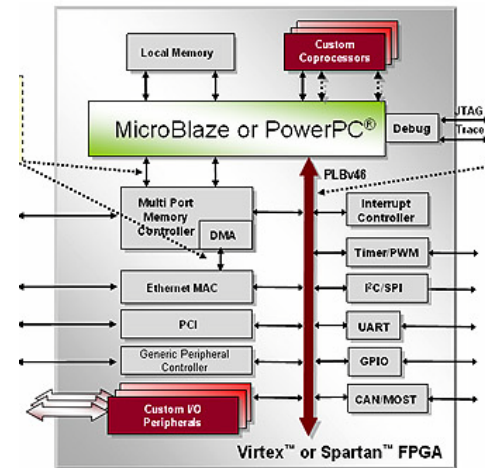
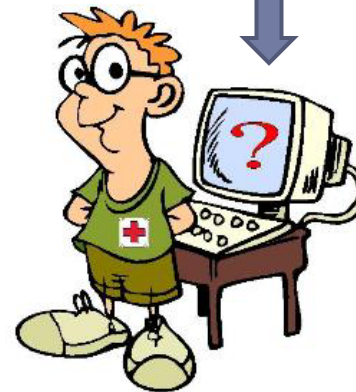
Xilinx XUPV5-LX110T



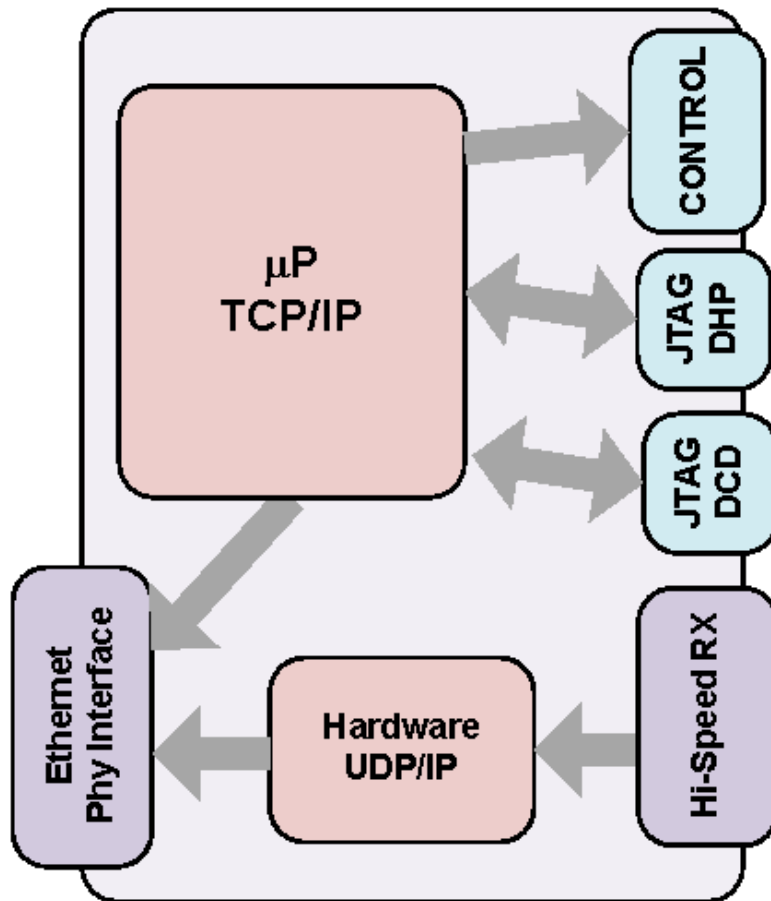
**Ethernet
TCP/IP**



**Ethernet
UDP/IP**



FPGA System Overview



- ▶ Microprocessor responsible for receiving commands (TCP/IP) and controlling chips
- ▶ Independent high-speed (UDP/IP - close to 1Gbit/s) for data

Simple Application

The screenshot shows the DHPBetaTest application interface. At the top, there are input fields for Host Name (192.168.0.3), Port (2001), and UDP Port (6000). Below these are buttons for 'Close', 'Send command', and 'Send Reset'. A text field contains 'CMD DHPJTAG DATA 0x11112222 32'. The main area is divided into two property tables and a command log.

Property	Value
Output Delay	
Core PLL Settings	
S11	<input type="checkbox"/> False
S00	<input type="checkbox"/> False
S01	<input type="checkbox"/> False
S10	<input type="checkbox"/> False
Divide by 5	<input type="checkbox"/> False
RefClk CMOS	<input type="checkbox"/> False
Output PLL Settings	
S11	<input type="checkbox"/> False
S00	<input checked="" type="checkbox"/> True
S01	<input type="checkbox"/> False
S10	<input type="checkbox"/> False
Divide by 5	<input checked="" type="checkbox"/> True
RefClk CMOS	<input type="checkbox"/> False
Other Settings	
Fb2Fast from ...	<input type="checkbox"/> False

Property	Value
Processing Core	
Mode	SEND_BUF
Chip ID	2
Latency	4
Last Row	200
Common Mode	<input type="checkbox"/> False
Common Mode ...	0
Pedestal Subtr...	<input type="checkbox"/> False
Pedestal Order	0
Threshold	0
Row2Sync DC...	0
Frame Sync D...	0
Random Fifo Data	<input type="checkbox"/> False
Switcher Pattern	
Offset Compensation	
Channel Enable	
CML TX	
Random Data	<input type="checkbox"/> False
Do CC	<input checked="" type="checkbox"/> True
Align Time	400

```
>>#DHP 0.1 TEST SYSTEM Firmware
v0.01#
CMD DHPJTAG DATA
0x002000000001 320000000000000000
00590 143
>>RET
0x00001 32000000000000000000590100
02007
CMD DHPJTAG RESET
>>RET
CMD DHPJTAG INST 0xe0 8
>>RET 0x01
CMD DHPJTAG DATA
0x002000000001 320000000000000000
00590 143
>>RET
0x002000000001 320000000000000000
00d90
CMD DHPJTAG DATA
0x502000000001 320000000000000000
00590 143
>>RET
0x002000000001 320000000000000000
00590
CMD DHPJTAG DATA
0x002000000001 320000000000000000
00590 143
>>RET
0x502000000001 320000000000000000
00590
CMD DHPJTAG DATA
0x502000000001 320000000000000000
00590 143
>>RET
```

Testing till now

Working:

- ▶ LVDS Input
- ▶ HSTL like Input (from DCD)
- ▶ Slow control (JTAG)
- ▶ Memories read/write
- ▶ CML Hi-speed link (tested up to 1.555 GHz) data transition
- ▶ Input readout
- ▶ Patter generator
- ▶ DAC
- ▶ Bend Gap

To Do:

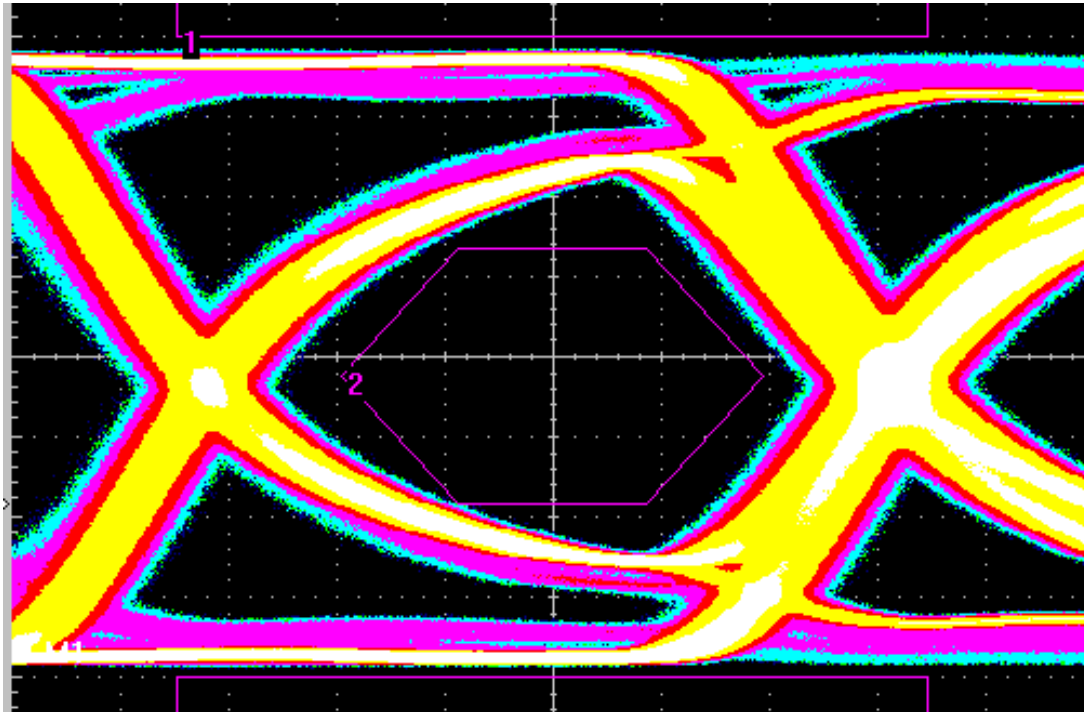
- ▶ Processing (different configurations)
- ▶ DCD communication and synchronization
- ▶ More High Speed testing

Power

- ▶ **Measurement conditions:**
 - ▶ 1.2 V, 400MHz (100MHz Core)

- ▶ **Current consumption:**
 - ▶ CML TX - ~25 mA
 - ▶ 2xPLL - ~5mA
 - ▶ digital core - ~60mA

PLL and CML



- ▶ 1.5552 GHz – data transmission (random 8b10b)
- ▶ WB + ~5 cm PCB + SMA + ~40cm coaxial cable + SMA
- ▶ 100 ps/div
- ▶ 100 mV/div

Problems till now

- ▶ Looks like CMOS output pads can work till ~100MHz (200MHz when bump bonded?) so unable to test with DCD at 400 MHz
- ▶ Configuration of one PLL output (slow one) not fully accusable (simple bug known from submission) there is a workaround
- ▶ Wrong input data format

Timeline

- ▶ Finish test setup to be ready for hi-speed data accusation
- ▶ Prepare setup with DCDB
- ▶ Radiation tests

- ▶ DHP 0.2:
 - ▶ still half size
 - ▶ add custom I/O and bias
 - ▶ Redesign serializer to final version

- ▶ ***Need to develop “final” processing algorithm***



Thank to

Bonn:

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Andre Kruth

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and others

Barcelona:

Albert Comerma

Angel Dieguez

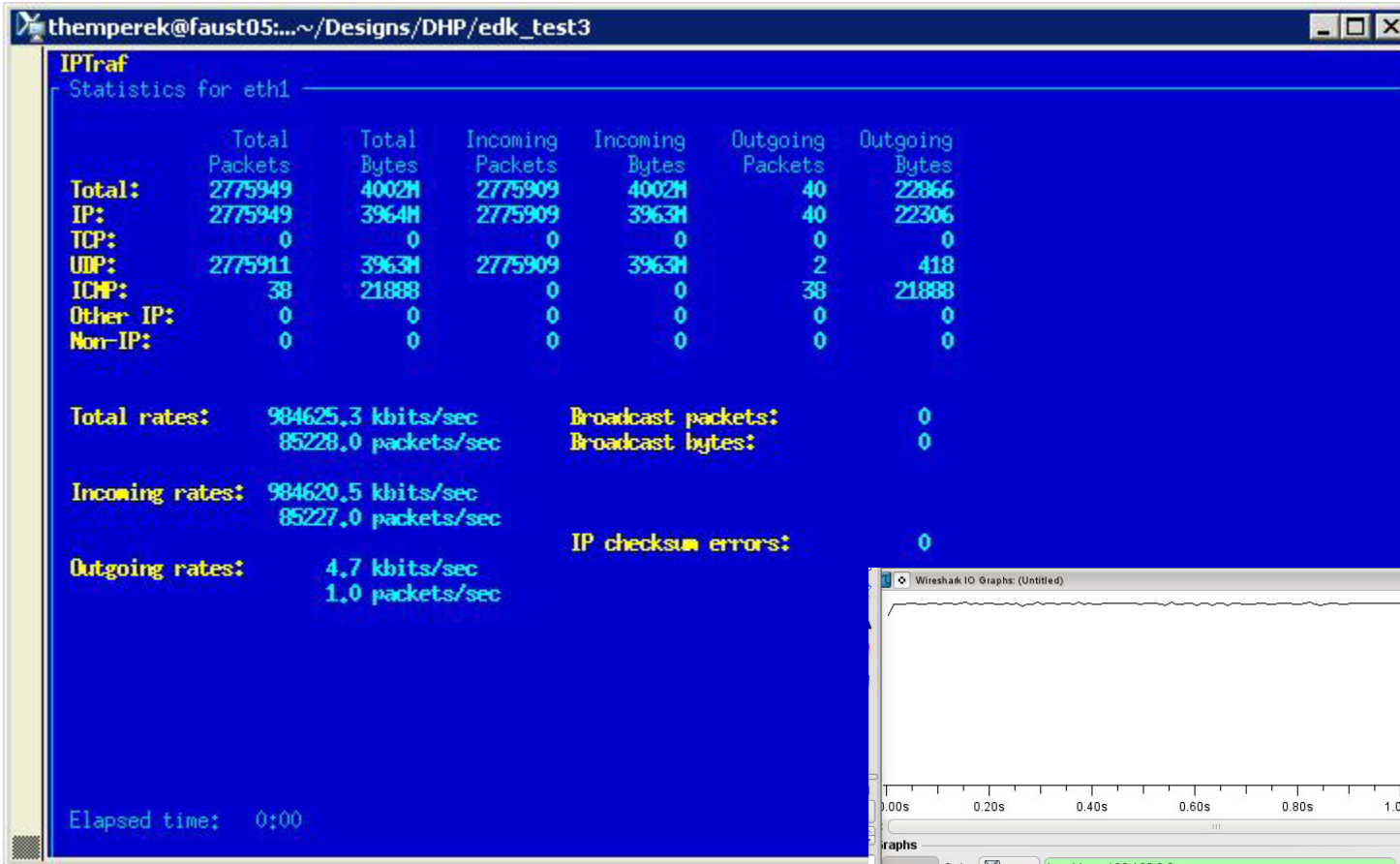
Lluís Freixes

Eva Vilella

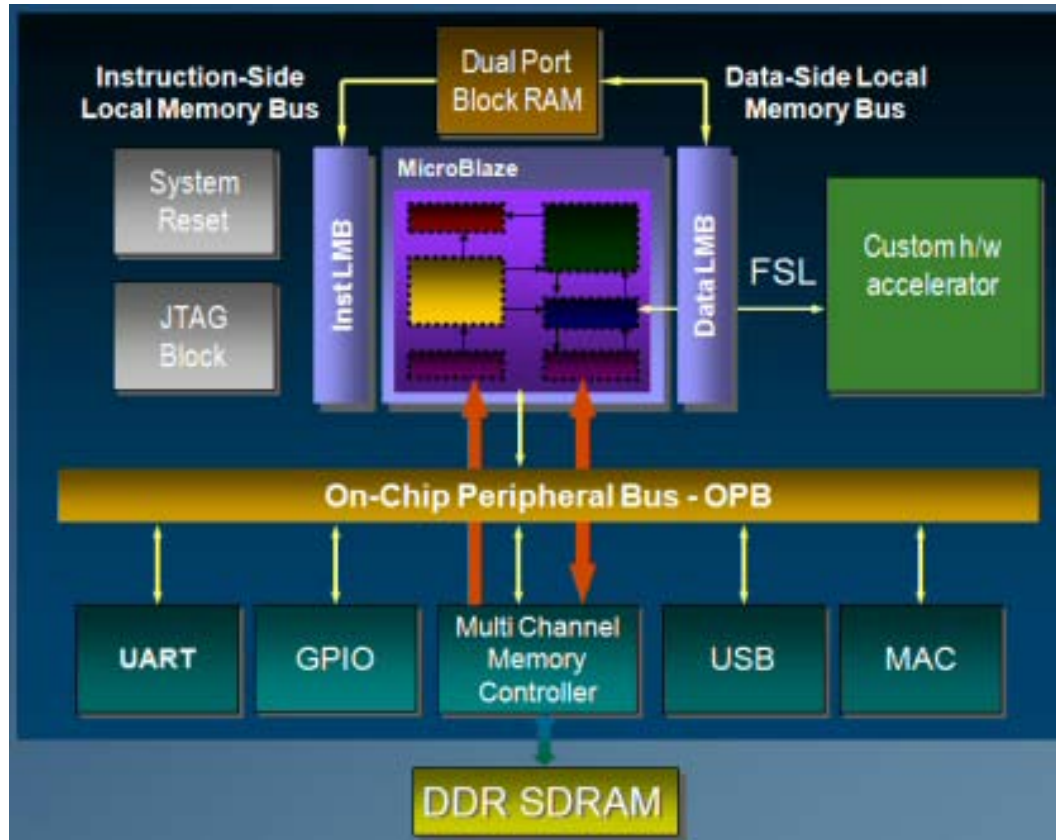
and others

Extra slides

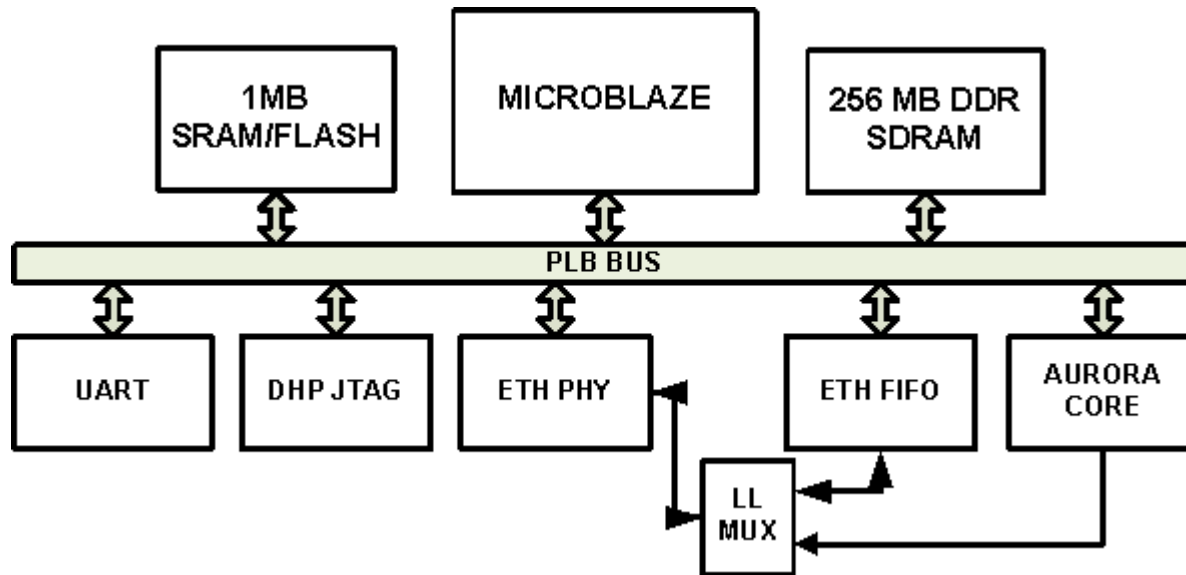
Performance



Embedded Development Kit



Our system



Transmission

