Data Clustering Engine for Belle2 PXD

Status and Integration

A. Wassatsch

Max-Planck-Institut für Physik
Semiconductor Laboratory
Munich (Germany)

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Outline

1. DCE8 test chip
   - status
   - algorithm
   - integration
2. IGEL
   - prototype

DCE8 test chip submission

- full custom layout (due to dice FF) of approx. 1M gates logic + 2M gates from ARM IP (dual-port sram, padcells)
- cross checked layout
  - drc clean: Assura script for fill pattern generation of PC and RX
  - lvs clean: checked against the design schematic
  - simulated with extracted parasitics from the layout (running up to 200MHz)
- ready 3 weeks in advance to submission date (27.09.2010)
  - but: on a short notice the budget for the submission was canceled

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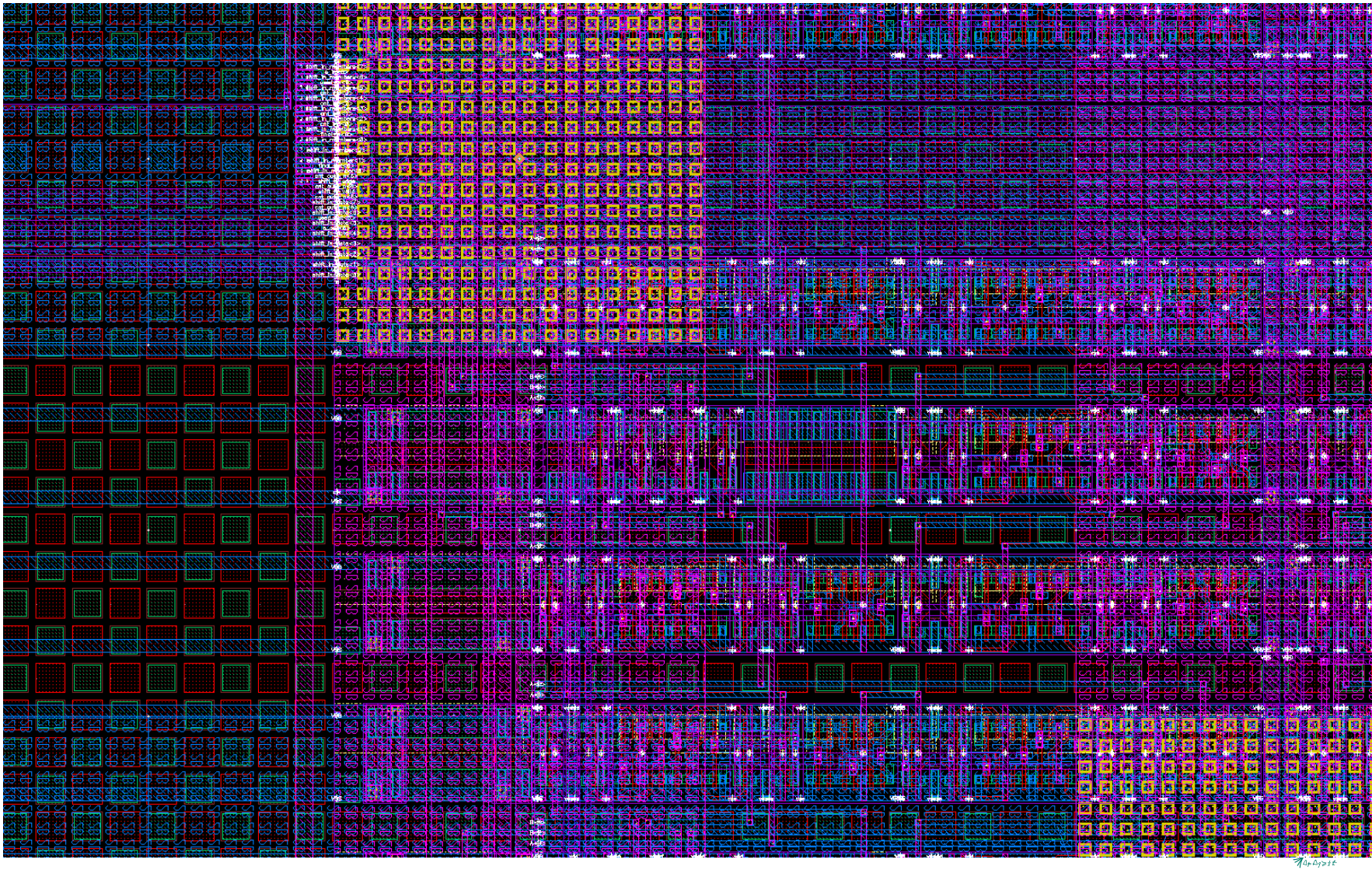

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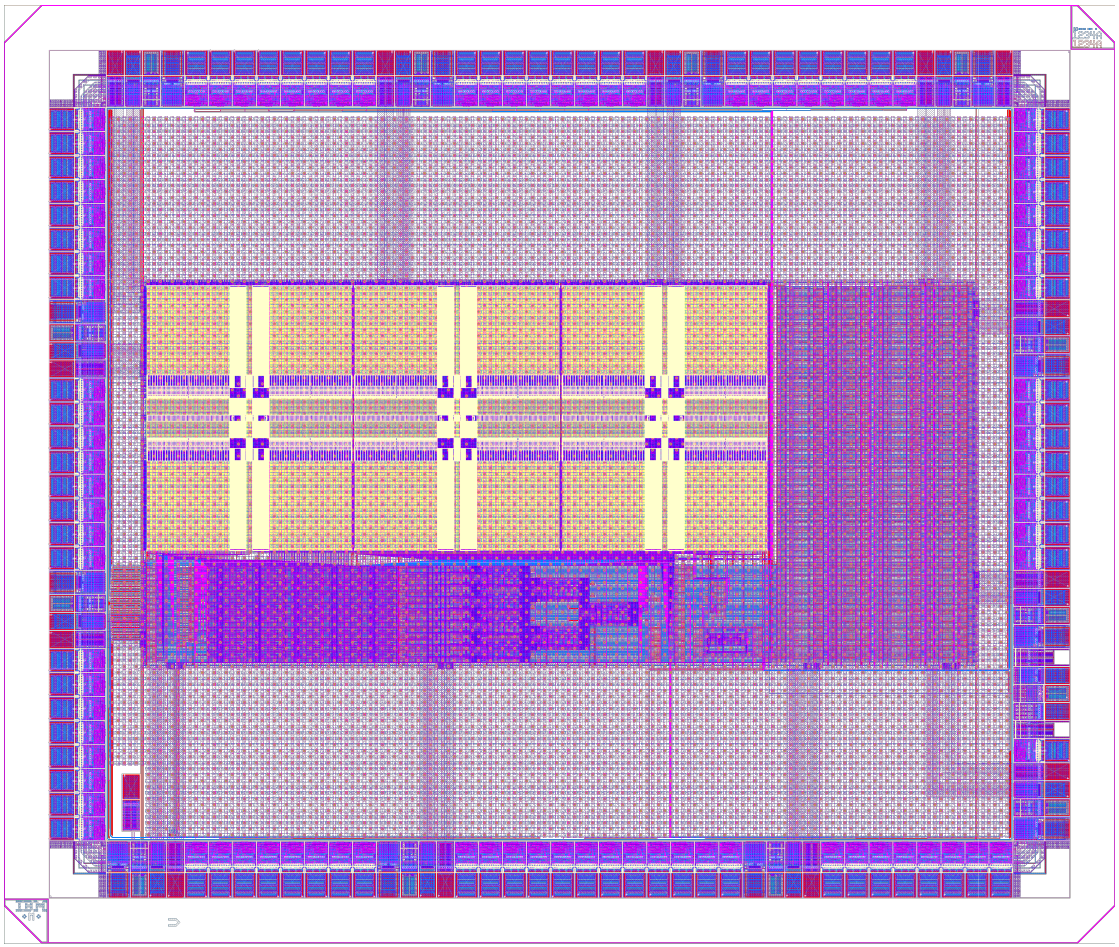
DCE8 layout 03.09.2010



$3.7x3.1mm^2$ full custom layout of 1M gates logic and 2M gates ARM IP

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DCE8 test chip submission (cont.)

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  - integration of the DCE core into the extended DHP 0.2 data flow
- implications by the submission budget drop of
  - adds a delay of at least 3 months do the time schedule, there is still the risk of a additional delay of 3-4 months due to canceled mosis runs
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- interface between physical simulation and HDL-simulation established
- first set of pattern processed
- need now more pattern with realistic data to proceed further

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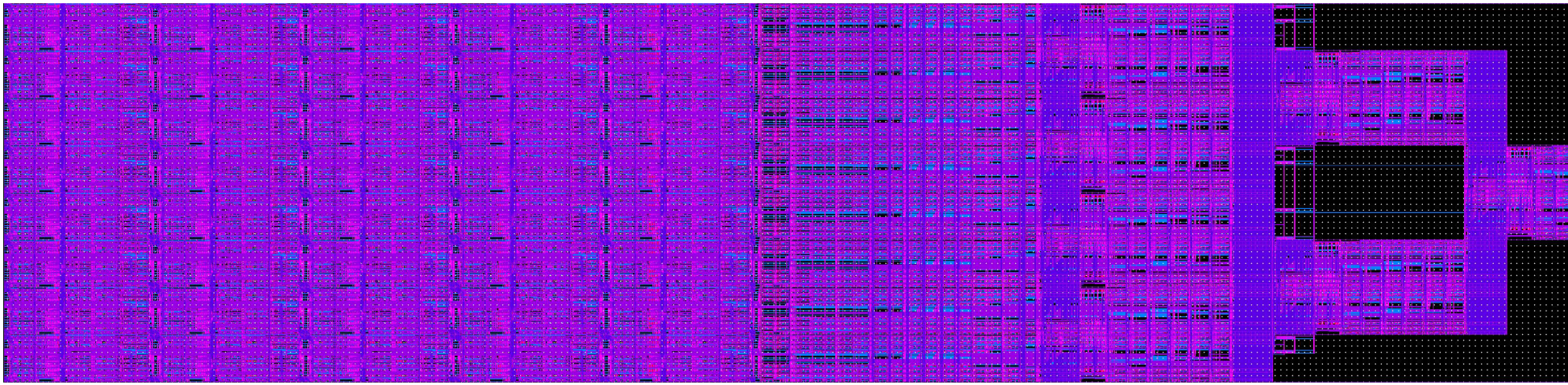
electrical black box IO modell

pure feedthrough $5 + 2 + log_2(n)$ pipeline without reset

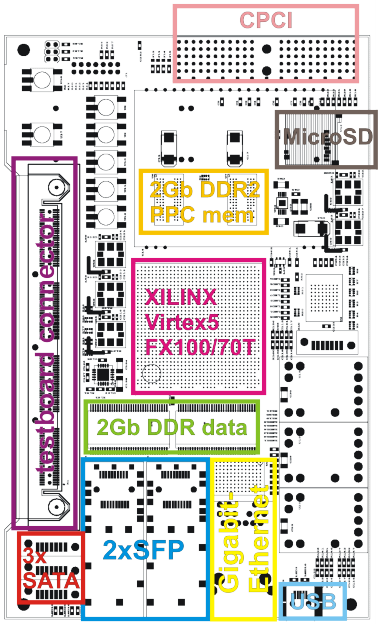
- inputs (single minimum inverter load)
  - row wise full parallel data input
  - clk (row timing)
  - row count
- output (
  - single result vector
  - optional tree pipeline los indicator
- power
  - single power supply (1.2V with approx. 220mA@200MHz) distributed via internal power mesh

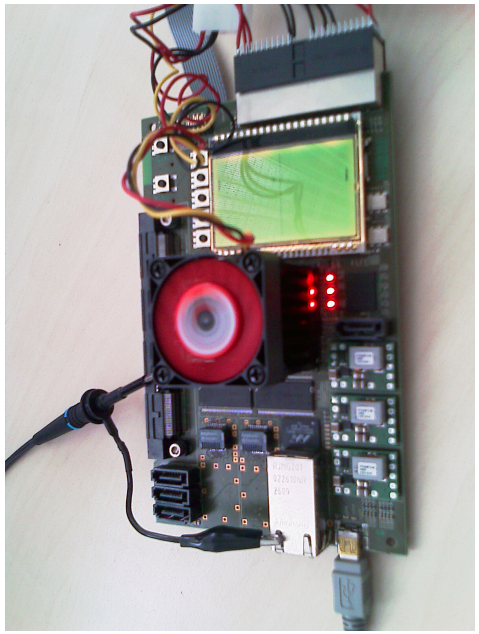
layout considerations



- height: $nx40\mu m$
- width : $5x127\mu m + 240\mu m + log_2(n)x200\mu m$
- only the first 4 metal layers are used in der clustering core

function verification





- 2 functional prototypes
- DDR, DDR2, Gigabit Ethernet via Phy/RJ45 and SFP (800Mb via utp), I2C clocks, Flash, LCD, USB-Uart, ...
- some “flying” wires added
- open points: full GTX freq range, boot-flash, cpci option

next steps

- prepare an reference application (dcd test hybrid?)
- prepare a functional optimized/stripped second version (6 months)
  - fix of additional wires
  - only DDR2 memory (SODIMM)
  - ... ?

Conclusion

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- Interface to simulation data ready and tested , waiting for real testpattern !
- IGEL all major parts succesfully tested, test of serial links in high speed mode needs SDA !

- Outlook
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  - proceed performance analysis with requested testpattern
  - increase the speed of the IGEL high speed serial links

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