DHP simulation for design optimization

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Data Handling Processor - DHP

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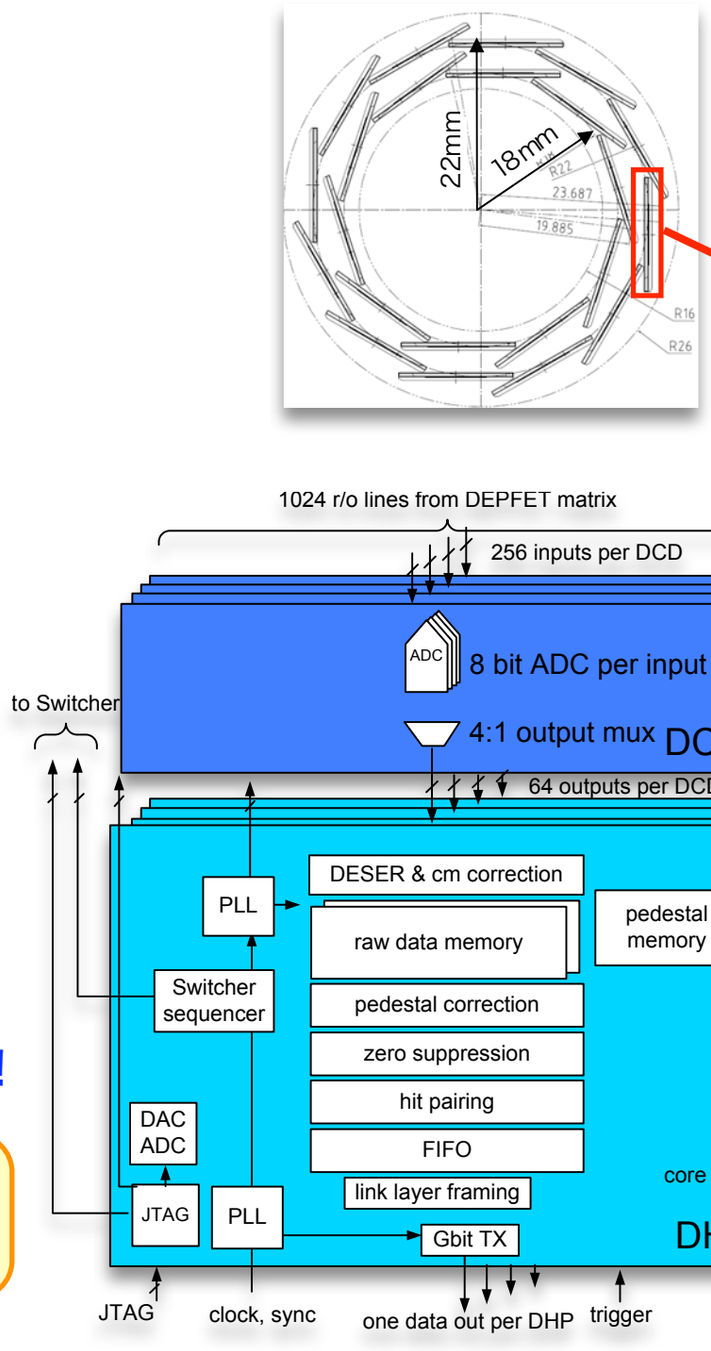
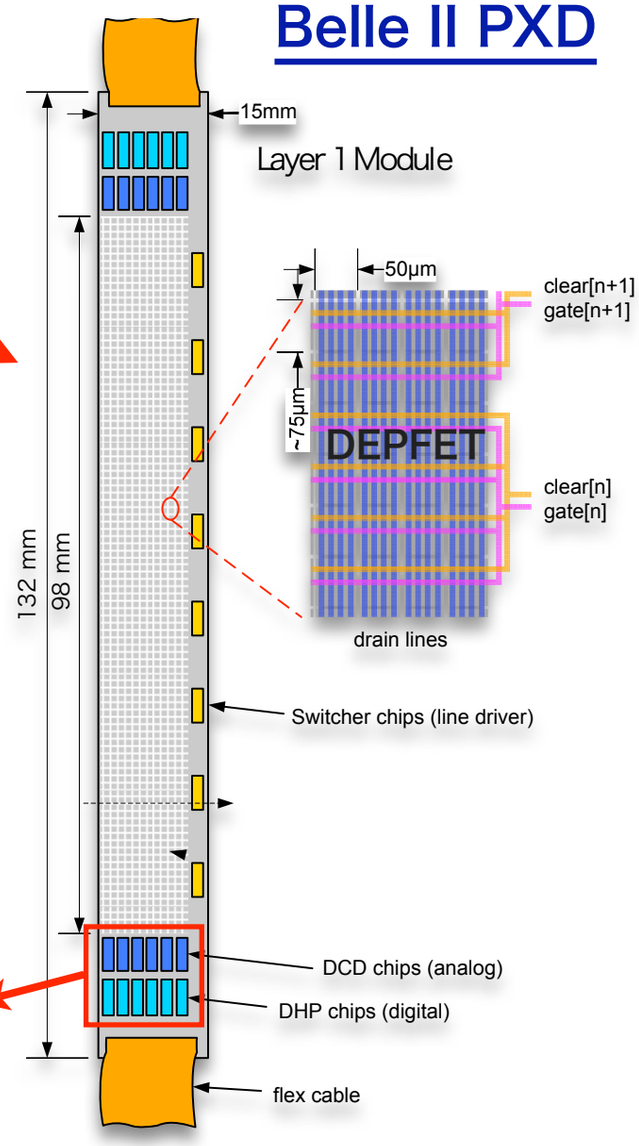
The Pixel Vertex Detector (PXD) is the innermost sub-system in Belle-II.
The DHP will be used to reduce the data rates produced by the DCDs.

- **receive & de-serialize ADC data from the DCD**
- **raw data correction**
  - ✦common mode correction→time dependent offset for all simultaneously sampled pixels
  - ✦pedestal subtraction→correct for fixed offset per individual pixel
- **data reduction**
  - ✦zero-suppression
  - ✦trigger coincidence

PXD to be ready by the beginning of 2013!

☑**The half size DHP 0.1 (32-channel version) is currently tested at Uni. Bonn.**





DHP Data Flow

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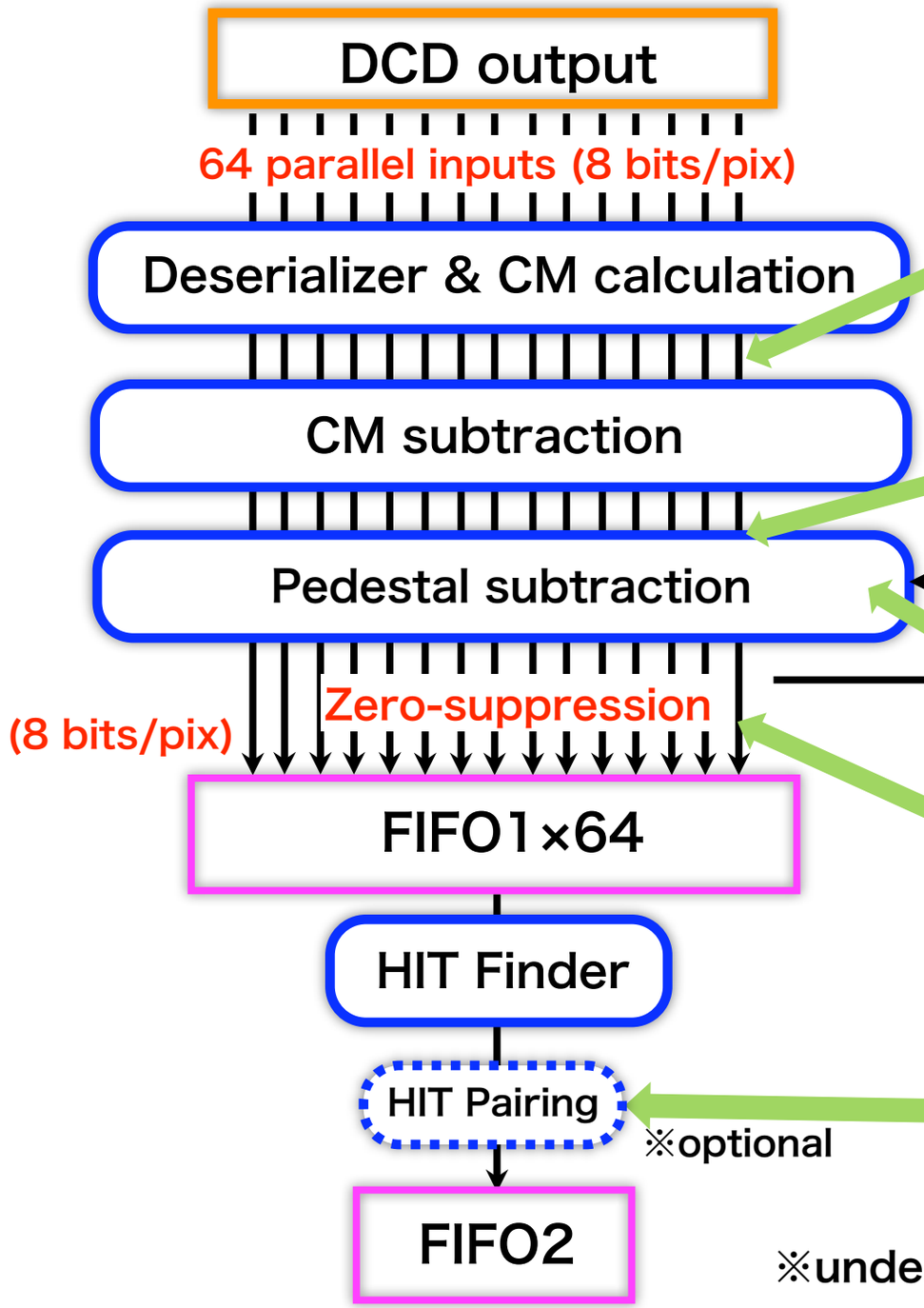

Procedure

- Mean signal value of all simultaneously sampled channels is subtracted as “CM estimator”
- Pedestal can be subtracted an individual but constant value per pixel
- Pedestals may be automatically updated with time (Dynamic pedestal update)
- Signals are compared with zero-threshold
- HIT Pairing tags topological pair flag for cluster events

※underestimated signals are corrected in offline procedure

Since parameters in processing blocks are unfixed, we need to determine with simulation.

DHP Simulator

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Pseudo events
(Monte Carlo, random data)

DCD output

64 parallel inputs (8 bits/pix)

Deserializer & CM calculation

CM subtraction

Pedestal subtraction

Pedestal Memory

Zero-suppression

(8 bits/pix)

FIFO1×64

HIT Finder

HIT Pairing

FIFO2

processed data

- Data quality
- Data efficiency

VS.

Memory resources

Offline correction procedure
(correct underestimated signals)

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Performance analysis of "Data quality"

1. Dynamic pedestal update
→pedestal fluctuation to be suppressed within 1 LSB (8 bit outputs)

2.The data processing error (numerical error)
→to be suppressed within 1 or 2 LSB (8 bit outputs)

3. Clustered events recognition

Performance Analysis – 1. Dynamic pedestal update

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Concept of pedestal update

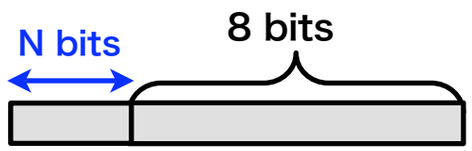
Once pedestal is detected, the new value is averaged with the previous one with

$$P_{\text{new}} = \frac{(2^N - 1)P_{\text{old}} + P_{\text{current}}}{2^N}$$

N: update order

☺ Easy implementation (bit shifts)

☹ The buffer storing the intermediate value need more bits than DCD input signal:



Open-issue

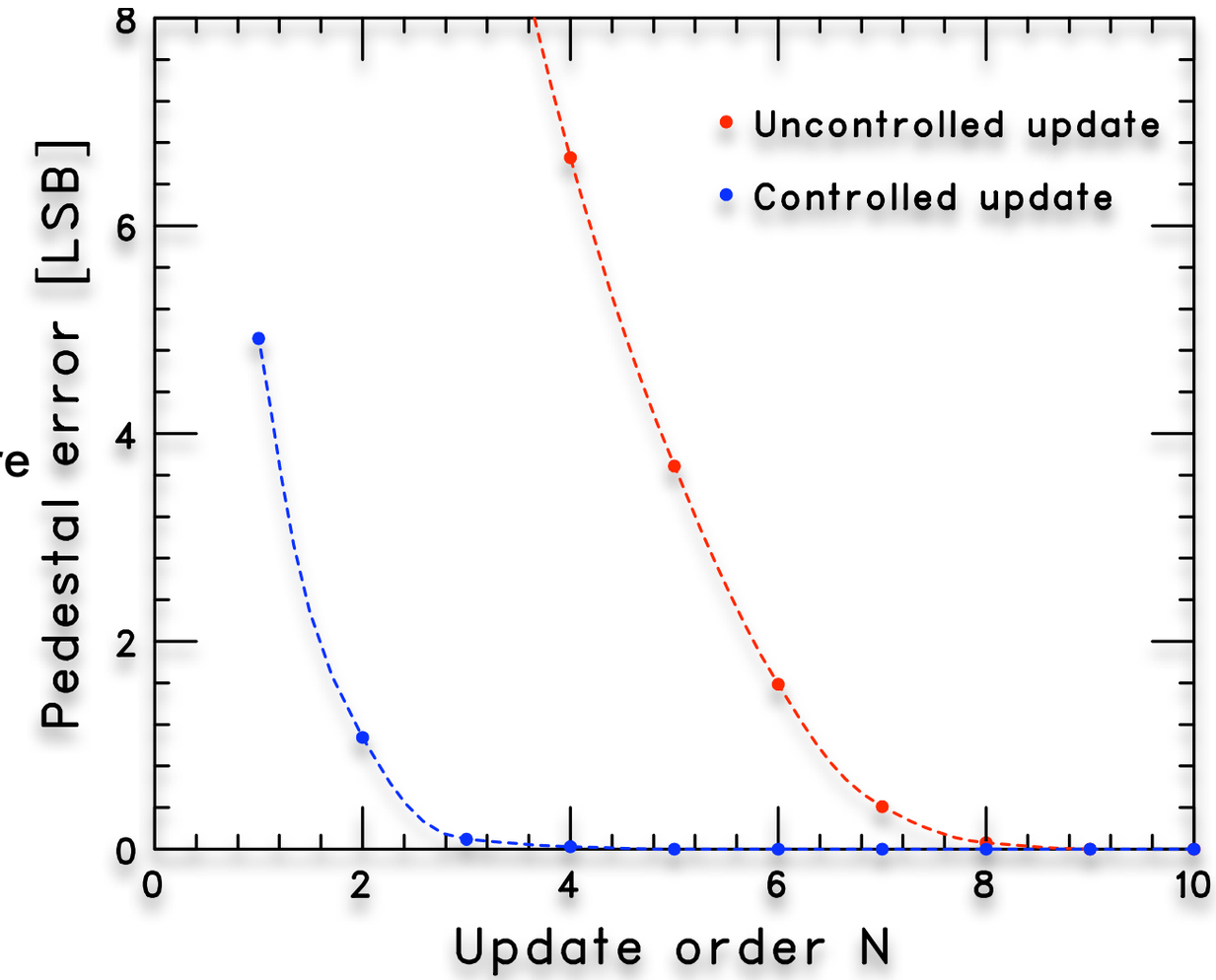
+

Controlled update: update pedestals when no signals are detected in each row

Uncontrolled update: unconditionally update pedestal values→occupancy-sensitive

Estimation of the pedestal error

Inputs: const. pedestal + noise (σ_{noise}=1.4 LSB)



☑ By averaging pedestal values, the pedestal update scheme suppresses or filters out the noise.

☑ For the typical fluctuation around ±1 LSB, at least the update order **N=4** is necessary in the **"controlled"** pedestal update.

Performance Analysis – 2. Data processing error

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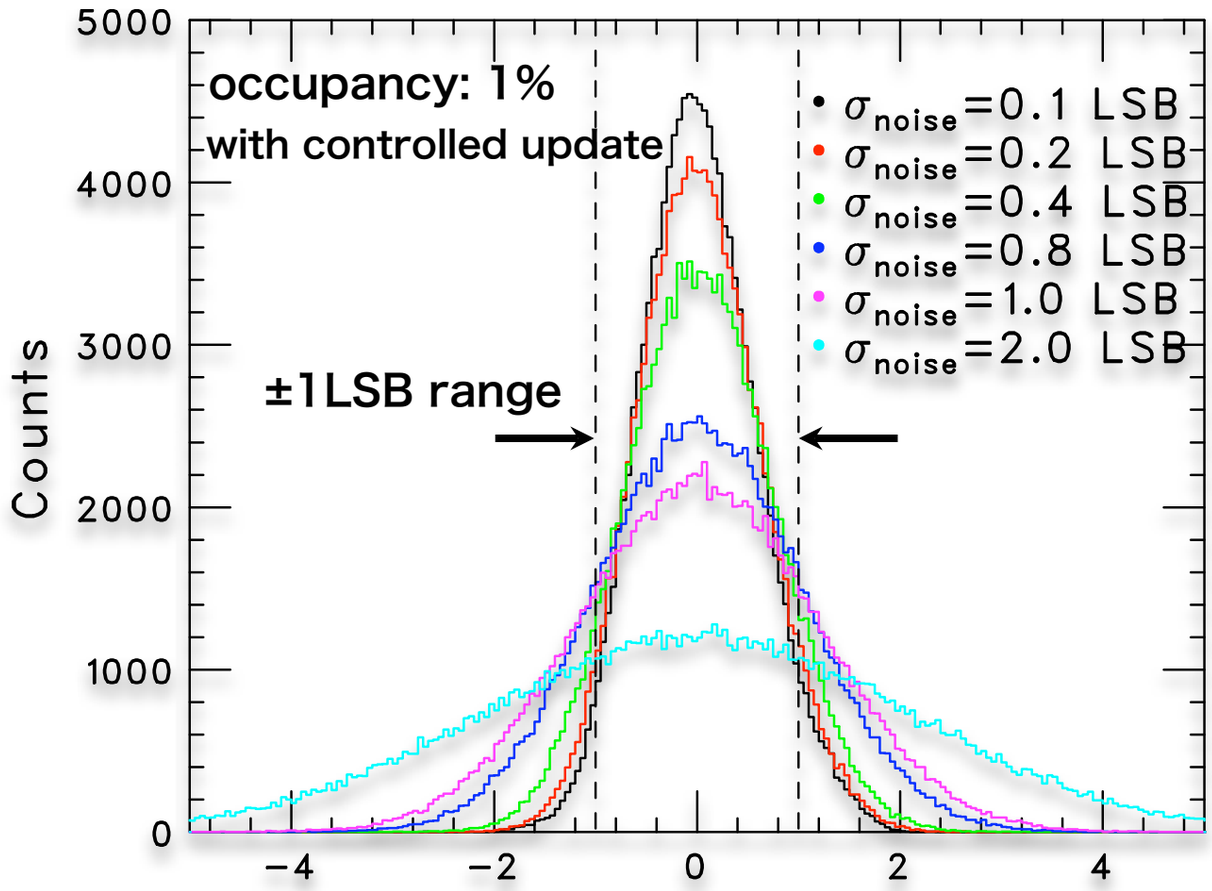
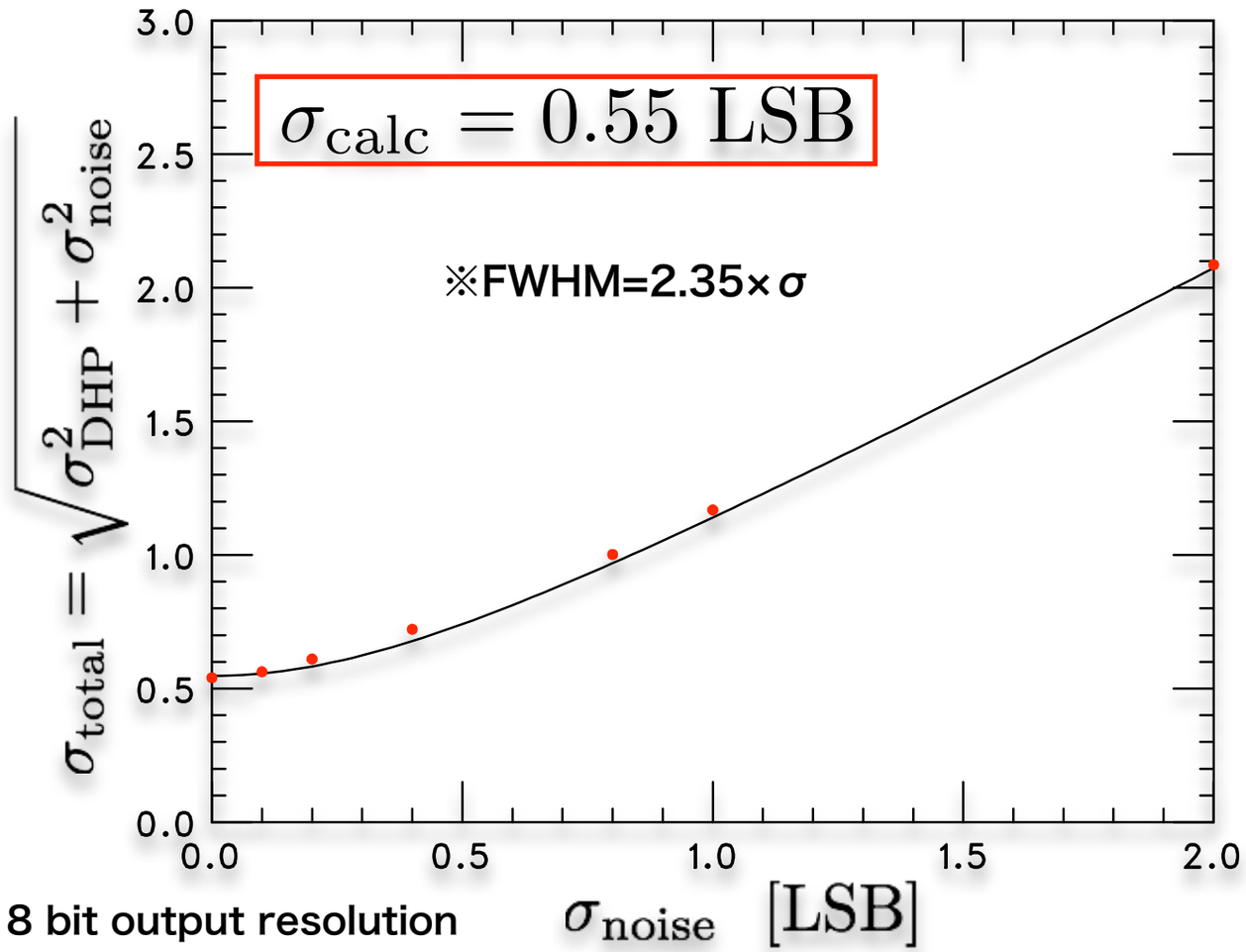
The processing error comes from digitization + round-off.

- CM & pedestal subtraction with **8 + 4 bits** (**N=4**)
- **Inputs: random signal + time-dep. CM + const. pedestals + noise, 1 pixel events**



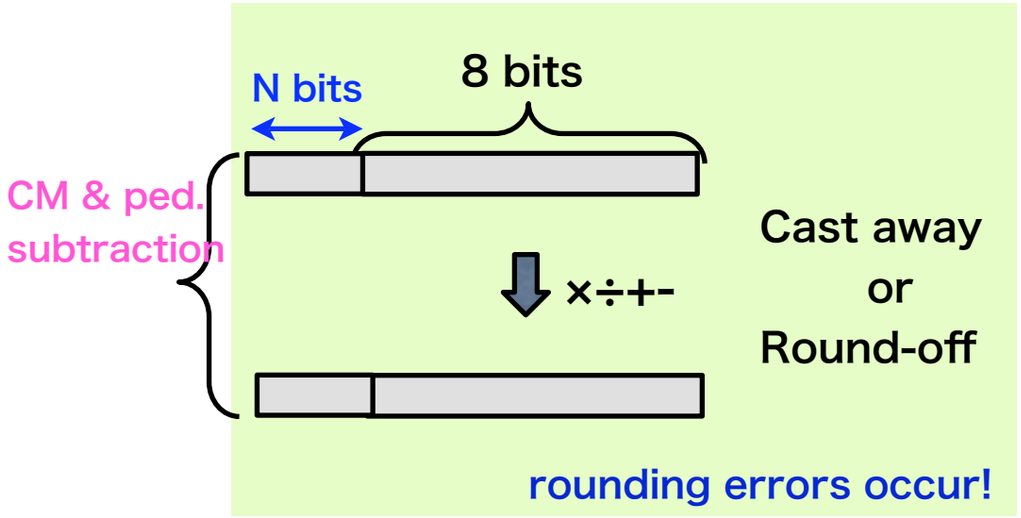


The processing error with **8 + 4 bits** can be estimated to be **σ_{calc} = 0.55 LSB**.
This value should be smaller than the DCD noise.

Performance Analysis – 2. Data processing error (Cont.)

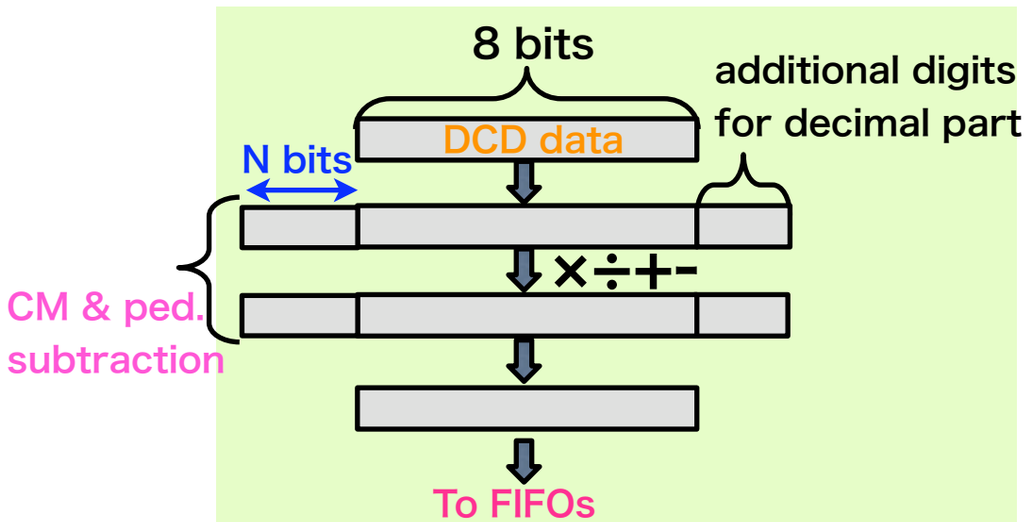
The processing error can be suppressed by increasing additional digits.

Without decimal digits



With decimal digits

Add decimal bits inside the DHP



Performance Analysis – 2. Data processing error (Cont.)

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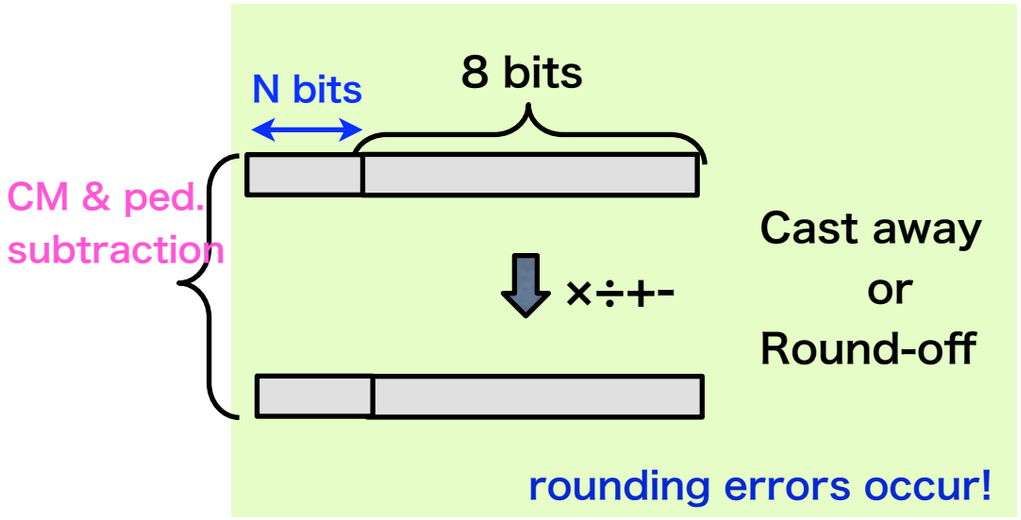
The processing error can be suppressed by increasing additional digits.

Without decimal digits



With decimal digits

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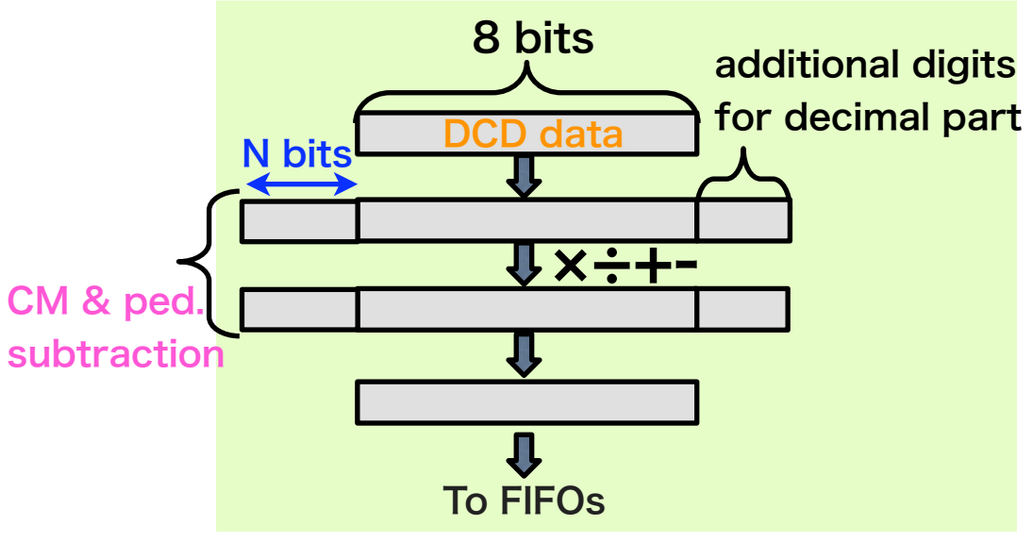
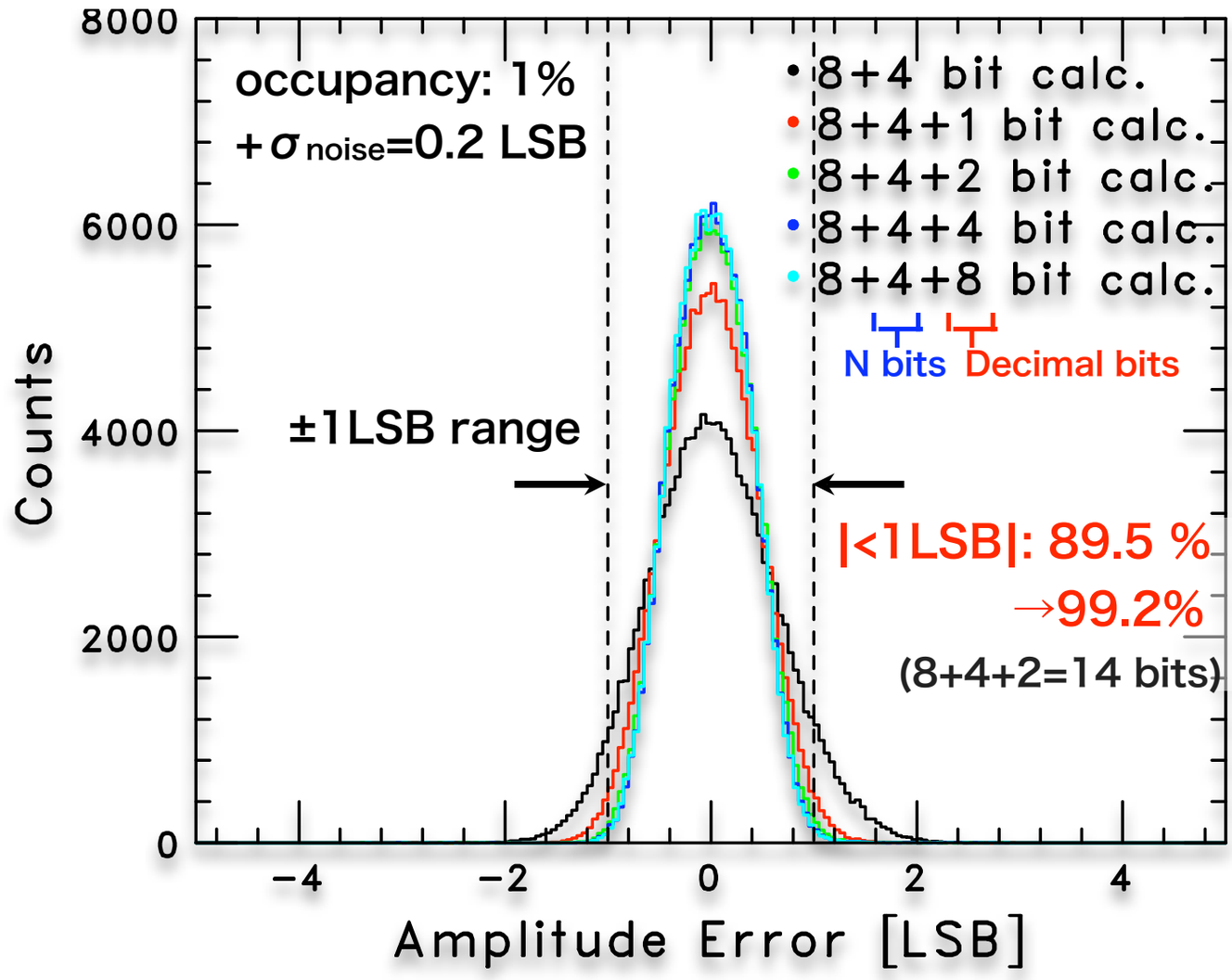


Additional decimal digits dependence



☑ At least **14 bit** (=8 (DCD) + 4 (update order N) + 2 (decimal part)) calculation width might be necessary inside DHP for CM + ped. subtraction.

☑ Increasing calculation width is valid only if $\sigma_{noise} < \sigma_{DHP}$

Performance Analysis – 3. Clustered event recognition

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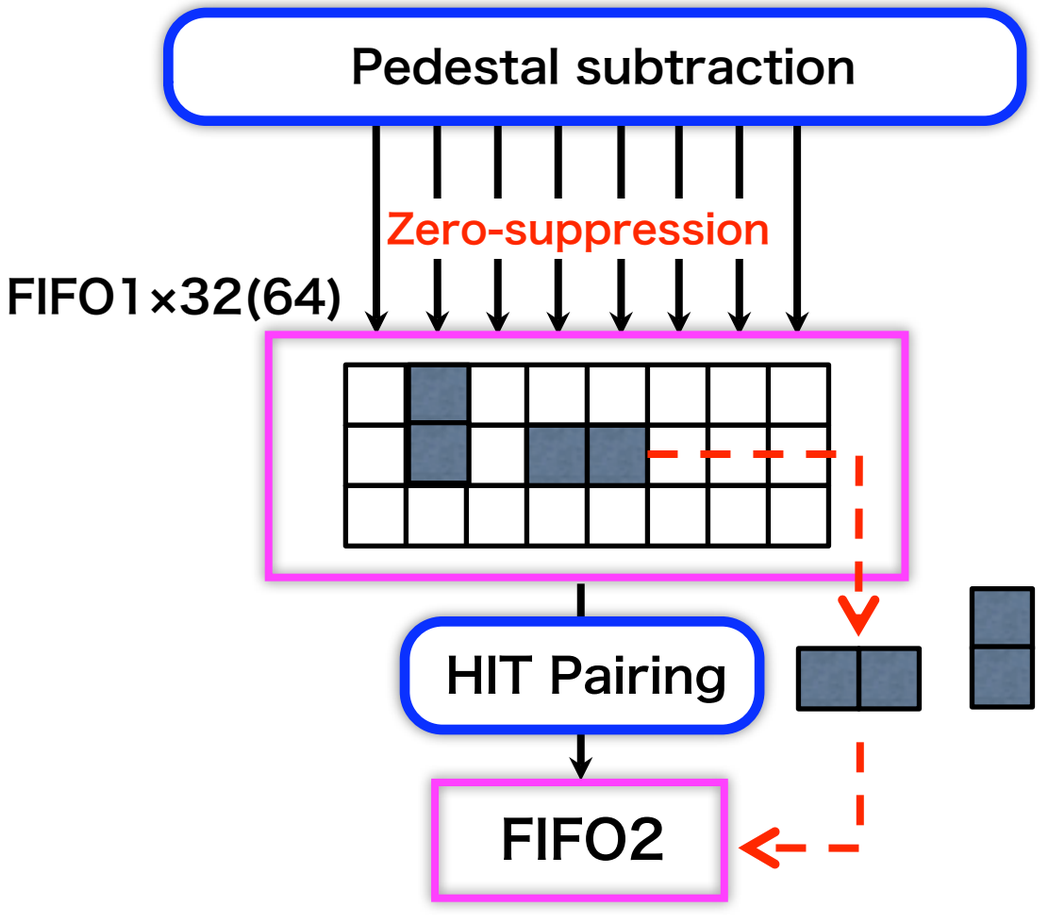
Clustered events strongly depends on the geometry and noise characteristics of the PXD.

Pairing scheme (DHP 0.1)

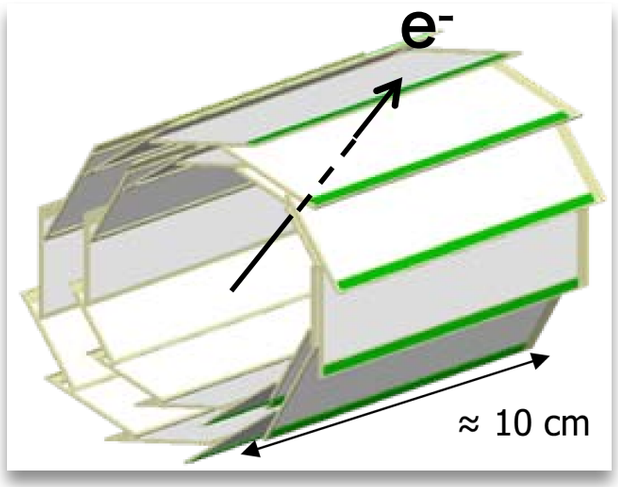
Pairing is performed for zero-suppressed data.

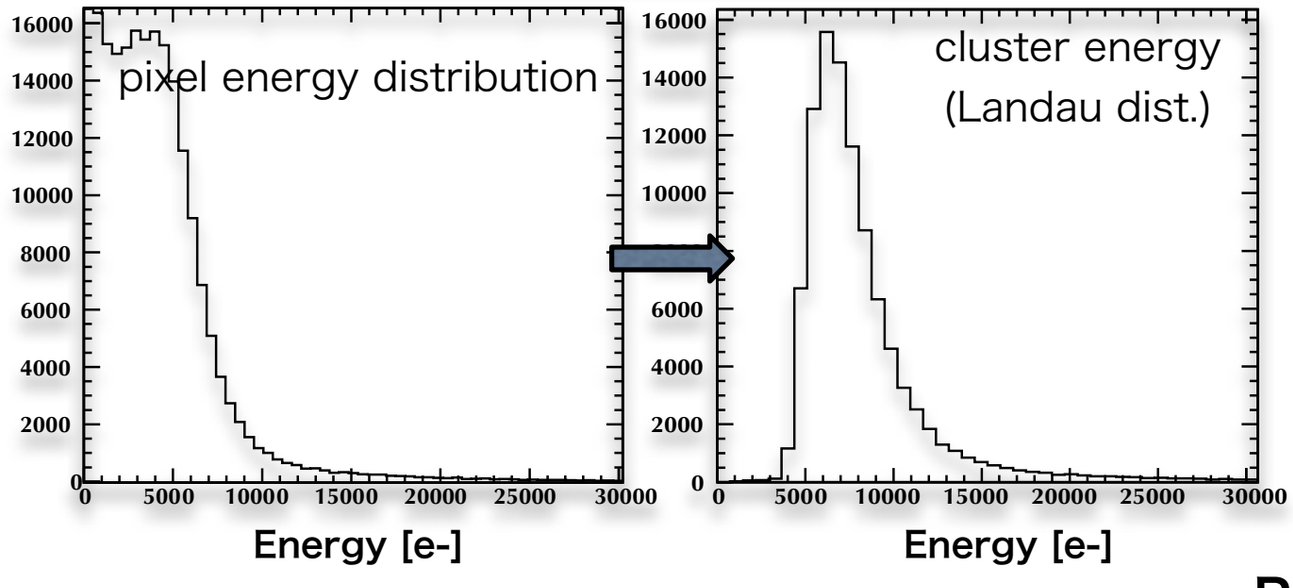


Pairing for sequential pixels (FLAG 0/1) and send only one address per double hit

Pseudo-events are generated with Geant4 Monte Carlo simulator (SiPxlDigi, MPG framework)

- Energy: 0.3 keV - 1GeV
- θ angle: 30 - 170deg (uniform in cos θ)





Performance Analysis – 3. Clustered event recognition (Cont.)

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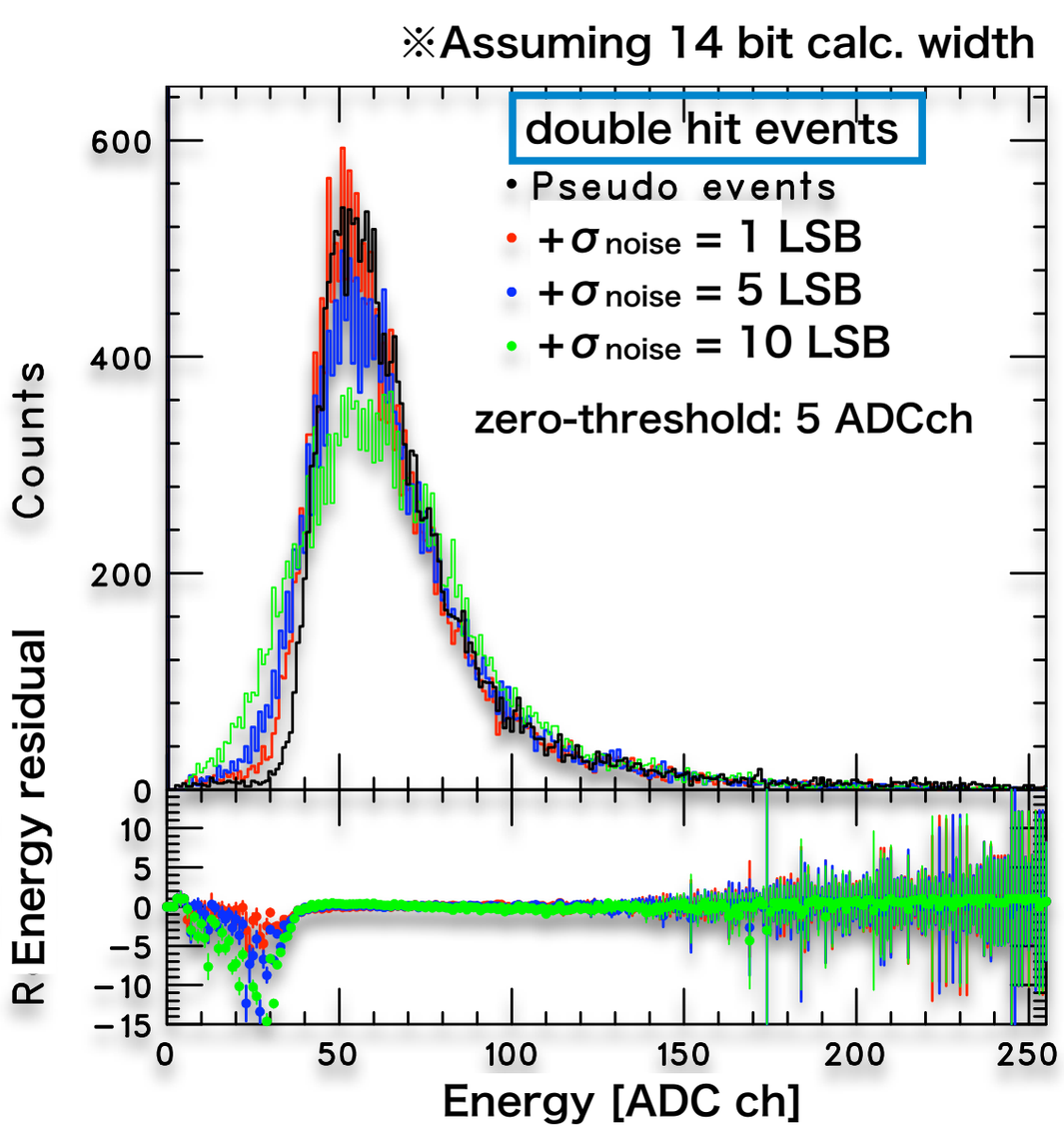
Energy reconstruction



☑Pairing scheme in the DHP 0.1 seems valid for clustered events.

But hit pairing is closely related with:

Data format

- generic raw data format: 16 bit address + 8 bit ADC data = **24 bit**
- with hit pairing: 16 bit address + 8 bit ADC data1 + 8 bit ADC data2 + 1 bit pair flag = **33 bit**

Data reduction factor

- hit pairing: 2/3 - 4/3, depending on cluster size distribution
- trigger data: 5.5 for 10 kHz trigger rate, 2.2 for 30 kHz for poisson trigger distribution

☑We need to consider the pairing scheme with taking data efficiency (lost hist vs. FIFO sizes, occupancy etc.) into consideration. → simulator!

Conclusion & Future Prospect

☑ The DHP simulator is developed for optimizing signal processing.

-processing error
-clustering efficiency (address compression)
-data efficiency (lost hits vs. occupancy, FIFO sizes)

☑ The realistic background data generated by the Monte Carlo simulation which includes the QED processes will be used as an input parameter.

☑ The test beam with DCD + DHP emulator readout system is planned on this November, and its result will help us to optimize various design parameters.

Thank you very much!