# DHP 0.1 analog blocks **preliminary** measurements

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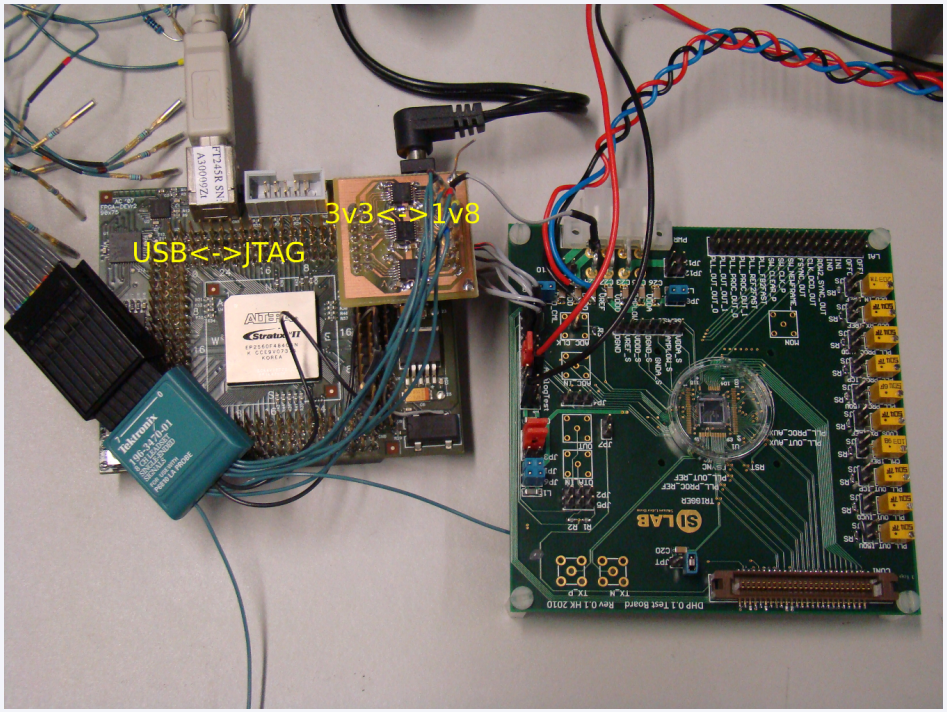
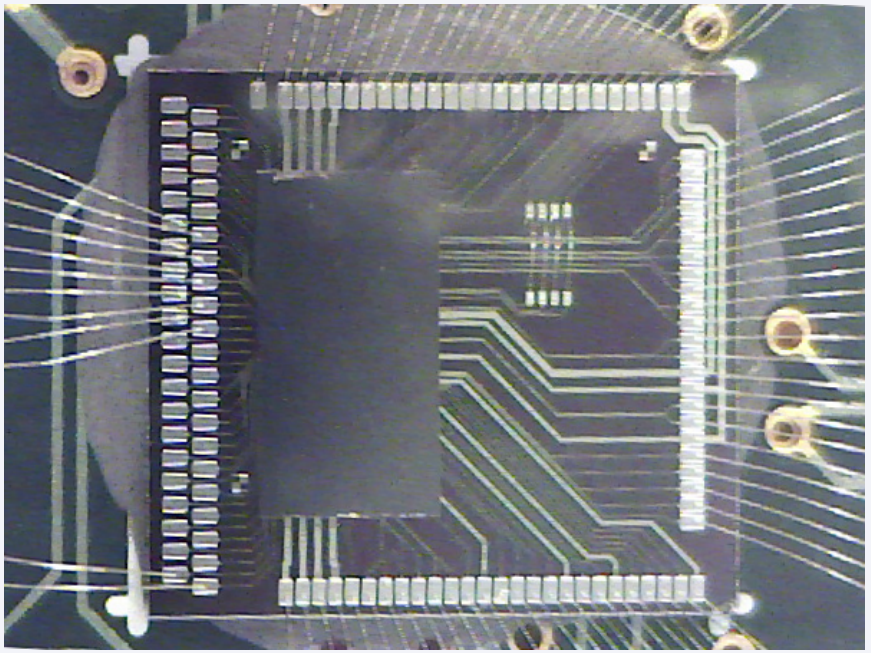
$5^{th}$ International workshop on DEPFET Detectors and Applications
$29^{th}$ September - $1^{st}$ October 2010 - València

# Test Setup

Power from Agilent E3631A.
Logic analyzer TLA7012 for debug digital signals generated from FPGA board.
TTi 1906 GPIB multimeter for readout of analog signals.



# JTAG

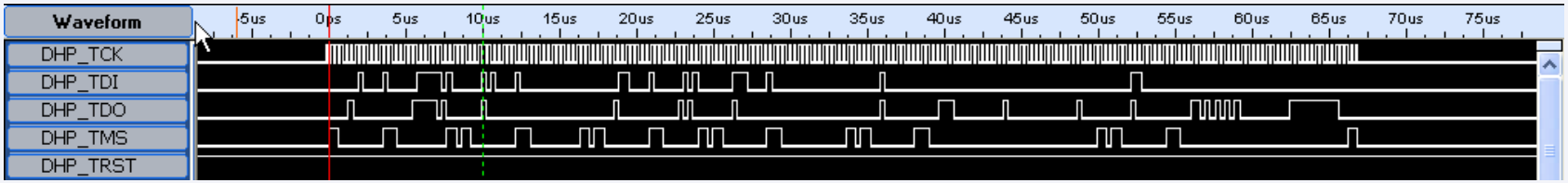
All device capabilities are controlled by a JTAG interface.

- JTAG has four registers for analog control: DAC, DAC ENCLOSED, BANDGAP and ADC.
- DAC and DAC ENCLOSED are used to setup a fixed value to the corresponding DAC (8 bits).
- BANDGAP register uses 4 bits to control operating voltage of the bandgap, and a fifth bit to control ADC start of conversion.
- ADC register is used to read the 10 bits data plus 1 bit EOC signal.
- ID register and UCODE register with fixed data for debugging purposes.

A JTAG interface with a C++ software to control it has been developed for this tests.

# JTAG

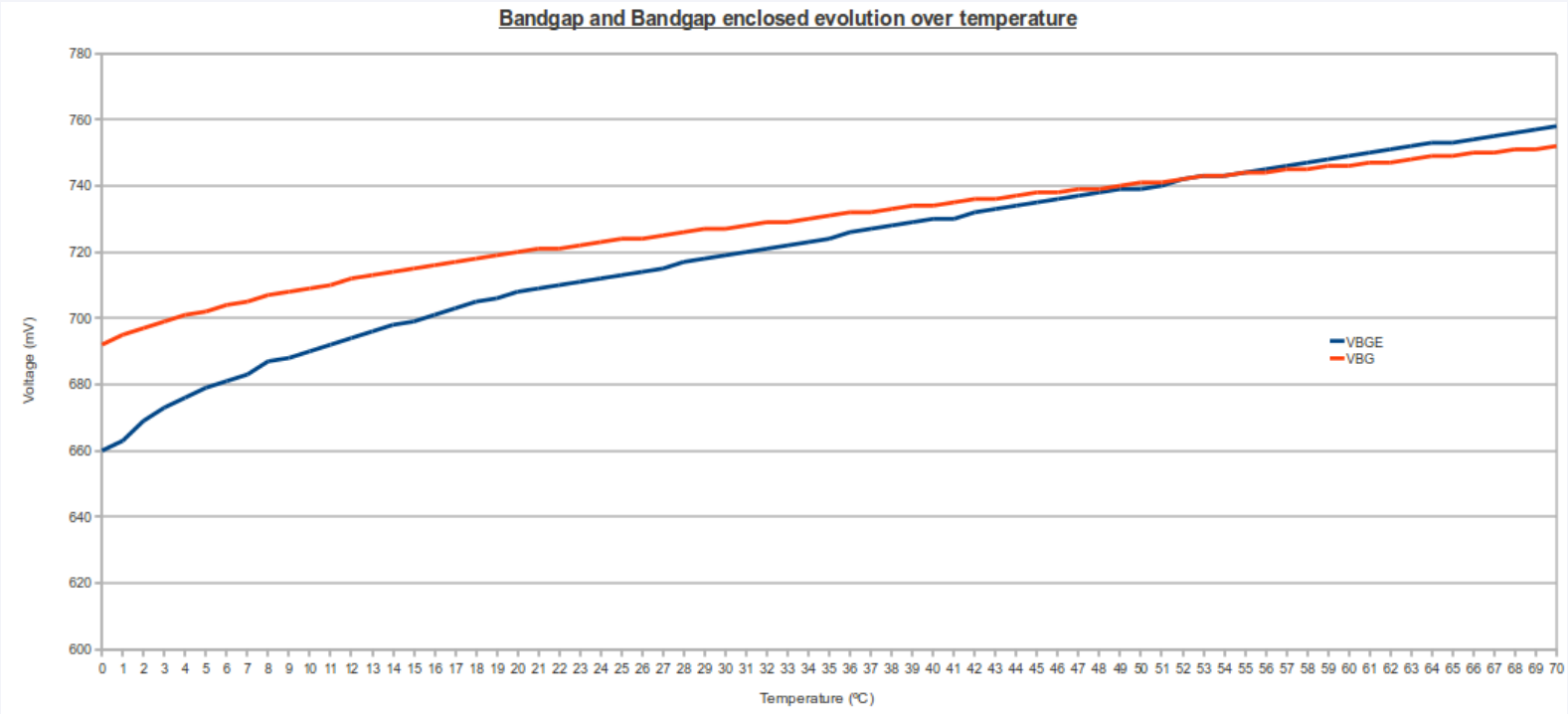
An example of the full access to all registers is shown in next waveform.




Note that JTAG clock is switched off once the device is setup to avoid digital noise in the analog measurements.

# Bandgap performance

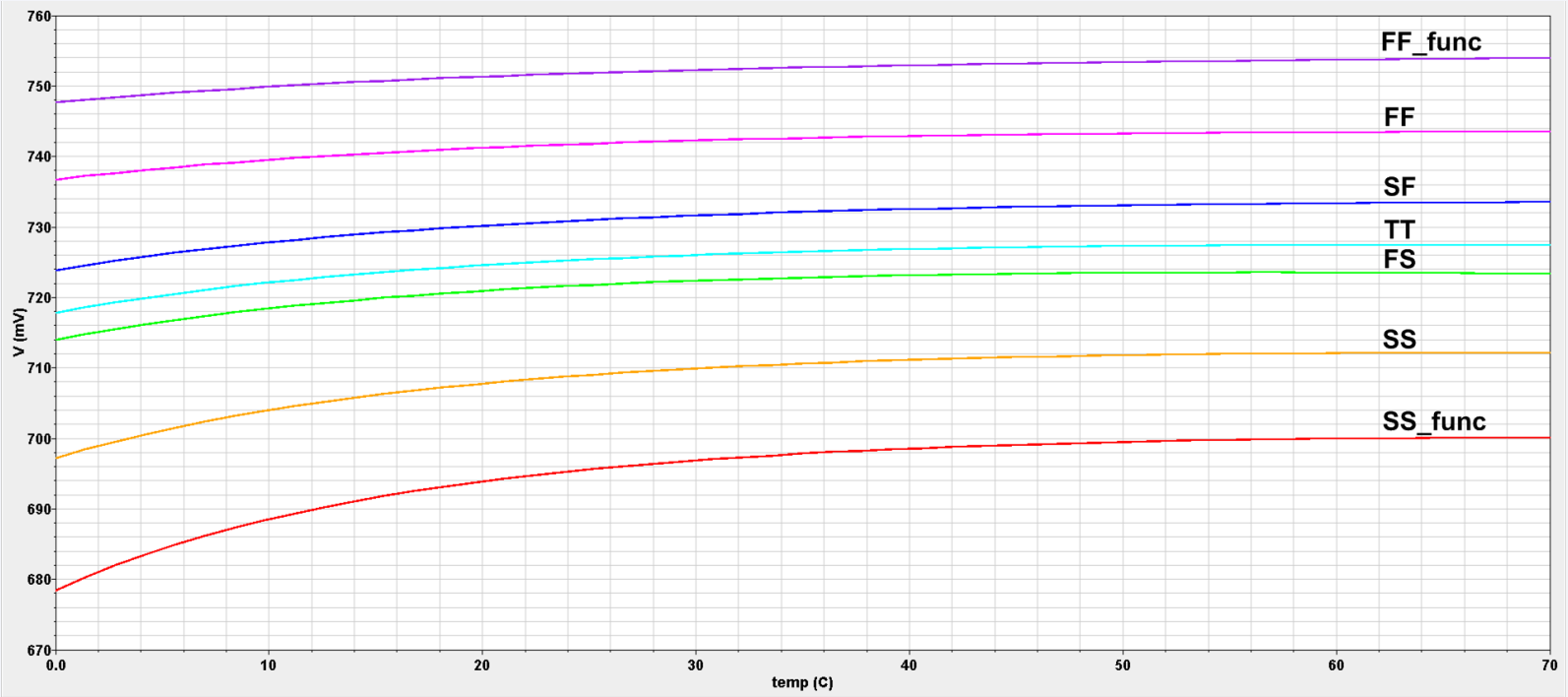
Using the BANDGAP register, it is configured for 1.2V operation (1001).
A temperature sweep between 0 and 70°C is performed.




Evolution with temperature is much worse than expected (50mV in 70°C)
Wrong simulation in temperature??

# Bandgap simulations

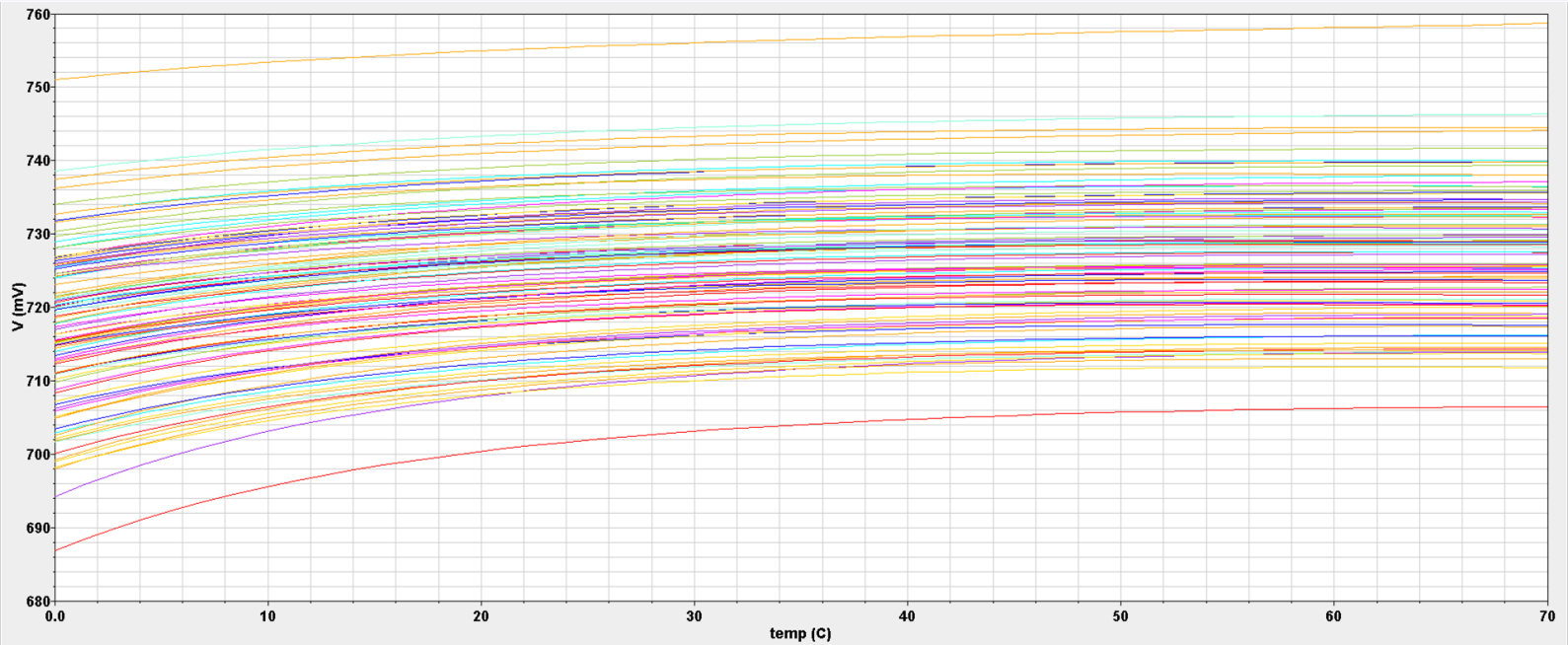
Corner simulations are repeated in the measurement range...




Again simulations are much better than measurements.

# Montecarlo simulations

Montecarlo simulations are also repeated...



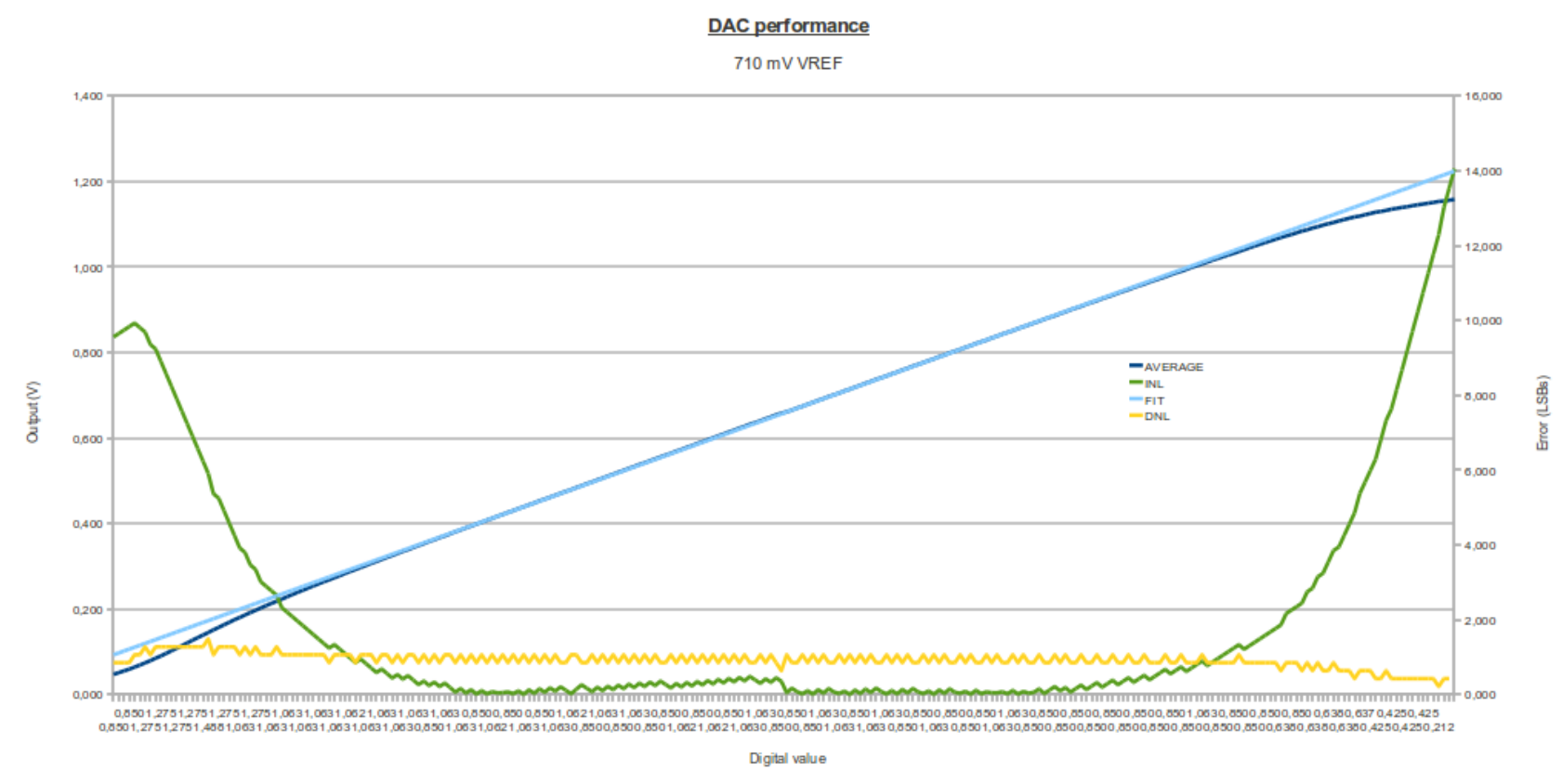

They are not worse than corners, and again simulations are much better than measurements.

# DAC performance

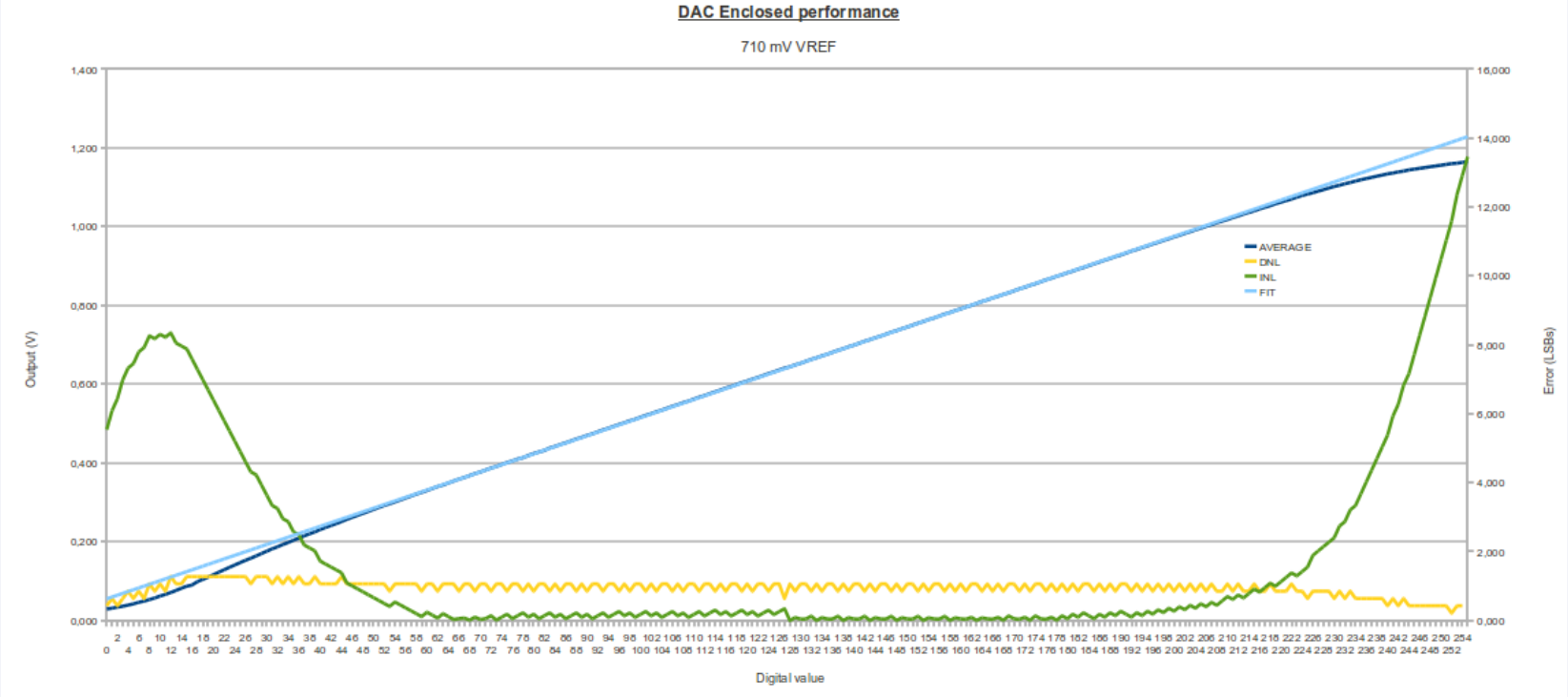
Using the DAC and DAC ENCLOSED registers a characterization of the blocs has been done (1.2V power supply).
Results are summarized in next table (using a LSB of 1,2V/255).

| | **DAC** | **DAC ENCLOSED** |
|---|---|---|
| Range | 300-970 mV | 300-970 mV |
| DNL | 1,06 LSBs | 1,06 LSBs |
| INL | 0,71 LSBs | 0,75 LSBs |

# DAC

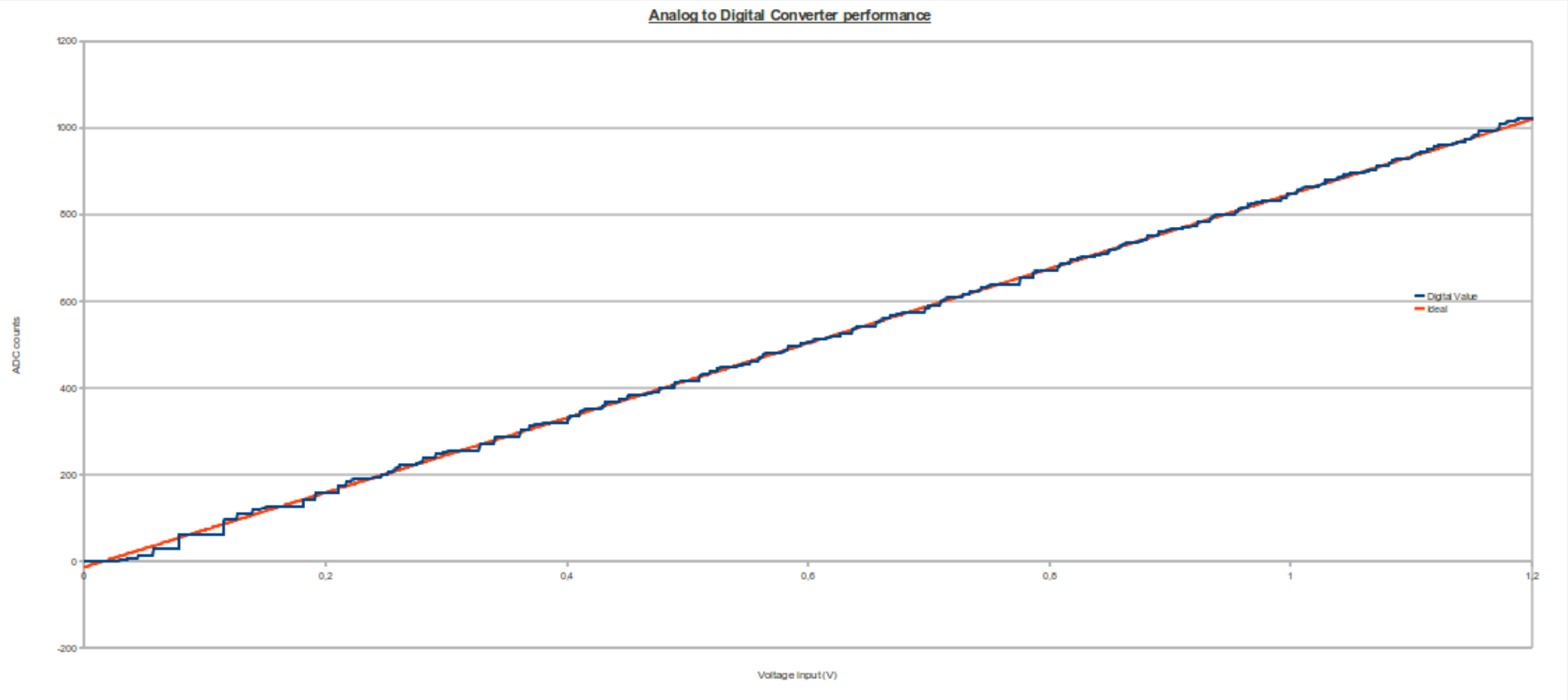

DAC performance
710 mV VREF
Output (V)
Error (LSBs)
Digital value
AVERAGE
INL
FIT
DNL
1,400
1,200
1,000
0,800
0,600
0,400
0,200
0,000
16,000
14,000
12,000
10,000
8,000
6,000
4,000
2,000
0,000

# DAC ENCLOSED



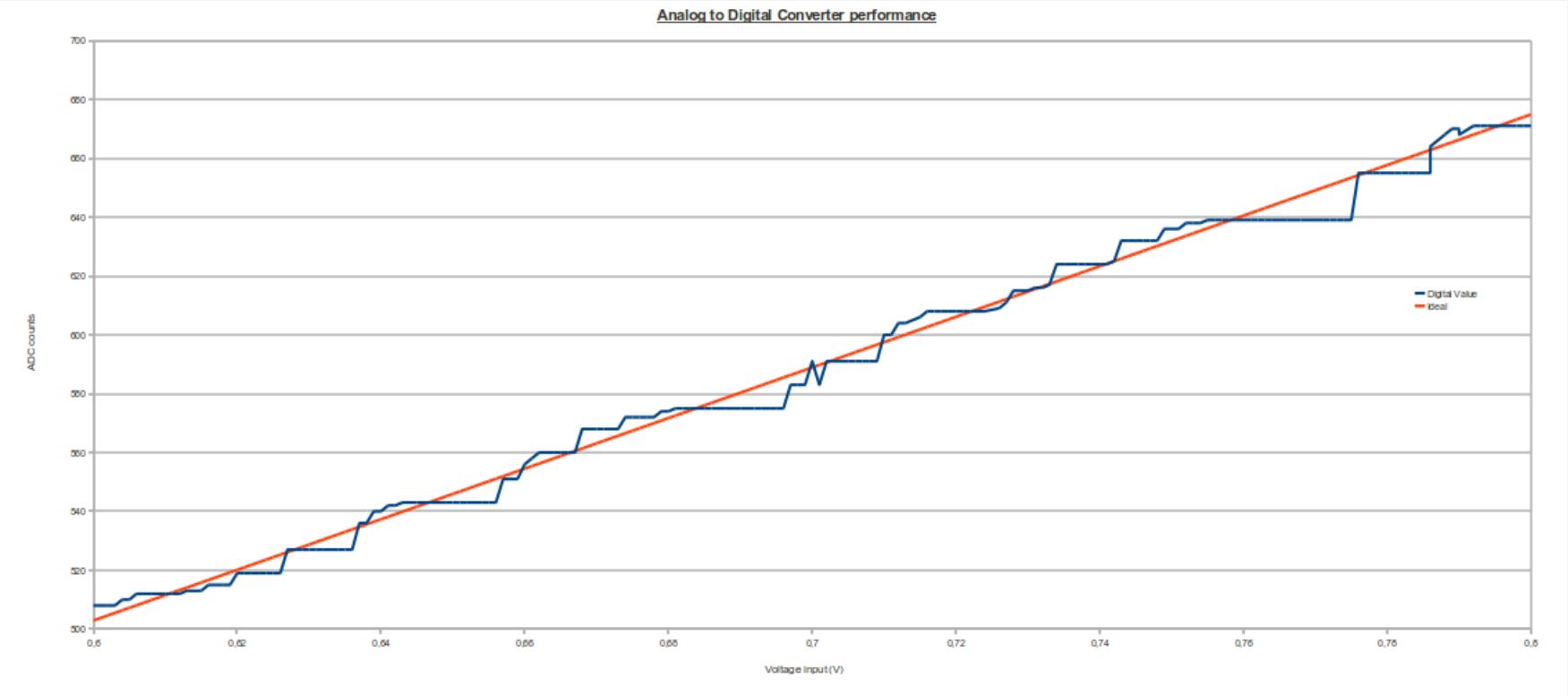
# ADC performance

Using the ADC register a characterization of the blocs has been done (1.2V power supply). Range is from 300 to 1200 mV. Internally it uses the same R2R DAC (10bits) + Amplifier.



# ADC

If we zoom in the ADC measurement, a better granularity input is needed for the characterization of the ADC.



# Conclusions

**What works:**

- ✓JTAG control and registers.
- ✓DAC.
- ✓DAC Enclosed.
- ✓Bandgap (at room temperature).
- ✓ADC (enclosed + digital control).

**What does not work or needs improvement:**

- ✗Output amplifier of DAC to increase usable range (better Rail-to-Rail).
- ✗Bandgap.

**What should be characterized:**

- Power consumption (all analog seems to consume less than 1 mA!).
- OTA.
- Characterization at 1V power supply.

# Next steps

Improvements;

- Finish tests.
- **Understand temperature simulation problems.**
- Redesign Bandgap circuit.
- Redesign amplifier to a full Rail-to-Rail one.

New blocks to design;

- Design of current output reference.
- Design of temperature sensor.
- Design of current mode DACs.
- Design of analog multiplexor for sharing ADC (8:1?).
- JTAG integration of all analog blocks control.