First Results of PXD6 Prototype Production

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for the HLL technology staff

Production status

First yield measurements

Discussion

Next steps

Production status

Reminder: PXD6 batch involved 10 wafer

In May the batch was split (4 + 6 wafer) for acceleration and to split the risk of the critical metallization steps

Status of the the first part:

- 2nd metal layer finished
- Yield measurements ongoing
- Lithography for backside back etching ongoing
- This week: first wafer ready for back etching (-> Laci)

Yield killer – shorts

Experiences from the first batch of PXD5

Valencia Feb. 2008

Poly bias resistor bus on Switcher pads

All Depfets can be switched off and

cleared by common Gate an Clear line, resp.

IV measurements on matrices

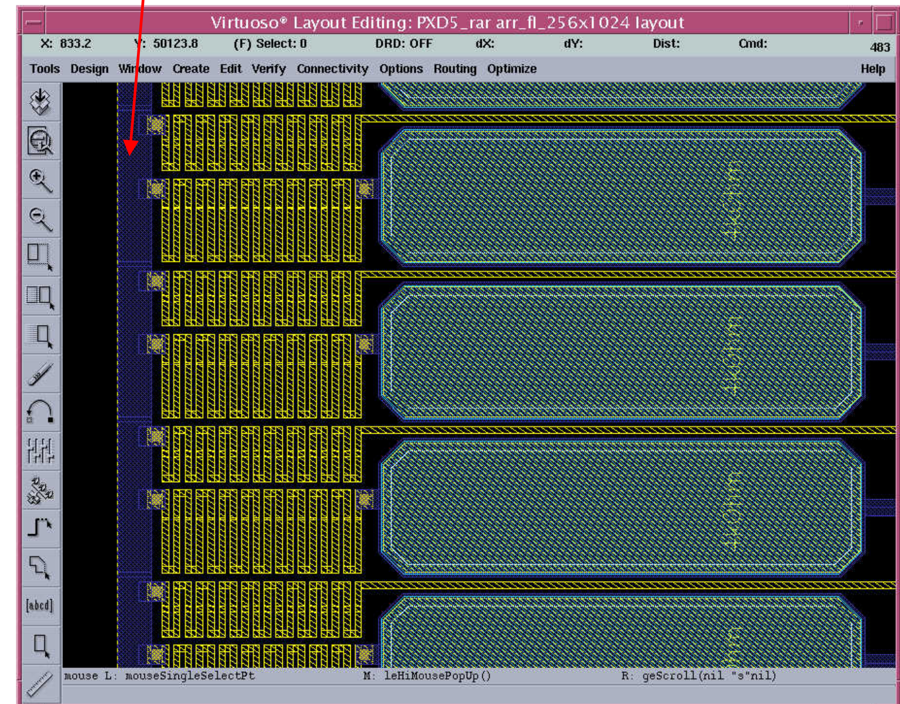
on wafer level are possible.

- leakage current
- diagnostics of failures
- individual DEPFET drain currents

Partially assembled matrices can be tested

common bias lines
for Gates and Clears

R_{Bias} = 20kOhm



What did we measure ?

Simple Short tests on matrices

1) all Gates vs bulk silicon (all Clears, all Drain, common Source)
2) all Clears vs all Drain and common Source (diodes)
3) all Gates vs common Cleargate
4) common Cleargate vs bulk silicon (all Clears, Drain, common Source)

All connected poly and metal lines are tested in parallel.

We cannot test:
A) shorts between Source and Drain
B) shorts between neighboring Drains (metal2)

Selection of chips for mounting and bonding

Process characterization

Evidence about yield for the final production

PXD6 Wafer
big chips up to 5cm²

X: 74000 Y: 78000 (F) Select: 0 DRD: OFF dX: dY: Dist: Cmd: 2

Tools Design Window Create Edit Verify Connectivity Options Routing Help

[abcd]

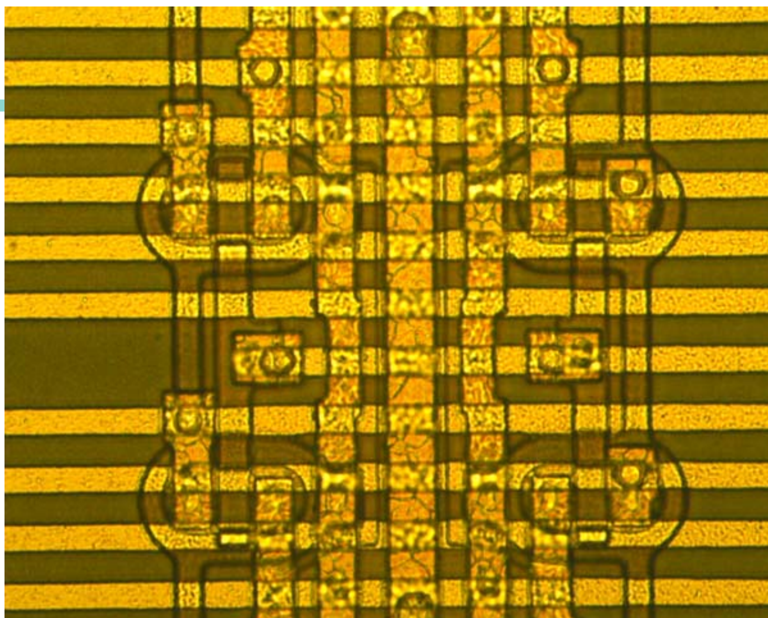
mouse L: mouseSingleSelectPt M: leHiMousePopUp() R:hiZoomAbsoluteScale(hiGetCurrentWin

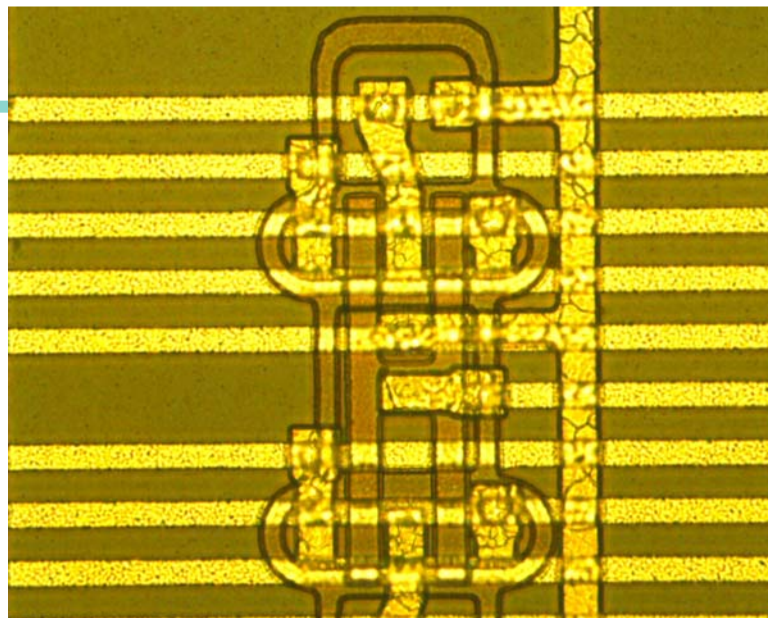
hll>

About
100 matrices

4 basic design
options
(+ derivates)

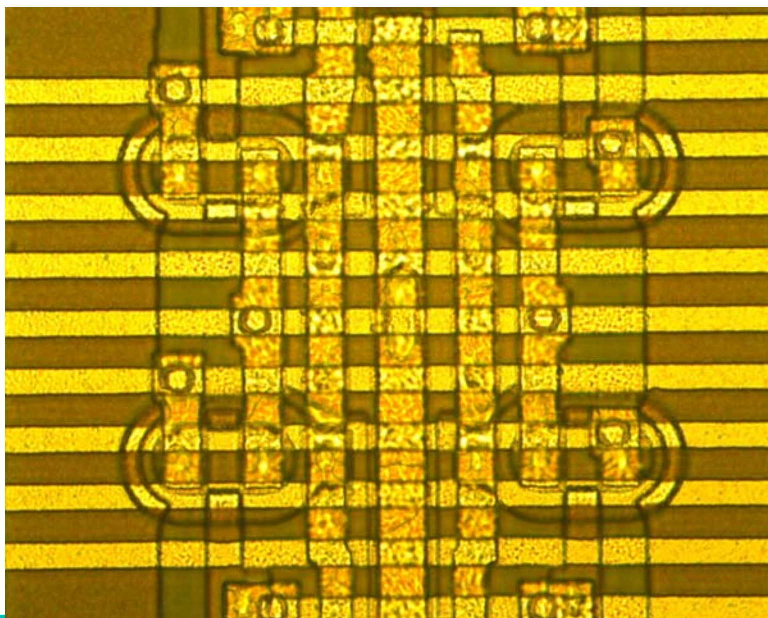
I00

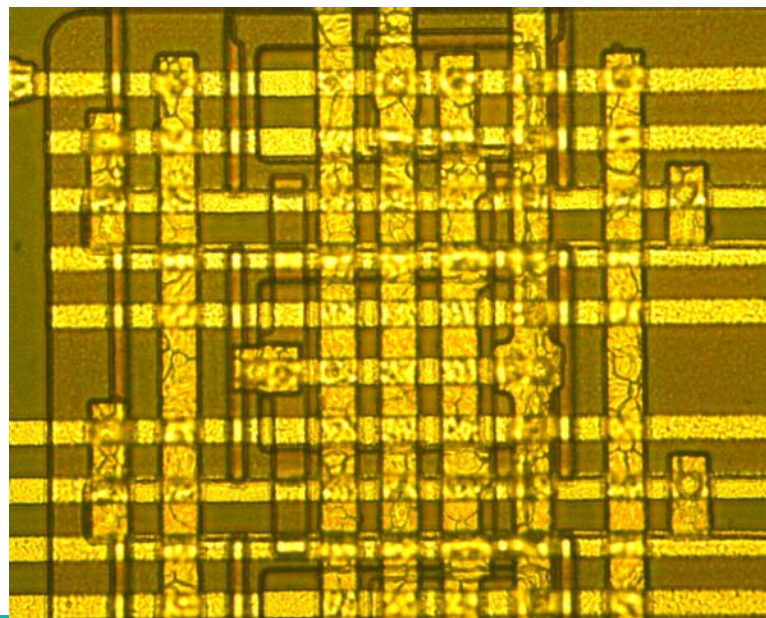




I06

J00





J06

Wafer #2 – Test1 (Gate vs Si)

1. Gate vs 1. Clear + 10V

			0	1	2	3	4	5	6	7	8	9	10			
A							0,8	###	0,27	0,01	0,29					
B					0,4	0,41	0,57	0,9	0	0,42	0	0,27				
C					0,47	0,51	0,57	0	0,46	0	0	0,19				
D						0,33	23000	0	0	0,14	0,17					
E					0,27	0	27000	0	0	0,16	0,17		0			
F						0,2	0,36	0,63	0,22	0,16	0,17					
G					0,26	0,28	0,26	0,34	0	0	0		0,23			
H					1000000	###	1000000			0,08	1000000	0,83				
I								5,2							1000000	
J								1000000						6,7		
K				0,15	0,15		0	0,12	0,22	0,17		0,16	0,13			
L							0	0,13	1000000	0,11						
M					0		0	0,09	1000000	0,13			0,17			
N							0	0	0,15	0						
O					0,12		0	0,13	0,16	0			0,14			
P							0	0	0,1	0,13						
Q							0,09	0	0,14	0,11						
R							0,13	0,13	0,17	0,58						

Wafer #2 – Test2 (Clear vs Source)

1. Clear vs Source

I/nA bei 20V

	0	1	2	3	4	5	6	7	8	9	10		
A					0,67	2,1	1	0,75	0,75				
B			1,15	0,75	2,2	4,1	1,45	1,75	1,8	0,78			
C			1,15	1,15	1,3	###	1,15	2,7	2	0,8			
D				0,82	0,92	###	2,4	0,75	0,84				
E			1,03	1,9	0,6	###	2,5	0,9	0,9		0		
F				0,8	1,2	2,3	0,77	0,77	0,83				
G			0,8	1,05	0,83	6	1,9	2,8	3		0,95		
H			1000000	###	2,3			1000000	1000000	###			
I						32							1000000
J						1000000						22	
K		1	0,77		1,75	0,78	1,15	1,07		0,8	0,67		
L					2800000	0,77	0,75	0,7					
M			0		700000	0,72	0,75	0,87			1,05		
N					1000000	1,4	0,74	1,7					
O			0,73		1000000	0,85	1,1	1,8			0,94		
P					1,7	###	0,74	1,05					
Q					0,73	1	1,05	1,05					
R					1,1	0,85	2	0,77					

Wafer #2 – Test3 (Gate vs ClearGate)

ClG vs Gate (with light) — I/nA bei +10V

			0	1	2	3	4	5	6	7	8	9	10			
A							0,02	0,03	0,03	0,02	0,03					
B					0,04	0,03	0,15	0,03	0	0,14	0	0,03				
C					0,02	0,05	0,05	0,03	0,05	1000000	1000000	0				
D						0,03	0,02	0,03	0,05	0,03	0,05					
E					0,04	0	0,02	0,04	1000000	0,02	0,02		0			
F						0,03	0,06	0,02	0,04	0,03	0,02					
G					0,03	0,04	0,03	0,03	0	1000000	1000000		1000000			
H					0,04	0,04	0,05			0,02	0,03	0,03				
I								1,4							1000000	
J								1000000						1000000		
K				0,02	0,03		0,01	0,02	0,03	0,03		0,02	0,03			
L							0,02	0,01	0,02	0,01						
M					0,1		0,03	0,01	0,02	0,01			0,03			
N							0,03	0,02	0,02	1000000						
O					0,02		0,03	0,03	0,02	0,01			0,02			
P							0	0,03	0,02	0,03						
Q							0,01	0	0,03	0,03						
R							0,02	0,03	0,1	0,02						

Wafer #2 – Test4 (ClearGate vs Si)

All_Clear vs ClG (with light) I/nA bei +15V

	0	1	2	3	4	5	6	7	8	9	10			
A					0,04	0,05	0,07	0,03	0,06					
B			0,06	0,06	1000000	0,06	0	1000000	0	0,04				
C			0,06	0,06	0,06	0,04	0,08	1000000	1000000	0				
D				0,05	0,03	0,05	1000000	0,02	1000000					
E			0,06	0	0,03	0,05	1000000	0,03	0,03		0			
F				0,05	0,06	0,04	0,06	0,03	0,03					
G			0,06	0,06	0,04	0,06	0	1000000	1000000		0,13			
H			0,08	0,08	0,07			0,04	0,08	0,04				
I						2,3							1000000	
J						1000000						5,75		
K		0,05	0,03		0	0,04	0,06	0,06		0,05	0,05			
L					0,05	0,02	0,03	0,02						
M			0		0,05	0,02	0,03	0,02			0,05			
N					0,05	0,02	0,04	1000000						
O			0,03		0,04	0,05	0,05	0			0,04			
P					0	0,05	0,03	0,05						
Q					0,03	0	0,06	0,04						
R					0,05	0,05	1000000	0,03						

Wafer #2 - all Tests

Bad / Good - Overview

			0	1	2	3	4	5	6	7	8	9	10			
A							G	B	G	G	G					
B					G	G	B	G	G	B	G	G				
C					G	G	G	B	G	B	B	G				
D						G	B	B	B	G	B					
E				G		G	B	B	B	G	G	G				
F						G	G	G	G	G	G					
G				G		G	G	G	G	B	B	B				
H					B	B	B			B	B	B				
I		G							B							
J			B						B							
K				G	G		G	G	G	G		G	G			
L							B	G	B	G						
M				G			B	G	B	G		G				
N							B	G	G	B						
O				G			B	G	G	G		G				
P							G	B	G	G						
Q							G	G	G	G						
R							G	G	B	G						

Measurement status

Full scan (test 1 – 4) over 2(4) wafers

Big chips are tested on all wafer

Yield (big chips): 1 of 16

Yield (small chips): about 80%

We found some design bugs in small chips

- 2 bugs are corrected in metal 2
- 1 bug has to be corrected in metal 1 (2nd batch)

Possible reasons – next steps

- Photo litho problem during contact openings
- Insufficient Metal etching
- Shorts in the interdielectrics, for instance metal 1 / metal 2 (hillocks)
- Damage during processing (external ion implantation source)

- Up to now coarse measurements to get the overview
- Failure analysis starts next week

2nd Part of the batch (6 wafer)

- new equipment: automatic inspection microscope, - > wafer to wafer inspection

allows inspection of the contact layer before we start (time 3 …4 month)

Future productions

- all implanations will be done inhouse
- use of automatic inspection microscope

J06 –ILC like (most aggressive design)

IOO first contact openings

Damage during external implantation

W11
Chip I00

Failed Test 4

CLG vs Si