Status of ATCA based Back-End readout for PXD Detector

Zhen-An LIU

IHEP Beijing

30 Sep. 2010

Many Thanks to Christian and Carlos for their kind invitation to this DEPFET collaboration and the nice city Valencia!

Outline

- Application information for DEPFET membership
  - Triglab members
  - Projects completed
    - L3Cosmic
    - BESIII trigger system
  - Projects now involving
    - Computer node development for PANDA/GSI
    - Belle2Link for Belle II experiment at KEK
    - Control system/LLRF for CSNS
- Status for PXD back-End readout
  - Structure of PXD readout
  - Modification ongoing
- Summary

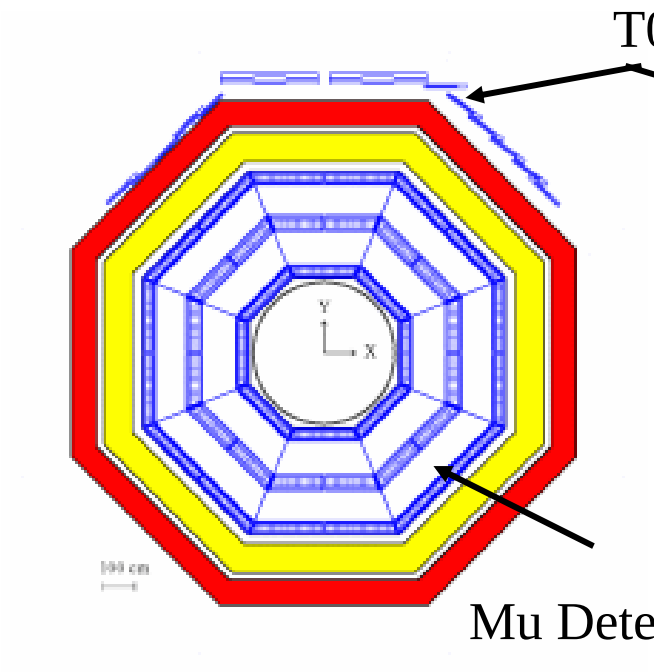
Application information for DEPFET membership

- Trigger Laboratory (15)

  A physics oriented, FEE, BEE, Trigger, DAQ
- Staff (10)
  - Zhen-An Liu, Prof. (Head, BESIII, PANDA, BelleII)
  - Dapeng Jin, Associate Prof. (CSNS/Control)
  - Hao Xu, Senior Engineer (PANDA/PXD,)
  - Ke Wang, Senior Engineer (ASIC)
  - Wenxuan Gong, Engineer (BESIII)
  - Jie Huang, Technician (assistance)
  - Jiajie Li, Technician (CSNS/Control)
  - Yali Liu, Technician (CSNS/Control)
  - Lei Hu, Technician (CSNS/Control)
- Students(5)
  - Qiang Wang (PhD, PANDA)
  - Dehui Sun (PhD, Belle II/Belle2Link)
  - Jingzhou Zhao (PhD, Belle II/PXD)
  - Haichuan Lin (MS, XTCA)
  - Liuqian Liu (MS, CSNS/Control)

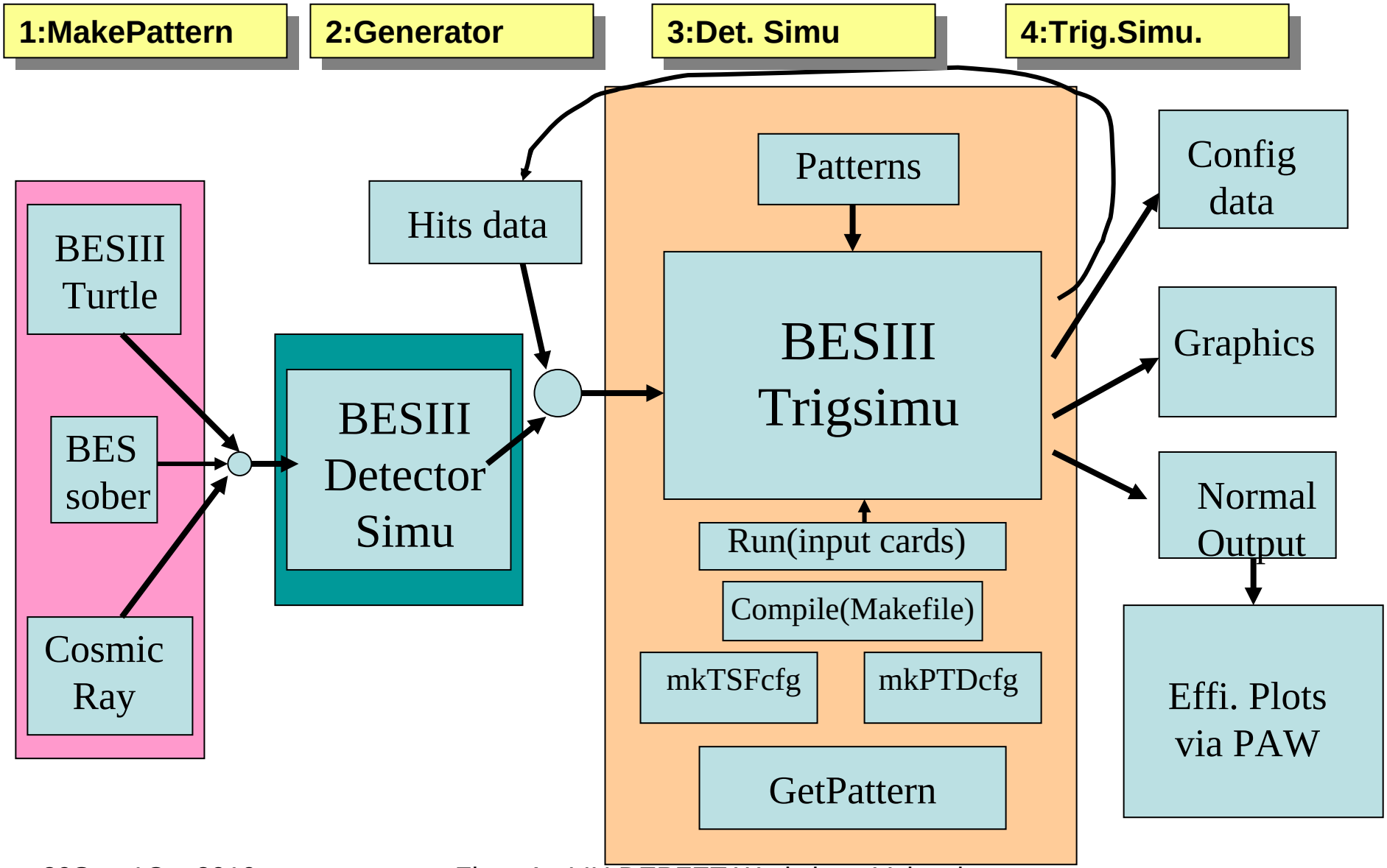
Projects completed: L3+COSMIC at L3/LEP(1997-2001)

- Setup of Quality control system of T0 detector
- Quality control in T0 Production in Beijing



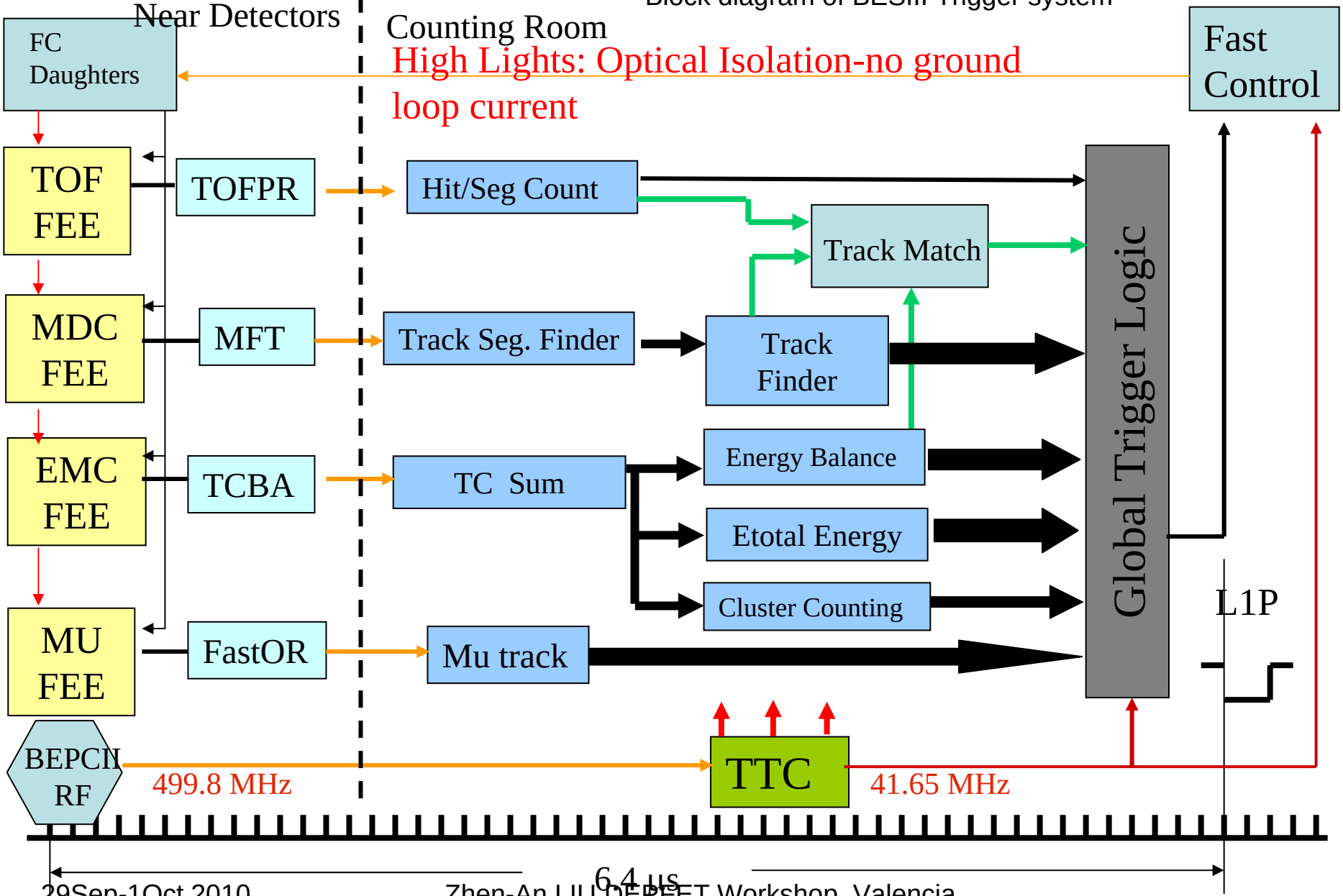
Projects completed: Trigger System of BESIII(2002-2007)

Conception Design, simulation, Technical design, Hardware Implementation, Installation, Commission



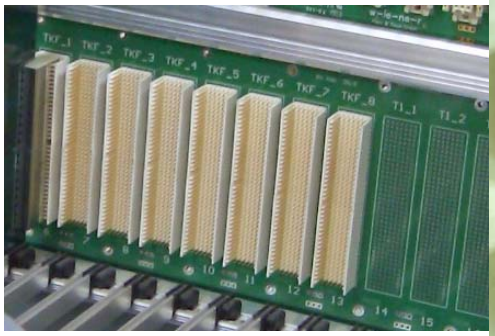
Projects completed: Trigger System of BESIII(2002-2007)

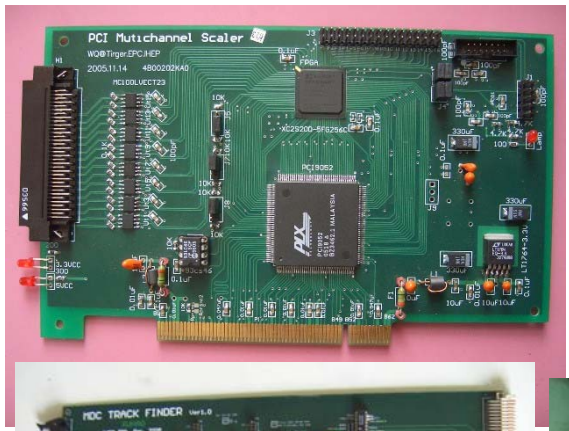
- Block diagram of BESIII Trigger system

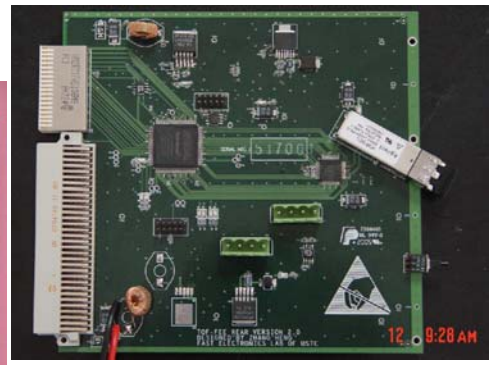


Implementation

- Based on FPGA
- Electrical Isolation via Optical fiber
- High Speed transmission via RocketIO
- Reconfiguration(onboard, panel, system)
- Total of 27(21 hardware) home designed

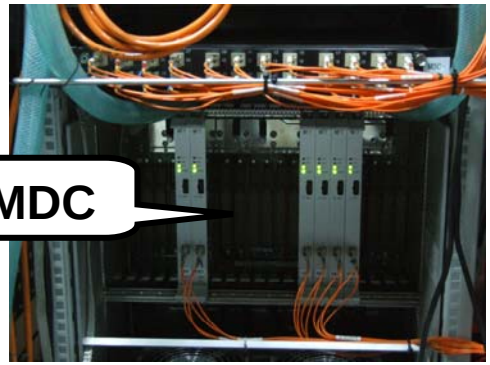


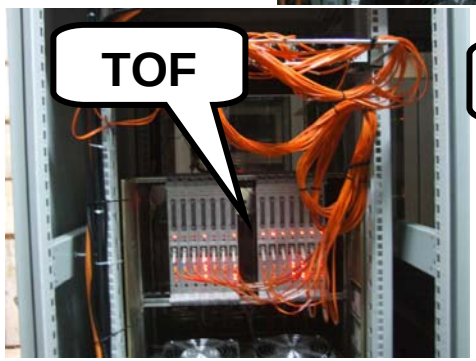


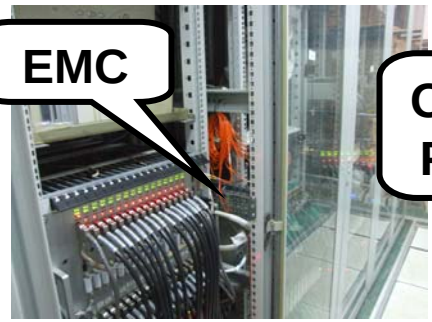


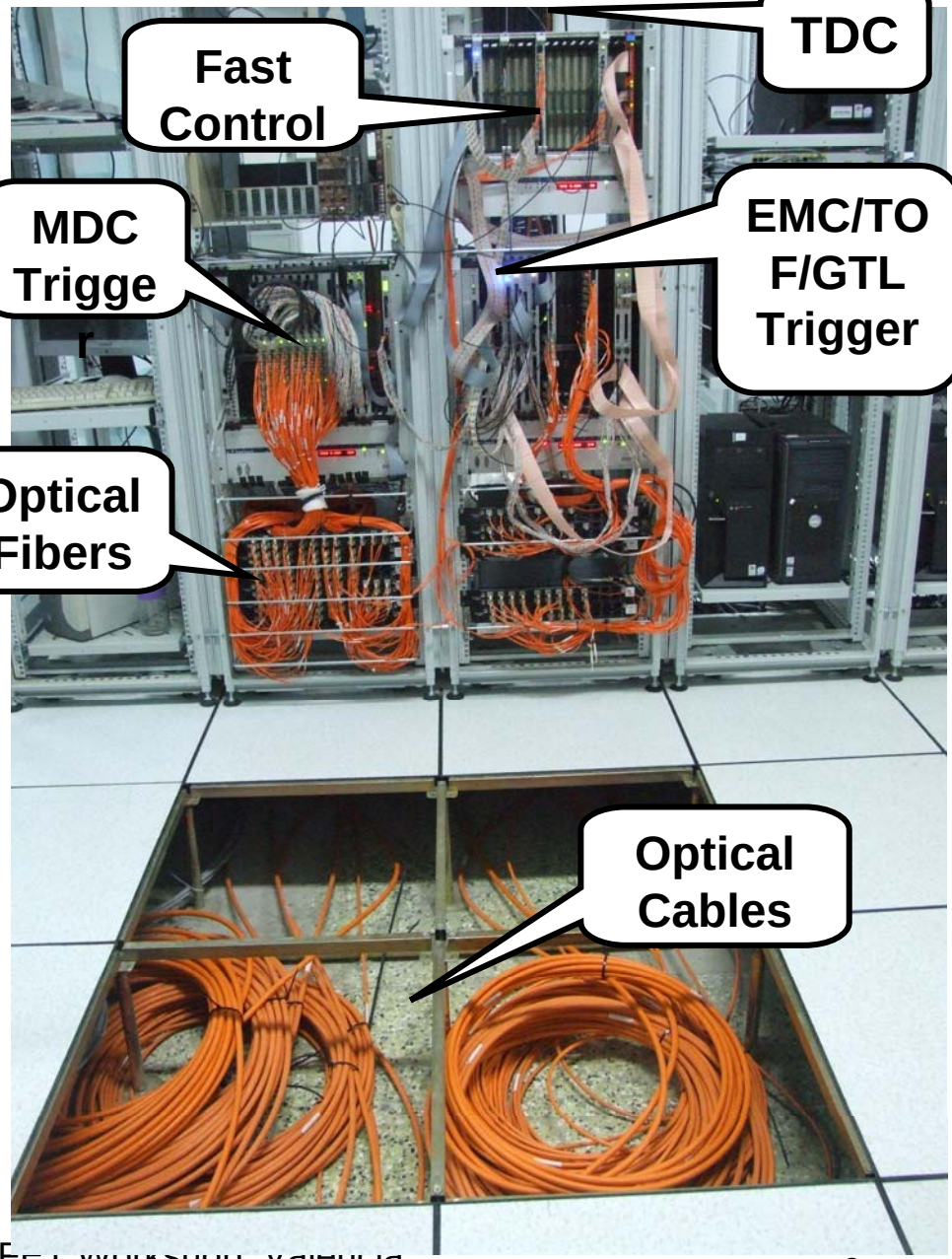
Installation/commission 2007

1.75Gbps/fiber,205Gbps synchronized



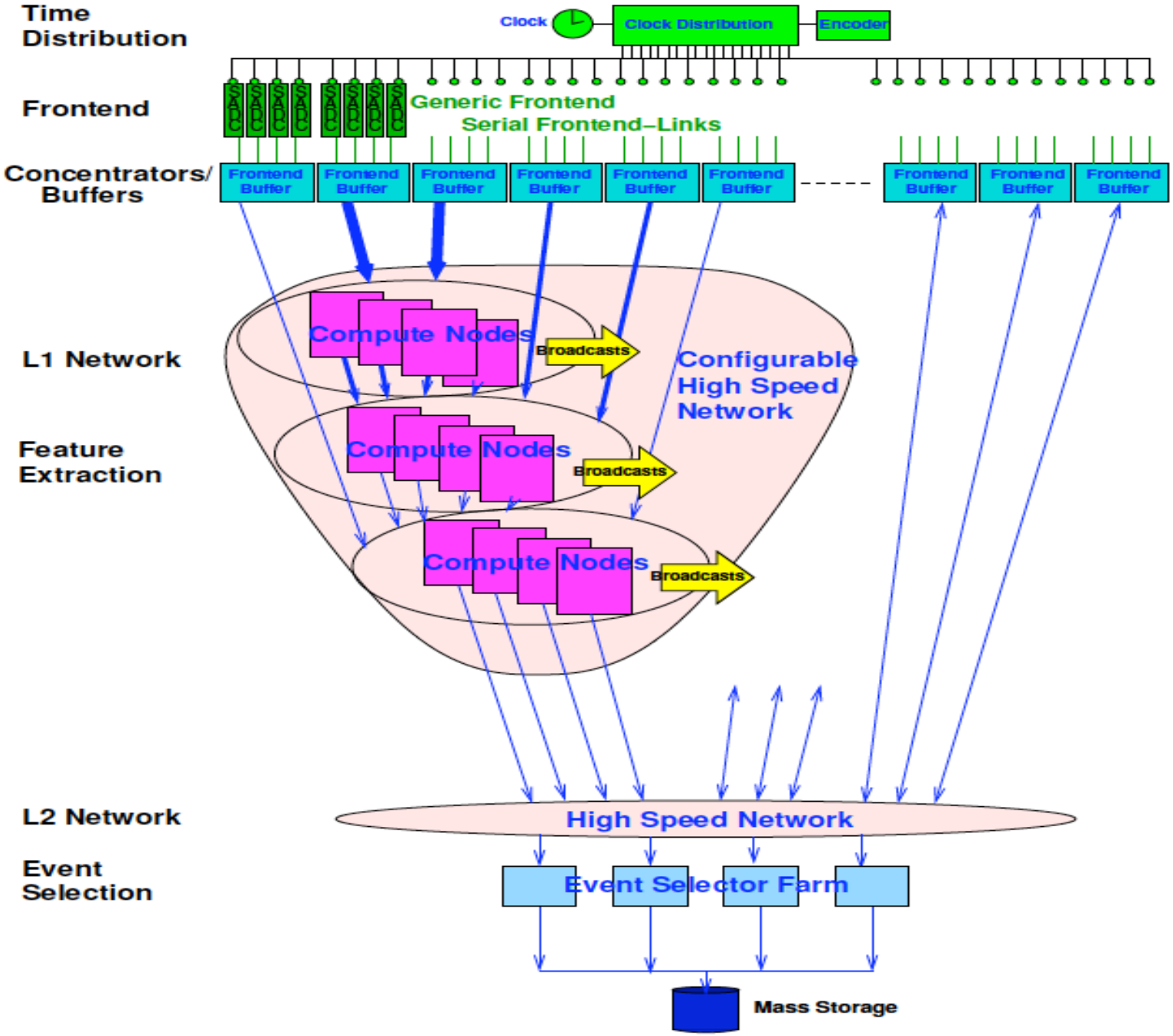






Projects now undergoing: **1.PANDA**

- **Requirements for PANDA DAQ**
  - Interaction rates up to 30MHz
  - typical event sizes 4 - 20 kB.
  - data rates after front end preprocessing: 40GB/s - 200 GB/s
  - high flexibility and selectivity
  - Solution:
    - continuously sampling data acquisition
      - No „hardware triggers“
      - Precision clock distribution system
      - Digital signal processing at FrontEnd level
    - Event selection in programmable processing units
    - Connection via high speed networks

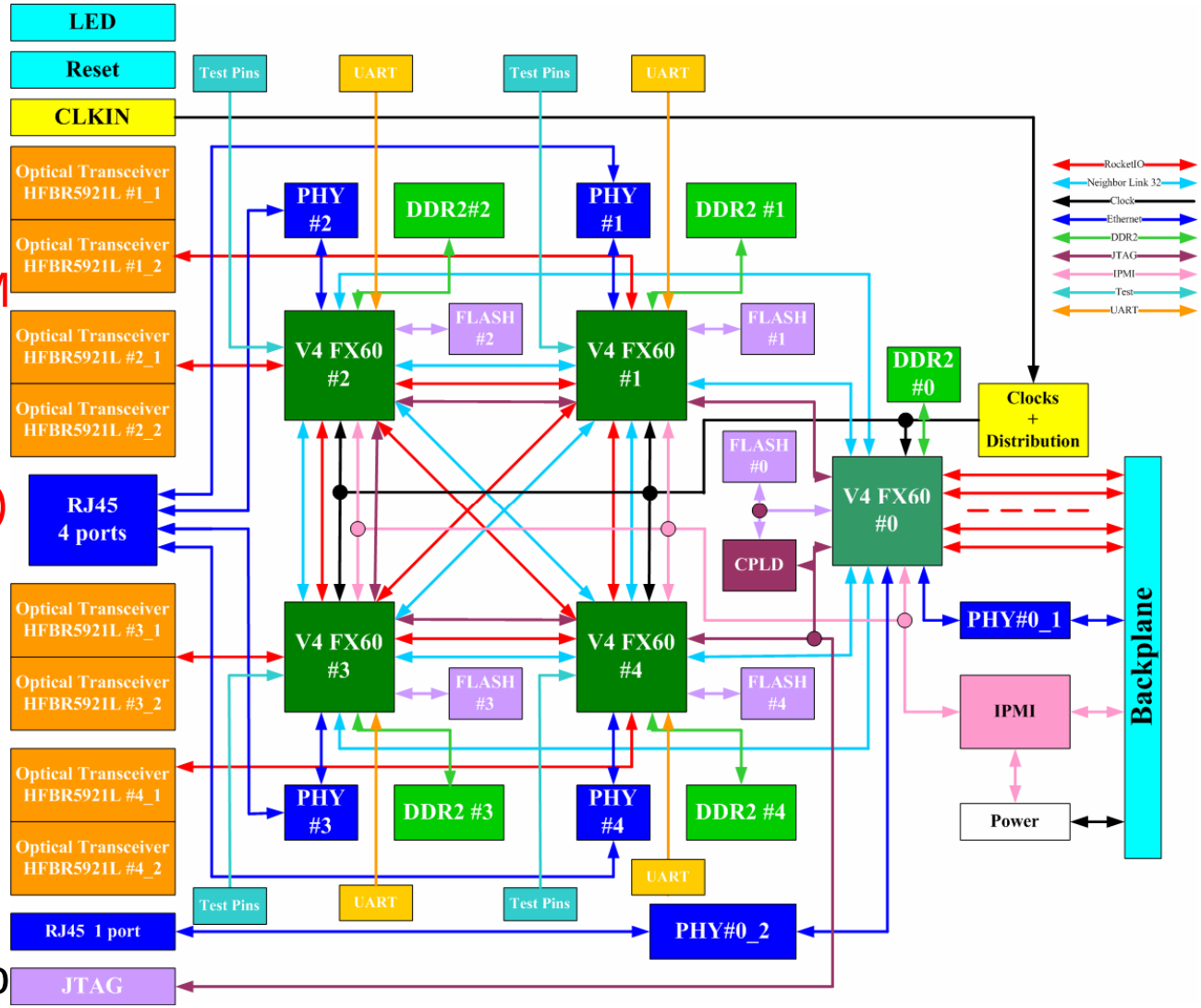

Time Distribution
Clock
Clock Distribution
Encoder
Frontend
Generic Frontend
Serial Frontend–Links
Concentrators/ Buffers
Frontend Buffer
L1 Network
Compute Nodes
Broadcasts
Configurable High Speed Network
Feature Extraction
Compute Nodes
Broadcasts
Compute Nodes
Broadcasts
L2 Network
High Speed Network
Event Selection
Event Selector Farm
Mass Storage

General Purpose FPGA Compute Node

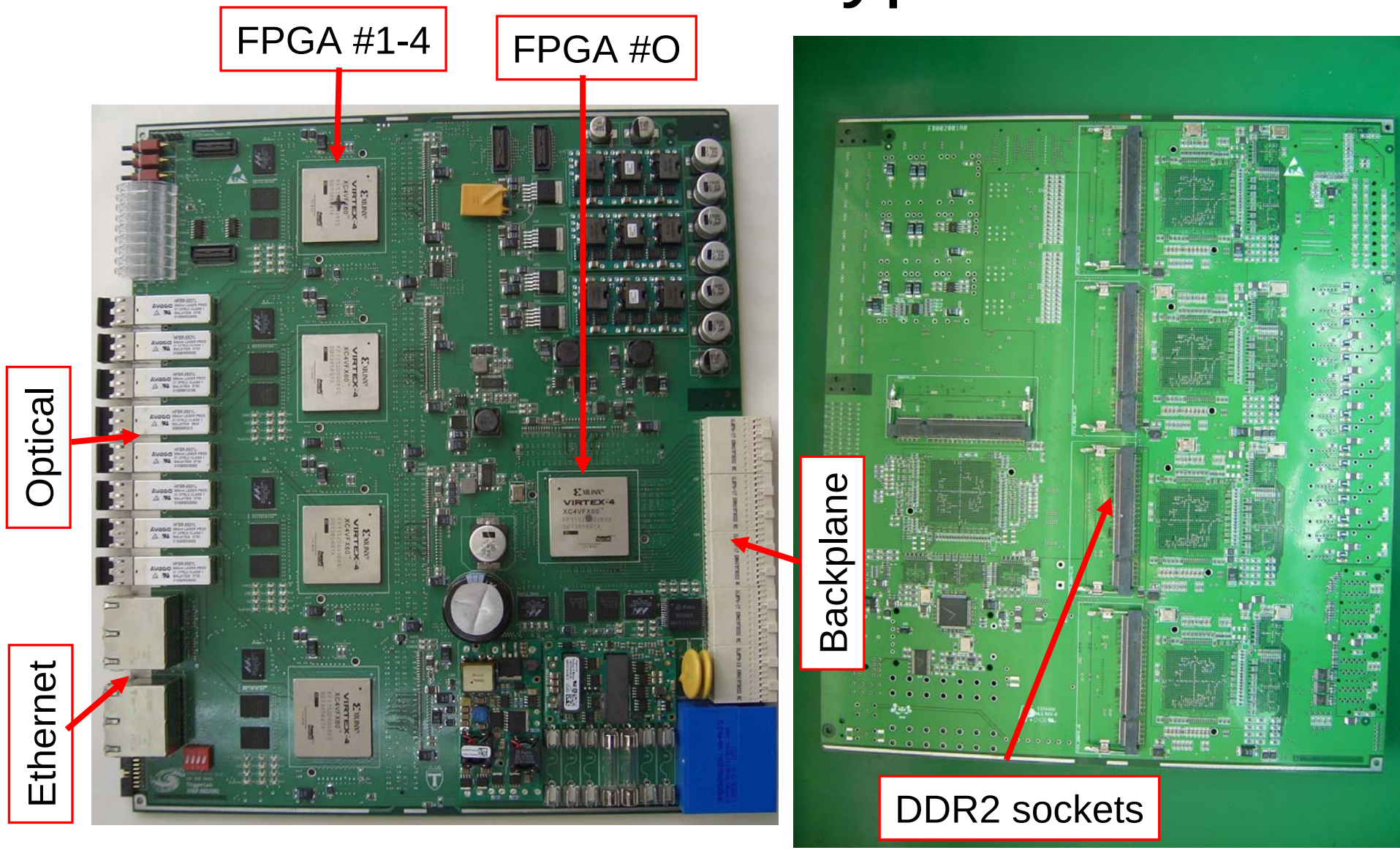
- Build a common platform : Compute Node
  - Highly scalable to adapt to different performance and bandwidth requirements
- Computing resources via FPGA: XILINX Virtex 4 FX 60
- Lots of buffer memory
- Flexible I/O connectivity
  - GBit Ethernet
  - Optical links via MGT (RocketIO)
- High performance backplane interconnection (no VME !)
  - Advance Telecommunication Computer Architecture
    - ATCA full mesh backplane

Architecture and features of CN

- High Performance Compute Power/resources:
  - 5 Virtex-4 FX60 FPGA
  - 10Gb DDR2 RAM (2G/FPGA)
- ~32Gbps Bandwidth
  - 8x panel Optical Link(3Gbps each)
  - 13x RocketIO to backplane
  - 5x Gigabit Ethernet
  - 1x GBit Ethernet to backplane
- 2 Embedded PowerPC in each FPGA for slow contro
  - Real time Linux
- ATCA compliant

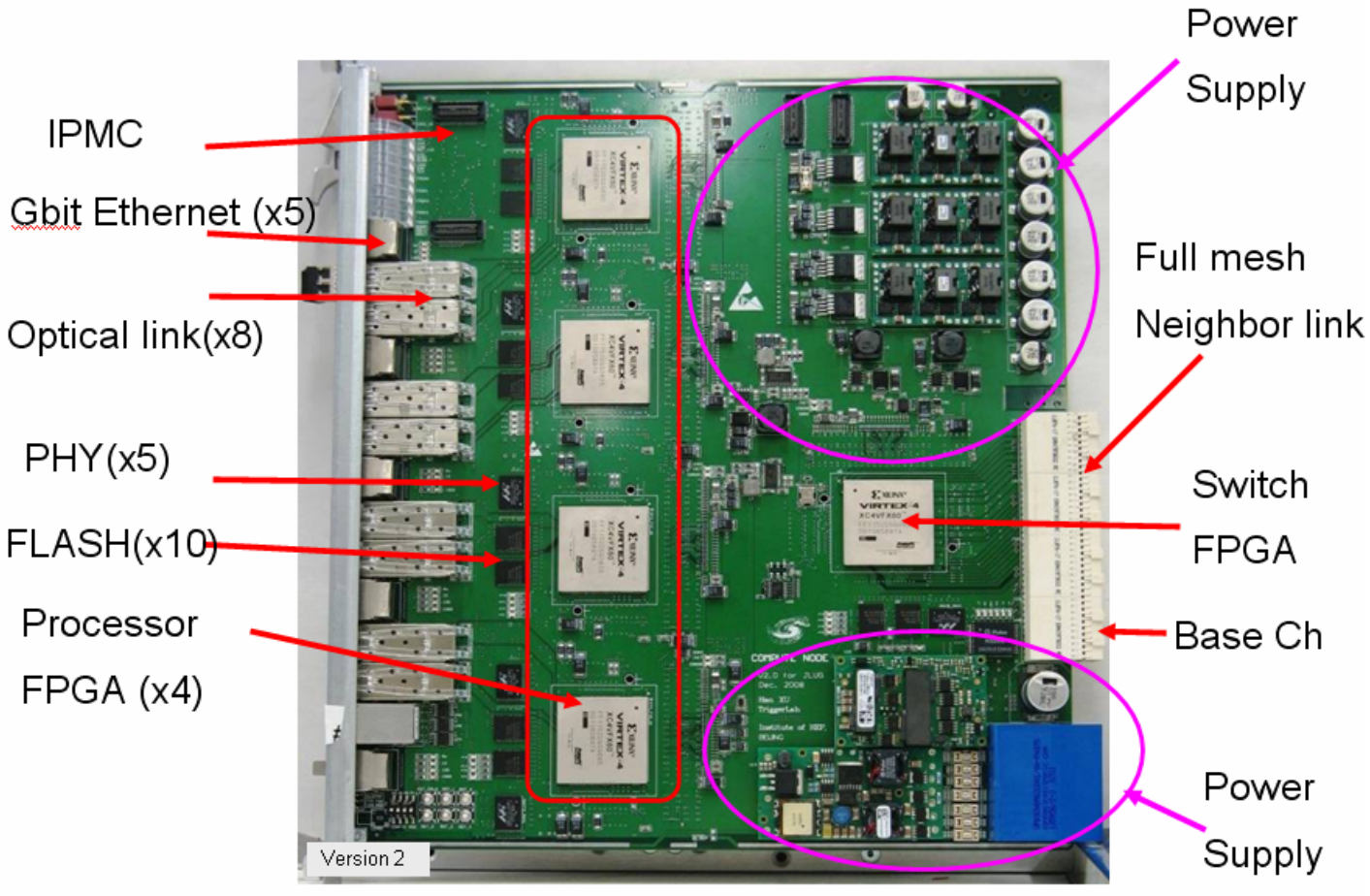


First Prototype



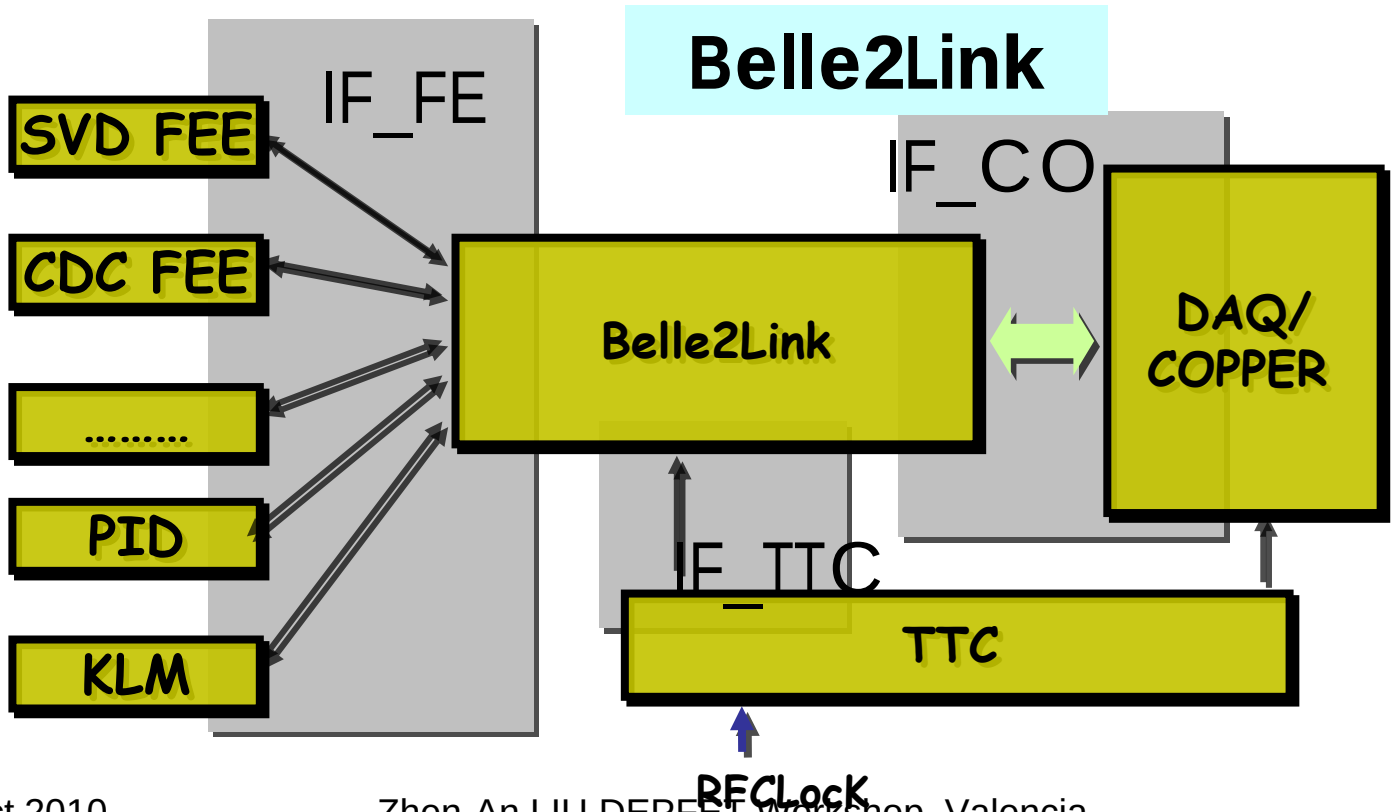
2nd version prototype

- SFP pluggable
- Mono RJ45 socket
- Higher bandwidth /SFP+
- Front Pannel
- Better LEDs



Projects now undergoing: **2.Belle2Link**

- Unification of High Speed data collection and transmission to COPPER board based on FPGA and RocketIO
- Discussion since 2007
- Decided in Nov 2009



Prototypes

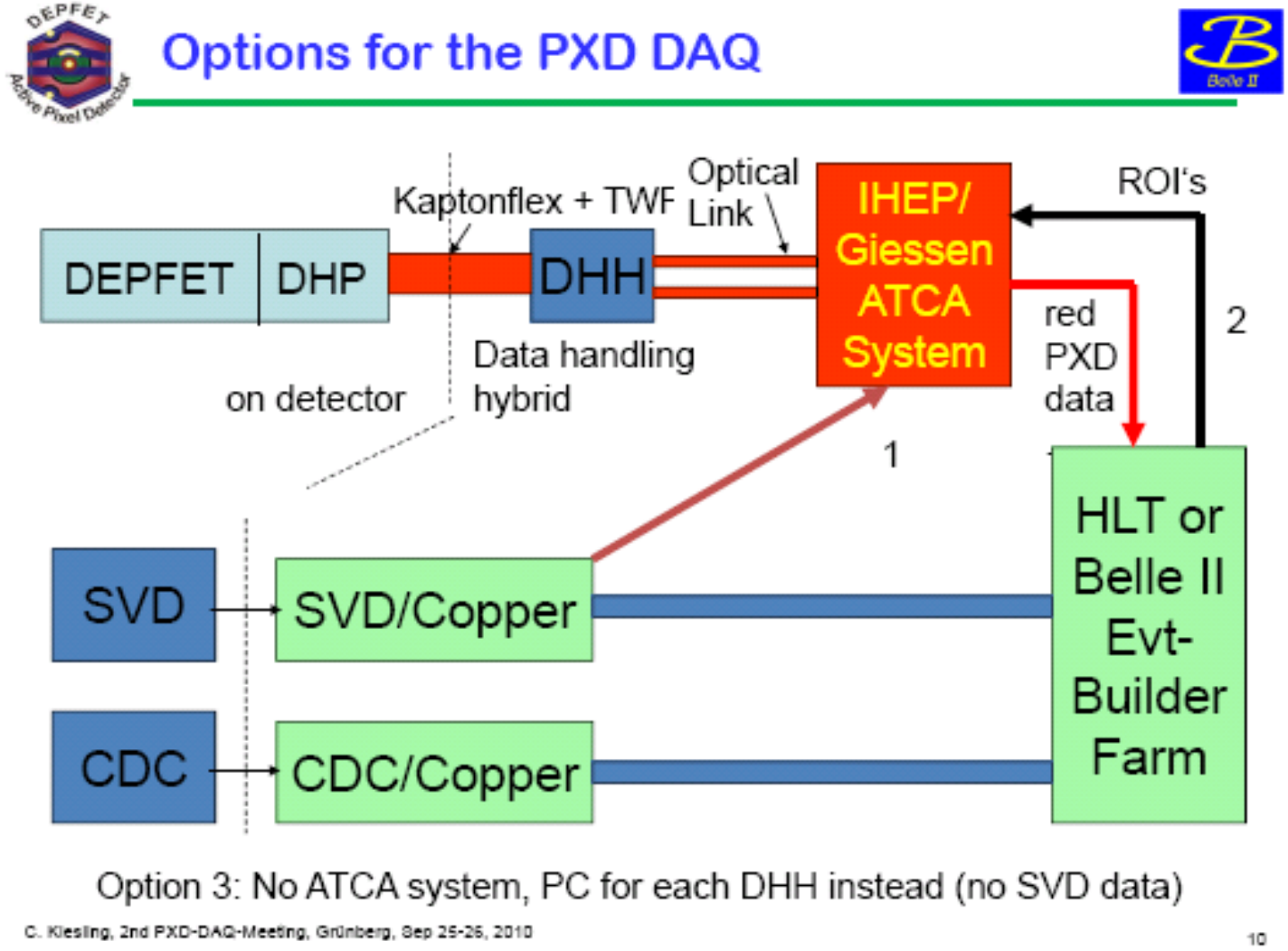
- Responsibility
  - System wide consideration including protocol
  - Prototyping including firmware for reading, transmission and merging,…
  - Testing and commissioning

Belle2Link Summary

- Hardware design of Belle2Link successful
- Firmware/protocol of Belle2Link is coded and works
- Mini DAQ has been setup and works at IHEP
- TDR of Belle2Link is included
- Joint test with CDC Prototype was successful July at KEK

Development for PXD back-End readout

- Structure of PXD readout



Requirements to CN by PXD

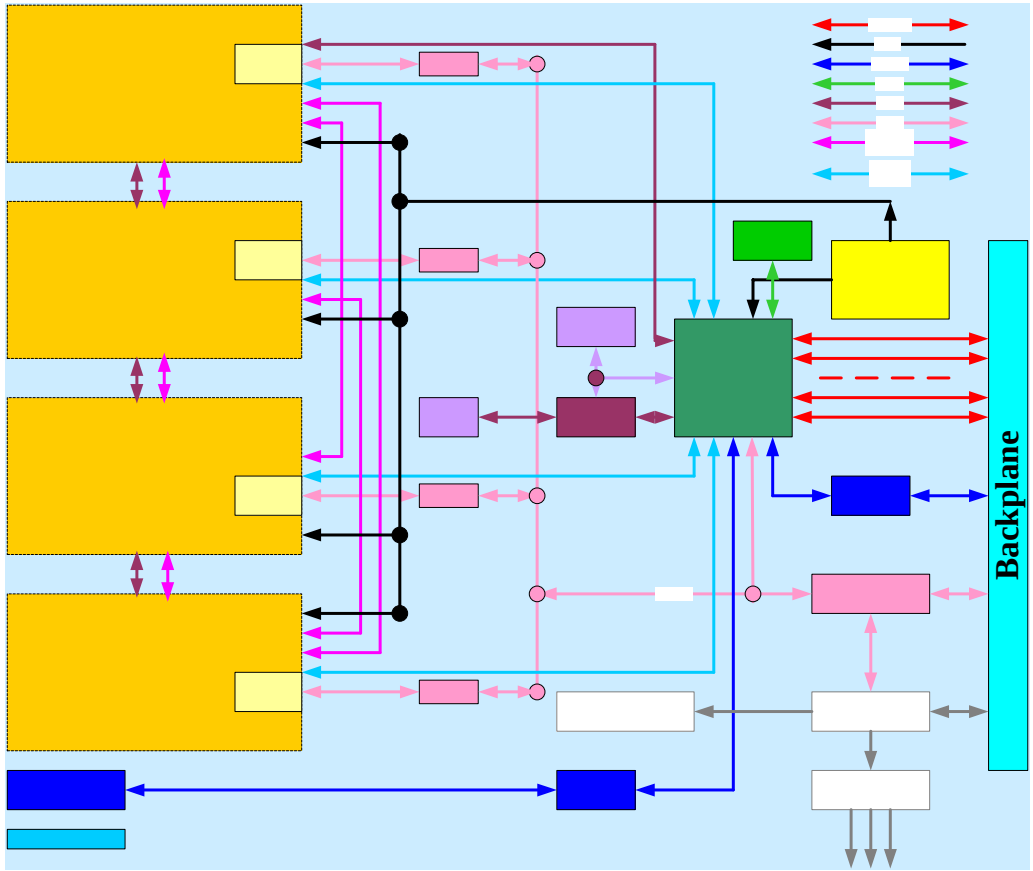
- DDR memory 4G/FPGA(20G/CN)
- 6 Gbps/FPGA

New version agreed in Gruenberg workshop

- Which Platform ---------→Carrier/AMC
  - ATCA or XTCA
  - ATCA or ATCA Carrier + AMC
- 3.125Gbps/ch or 6.25Gbps/ch -→ 2x3Gbps
  - 6G/FPGA
  - 2 X 3Gbps/link
- DDR2 or DDR3 or DDR4, or …… → 2X DDR2
- V4 or V5 or V6 or SP6? -------→ V5
- Memory 4G/FPGA(total of 20Gb)->4(20)G
- Clocks and controls ---- Yes

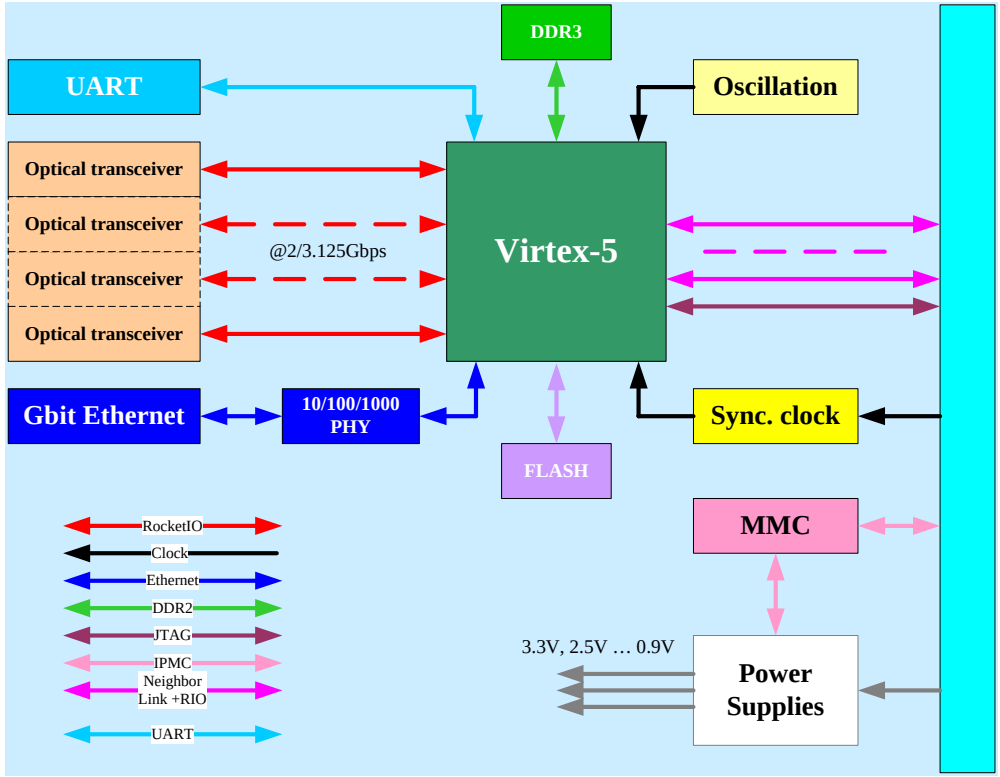
Modification ongoing -Motherboard/Carrier Board

- 4 AMC connectors
- FPGA0 for interconnections in XTCA
  - V4
- IPMC routing
- Clock/trigger/ distributions
- Power conversions
- RTM reservation



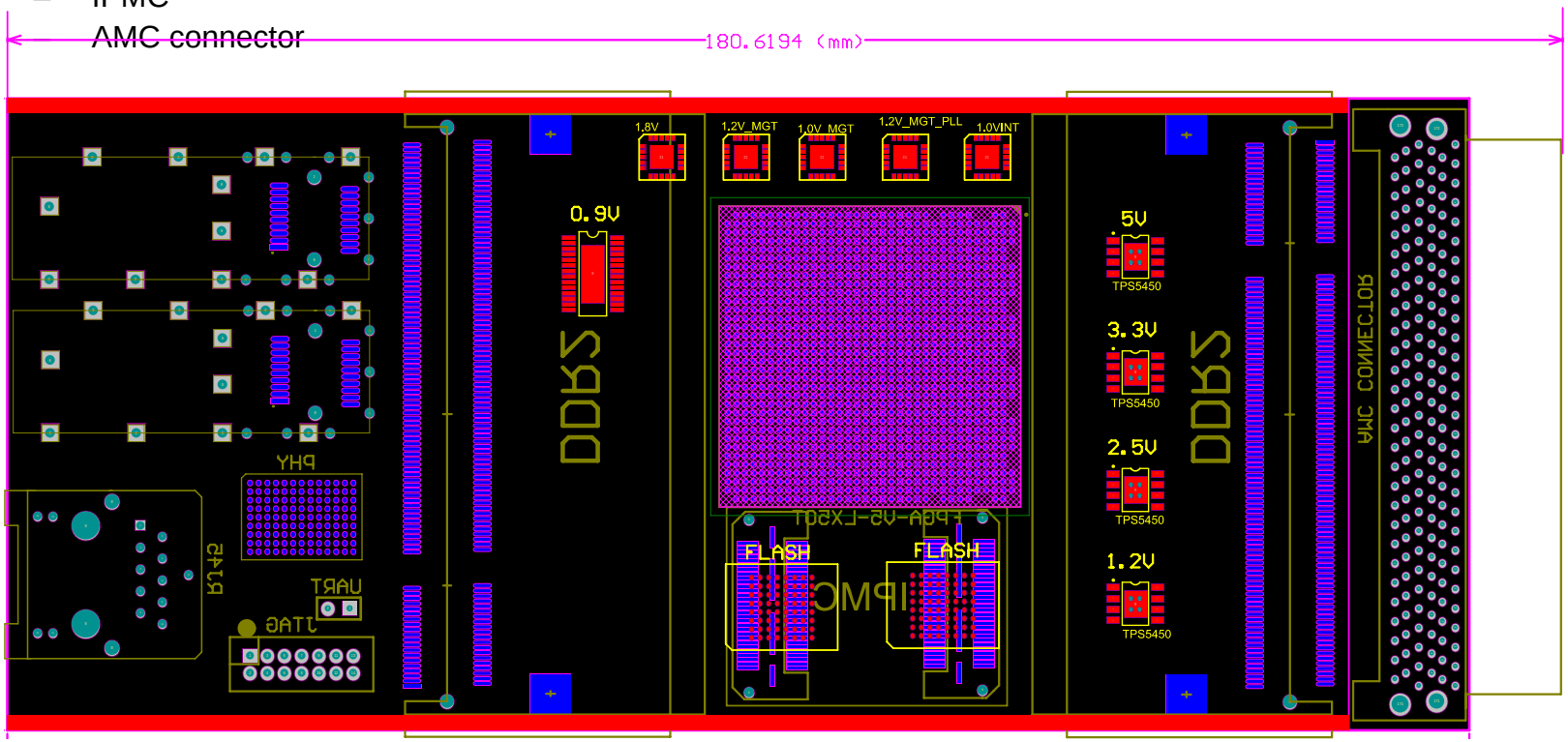
Daughter Board/AMC

- 2 x 3Gbps /FPGA
- 2 x 2G DDR2
- 1 Gbps ethernet
- 1 UART



AMC: PCB layout

- Component side
  - 2 x SFP+
  - 1 ethernet
  - 1 UART(on board)
  - FPGA
  - 2 DDR2
  - IPMC
  - AMC connector
- Sodering side
  - Powers
  - FLASHs



Short plan and summary for PXD DAQ development

- Dec. 2010 first prototype
- Hardware design is going smoothly

Thanks for attention!