LMU – Cluster Universe
Stefan Rummel

Power supply for the BELLE II PXD

5th International Workshop on DEPFET Detectors and Applications

29.09-30.09. Valencia

Overview

- News from LMU
- PS project schedule
- Requirement analysis
  - Parameter definitions currents, voltages
  - Transient behavior
  - Radiation, B-Field
  - Position of PS
- Regulation over long distances and test structures
- PS - Slowcontrol

News from LMU

- Since July member of the BELLE II collaboration

- Regular EVO meeting on PS development

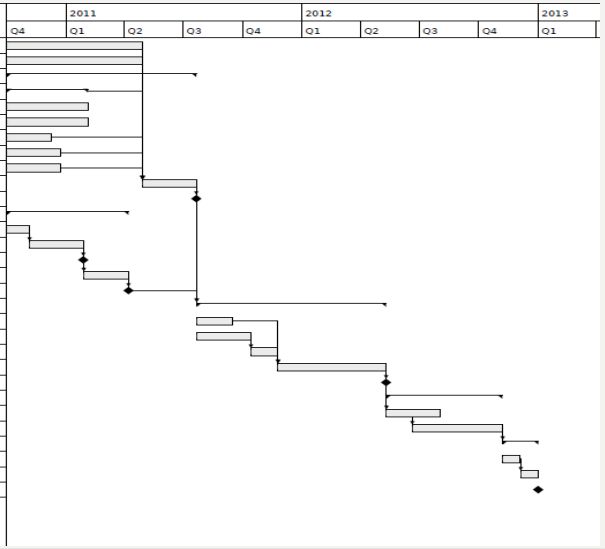
- Group is growing – Electronics Engineer Andreas Seiler has joint us in of August

- Setup of electronics lab is almost finished
  - Mixed signal oscilloscope / current probe
  - AC/DC active load
  - Signal generator, 6.5 digit DMM, PS's
  - Soldering equipment
  - Layout program – Altium Designer
  - ...

Project schedule

- Important milestones:
  - Demonstration regulation under realistic conditions (cable, distance, noise, transients...)
  - Demonstrate connectivity, steering of analog part
  - Prototype: demonstration of multi module operation, safety features
  - Prototype for testing of ladders in 06/2012
  - Commissioning beginning of 2013

Name	Work
Requierment analysis - Transient, noise, overvoltage	150d
Grounding scheme	150d
R&D analog	**410d**
Analyse regulation over large distances	**180d**
Test circuits (Remote sensing, negative output resistance)	90d
Simulation	90d
Simulation / Test Hardware current limits	50d
Overvoltage protection	60d
Design cables	60d
Layout of test circuits	60d
Demonstration of analog power supply channel	
R&D digital / steering	**135d**
Evaluation microcontroller, MS - FPGA's, Market survey	25d
Investigation with testboards - conectivity (ethernet, usb, spi, I2C), analog	60d
Decision: Interface for slow control integration	
Layout und production	50d
Demonstration of steering / Interface (scalability...), DAC's	
Prototyping	**250d**
Development of software	40d
Design and Layout	60d
Production	30d
Test - Laboratory, with DAQ, test beam	120d
Demonstration of multi-module operation, safety features in realistic environment	
Production	**160d**
Mass production	60d
Testing - burn in, specs achieved?	100d
Installation	**40d**
Shipping	20d
Installation & final tests	20d
PS system online	



Requirements update

Position of PS

- Baseline: Outside of detector (same as DHH)
- Moderate distance of ~15m from IP
- Primary supplies in electronics hut 30m from IP

Space weather forecast for PS

- Magnetic field ~10 Gaus (~ mT)

- Estimate on radiation based on outer layer of KLM - to our current best knowledge 0.48Hz/cm2

- Back on the envelope calculation gives:
→ 50rad over 5 years including factor 100 safety (assuming MIPS)

- Radiation and magnetic field seem to be no problem outside of the detector
- Commercial components should do the job

Parameter definitions

- High voltage increased from 40V to 80V due to lower resistivity silicon, punch through biasing and thicker detector

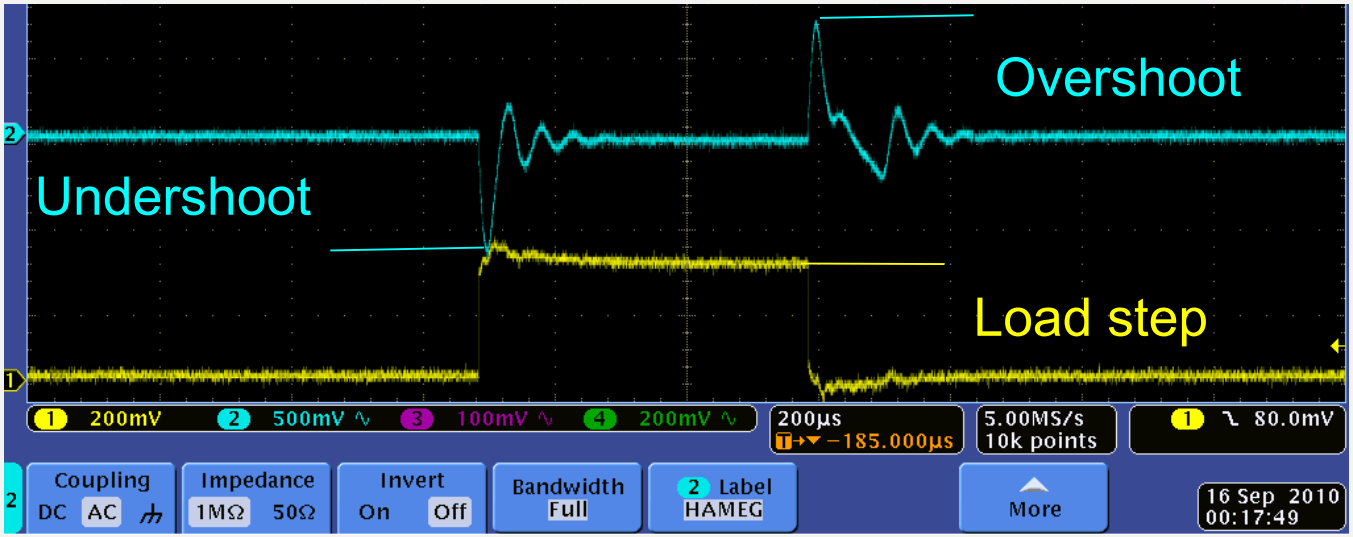
- For calibration propose the Gate voltage must be variable from threshold to nominal value (~ V_SOURCE to V_SOURCE + 6V)

- Ganging has also impact on power consumption:
  - I_SOURCE doubles from 100mA to 200mA
  - Currents of steering voltages
  - Rest should be stable

Transient behaviour

No regulation is ideal

- DC regulation not perfect
- Load steps lead to temporary deviations



Voltage at point of load

Current

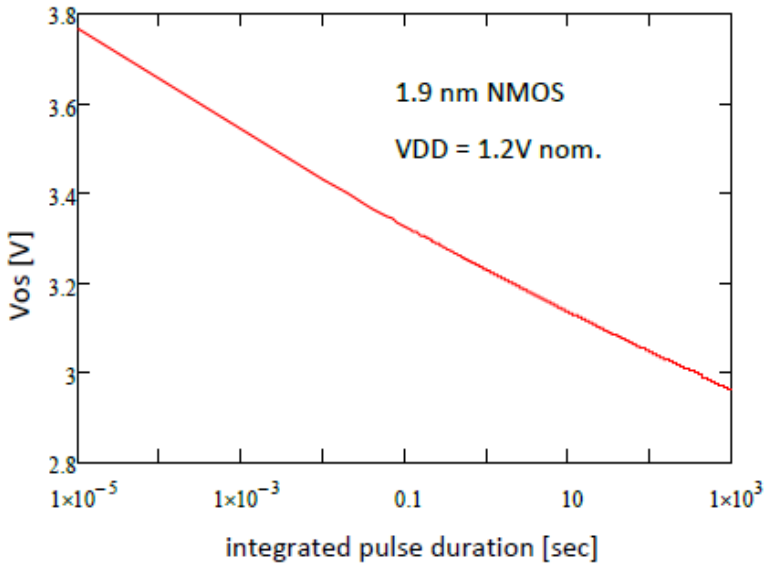
- Deviations need to be controlled:
  - Overshoots can damage oxide
  - Undershoot may lead to loss of data

DHP Maximum Voltage Ratings

universitätbonn

- two DHP voltage domains: core with **thin gate oxide** and IO with **thick gate oxide** MOSFETs
- recommended values according to the equations in the IBM CMOS 90nm (CMS9FLP) Technology Design Manual for **gate dielectric reliability** voltage limits:
  - **Vdc max**: maximum **static** DC voltage (@ 100.000 operation hours, T = 30°C)
  - **Vos 1%:** maximum **overshoot** for **periodic signals**, calculated for overshoot pulse width equal to 1% cycle time
  - overshoot due to power switching has much less duty cycle
  - transient stress damage is a product of **pulse duration** and the **number of events = integrated pulse duration**

	Tox [nm]	V nom [V]	Vdc max [V]	Vos 1% [V]
Thin oxide	1.9	1.2	1.6	2.7
Thick oxide	5.2	1.8	3.5	4.2



Transient behaviour

- Assuming: 50us overshoot, 1 overshoot/run, 10min/run
  → Duty cycle $<10^{-7}$
- Numbers at 30degC
- Need some room for radiation induced damage

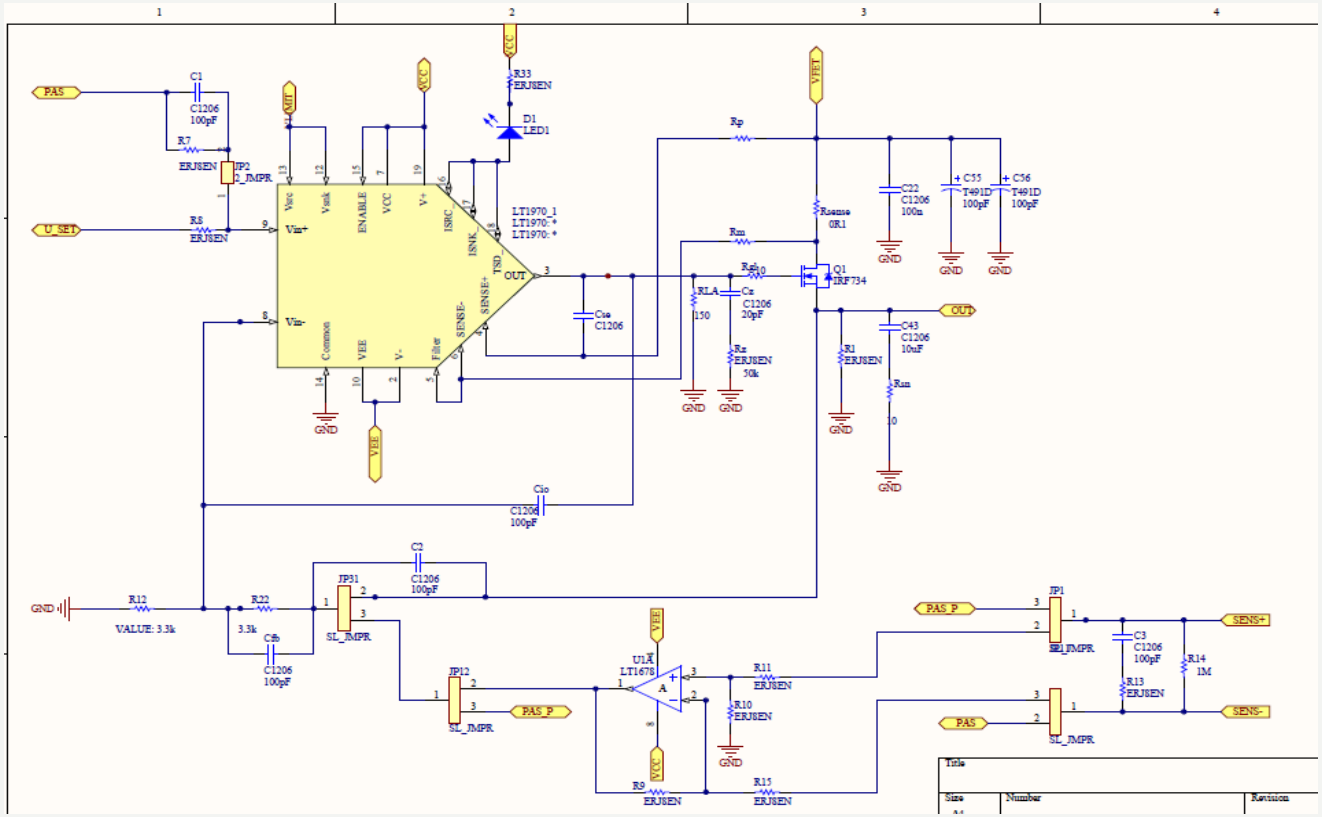
- „Vos 1%“ should be conservative – but some doubts remain…

Regulation over long distances

Regulation over large distaces

- Twofold approach:
  - Simulation (Matlab, Spice)
  - Experimental
    - Test regulator
    - Long cables

First test vehicle



- Discrete pass element linear regulator
- Hardware current limit
- Various ways of remote sensing – no, passive, active

First test vehicle

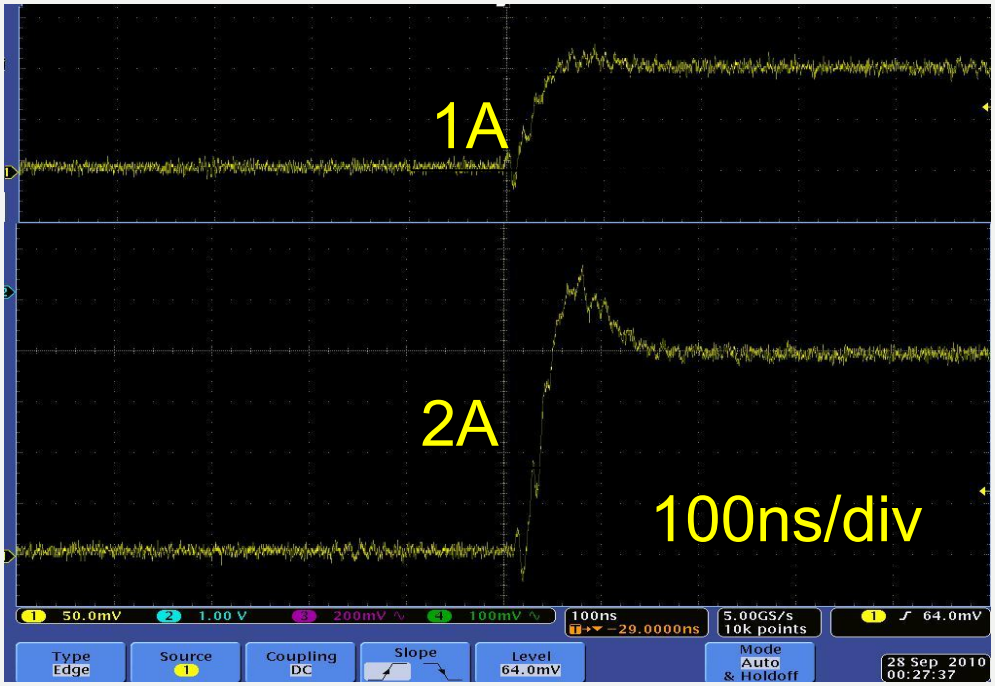
- Why LT1970?
  - Integrated current limit amplifier – hardware current limit
  - Enable pin and thermal shutdown
  - Specified from 5V to 36V supply voltage
  - >500mA output current
  - Also used in NI PXI-4110 PS

  - Very low dropout voltage
  - Output can be set down to 0V
  - Power consuming part separated from “intelligence”
  - FETS with low thermal resistance packages available → easy thermal management
  - NMOS – source at output → good PSSR
  - Precise current sensing on “high side” no additional resistor between load and regulator
  - Can be easily configured as current sink
  - Need additional voltage (few mA) to drive the FET

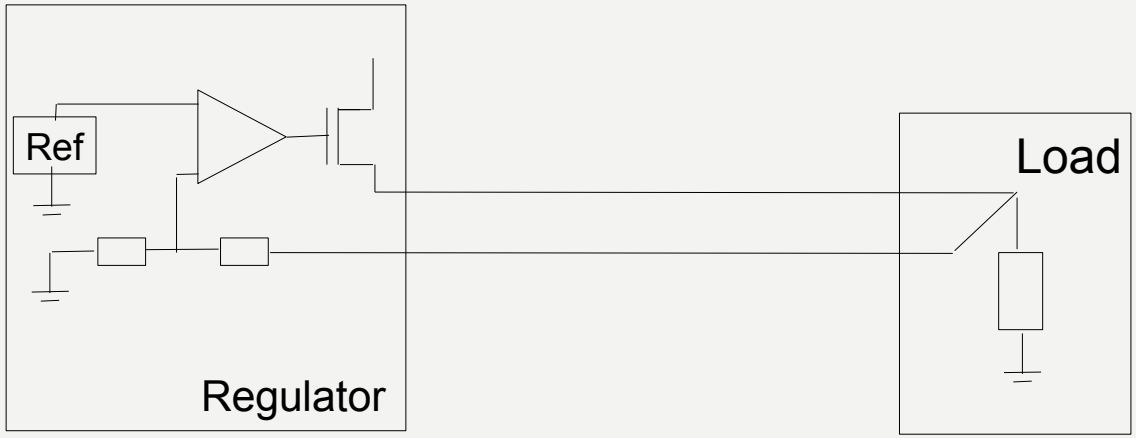
→ Allows a unified design which serves for ALL voltages (except HV)

Setup

- Circuit to simulate fast transients (few Amps @ 50ns risetime)
- Long cables in AWG12/18 as TDR cable
- Test bench is available

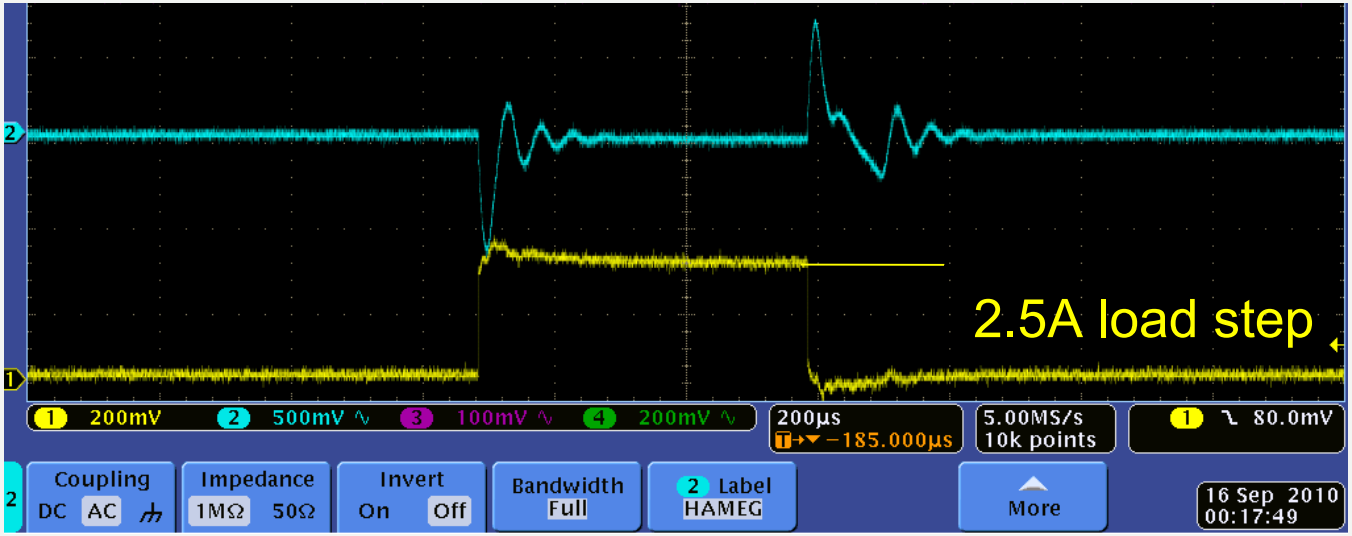


Setup



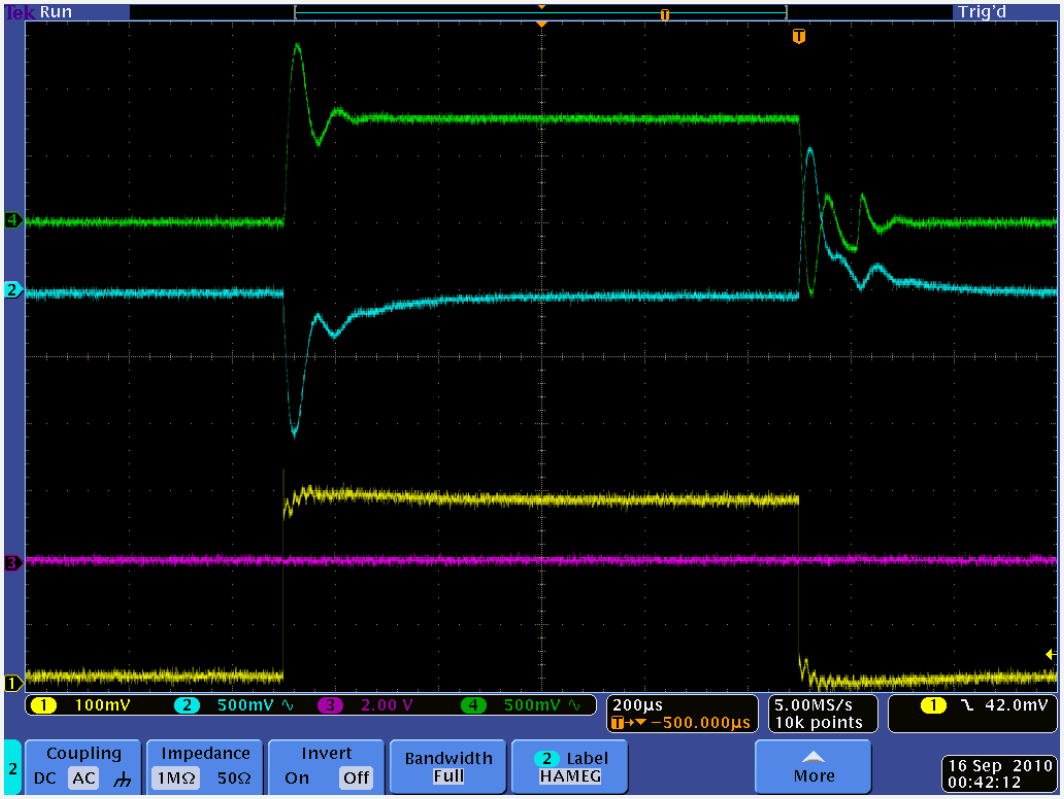
- Load and regulator share common ground
- Realistic delays

First results



- Wire: 7.5m, AWG 18 → 170mΩ
- (0.1/2.6)A load step
- Overshoot: 700mV for 20us

First results



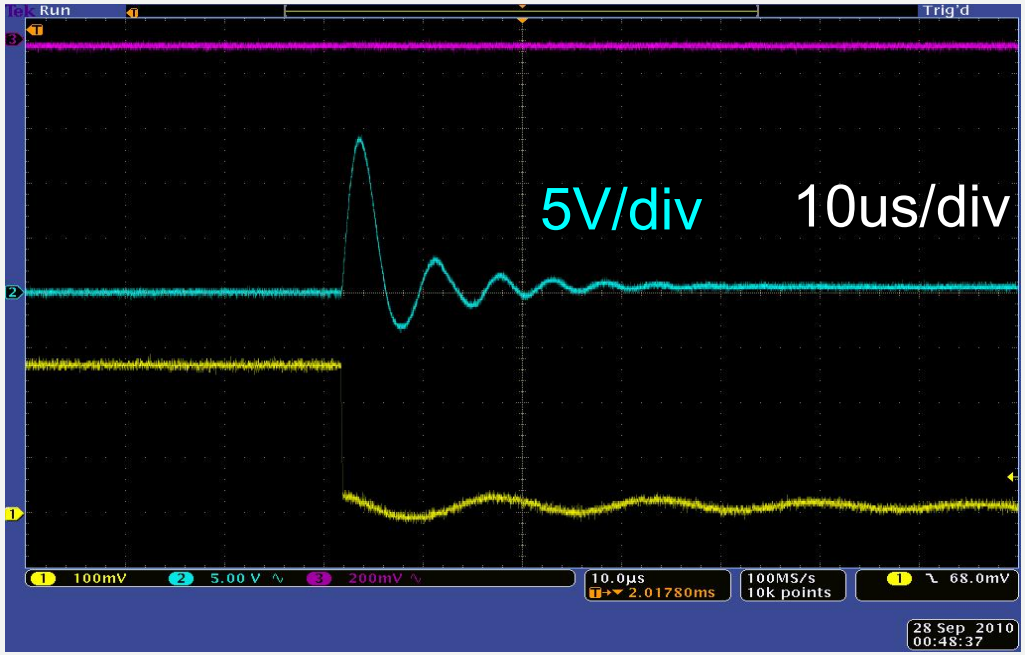
Voltage @ regulator

Voltage @ load

Current 1A/100mV

- Wire: 15m, AWG 18, 320mΩ
- (0.1/2.6)A load step
- Overshoot: 1V for 20us
- Increase of 40% compared to 7.5m

First results – low load capacity, long cable

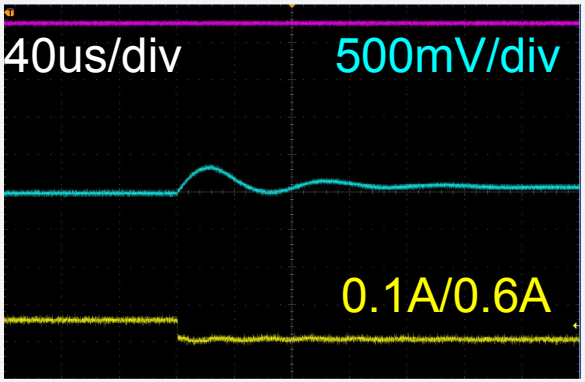


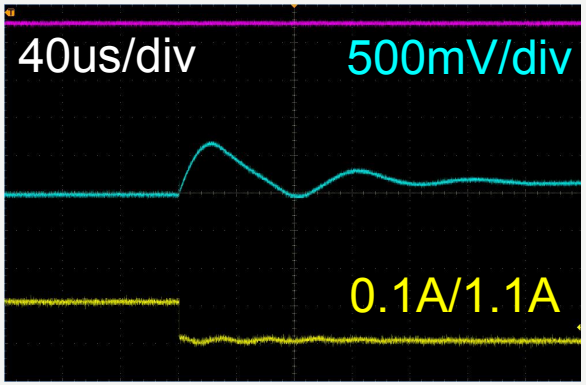
Voltage @ load

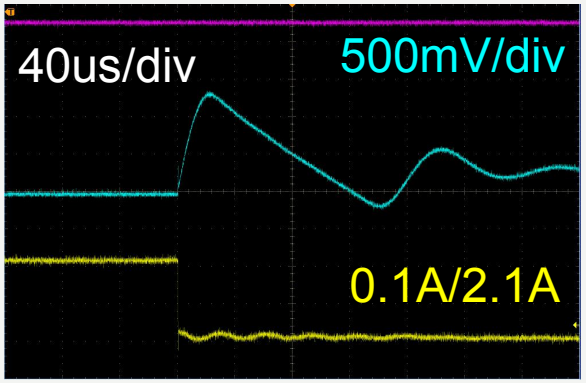
Current dI=2.5A

- Wire: 15m, AWG 18, 320mΩ
- (0.1/2.6)A load step
- Load capacity 100nF
- Overshoot: ~14V

First results – current dependence



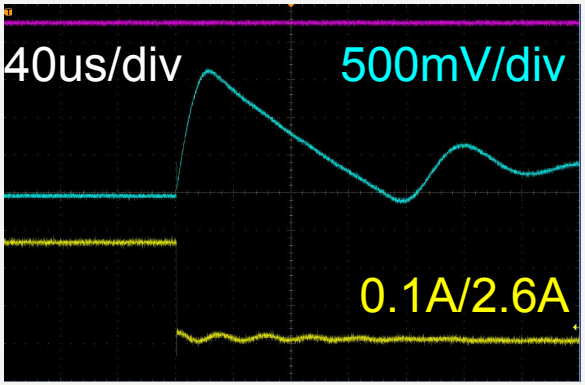




"DHP"

- Wire: 15m, AWG 18, 320mΩ
- Load capacity 10uF

→ Overshoot scales with current



"DCD"

Comments/ Next steps

- Up to now regulator behaved quite stable (100nF – 50uF ceramic capacitors, with 100mΩ ESR, various cable length)

- Get more experience with the regulator:
  - Region of stability
  - Comprehensive DC characterization
  - Noise

- Improve sensing:
  - Reduce DC error: Active sense amplifier with high input impedance
  - Test impact of termination (at HF)

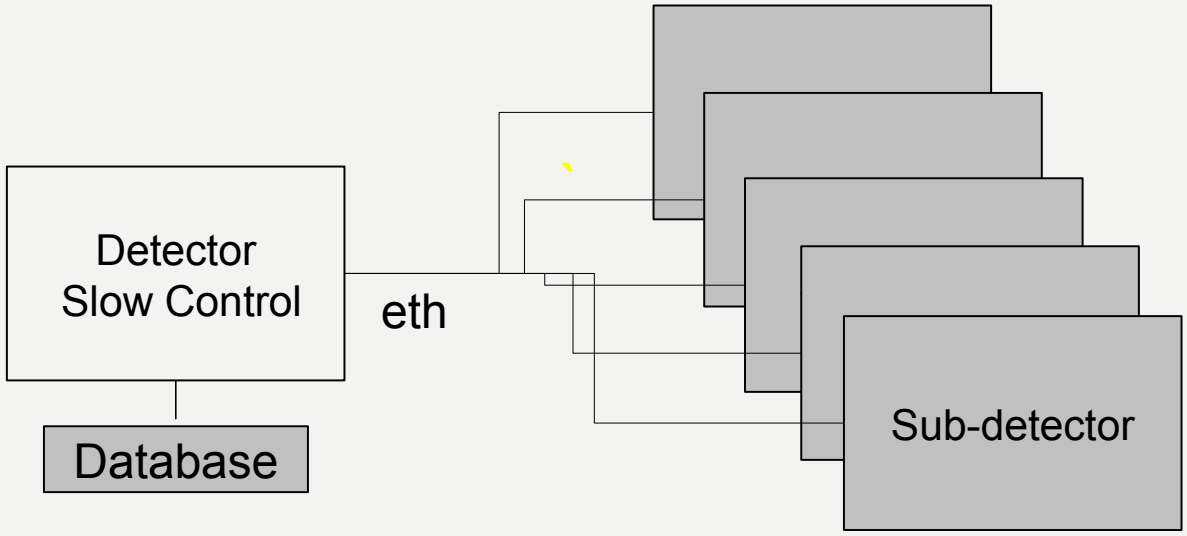
- Test current limit

- Include flex (prototype) into tests

Slow control

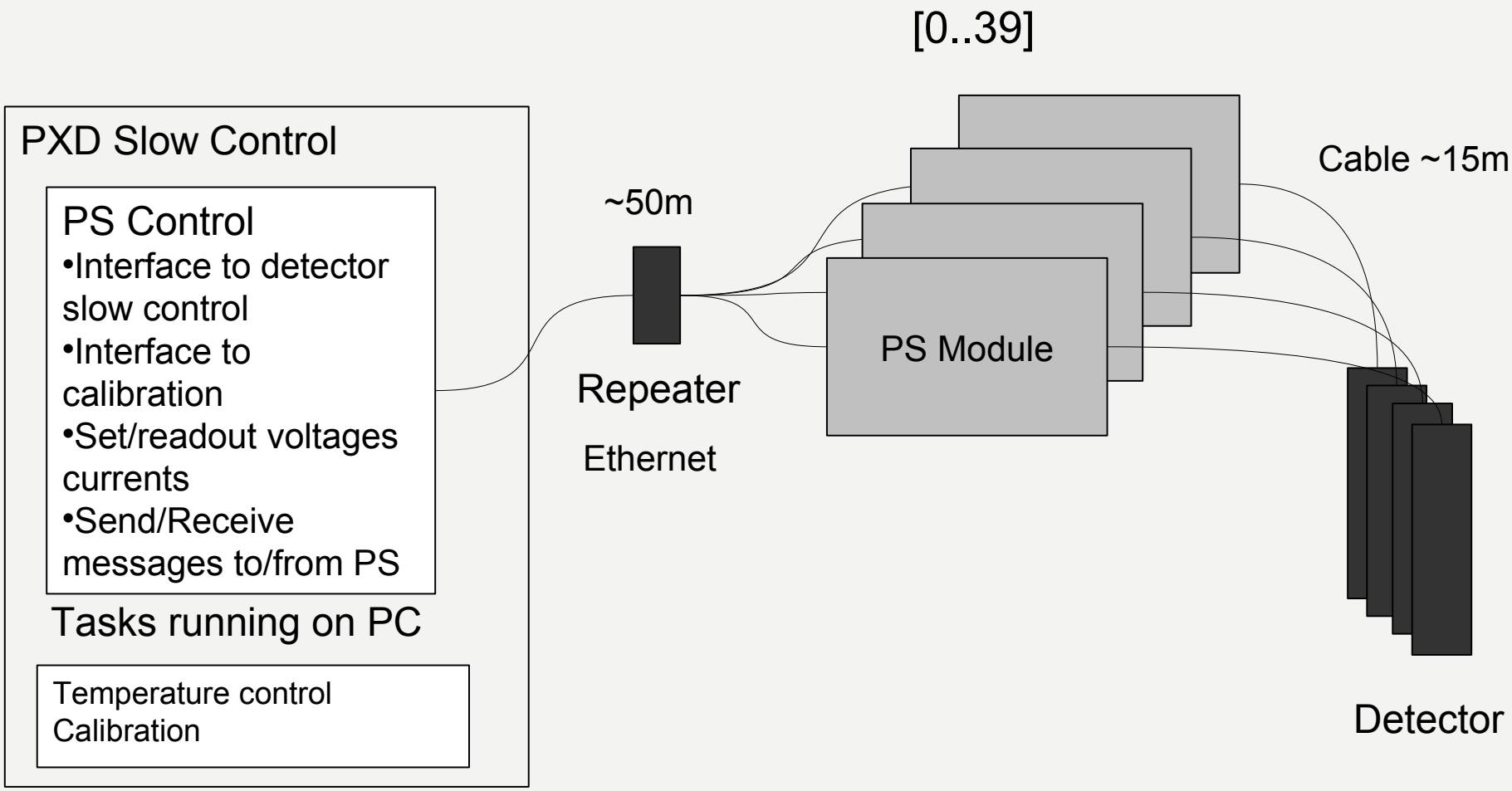
Belle slow control system

- Slow control
  - Control of services (power, cooling)
  - Logging of temperatures, voltages, currents, calibration data...



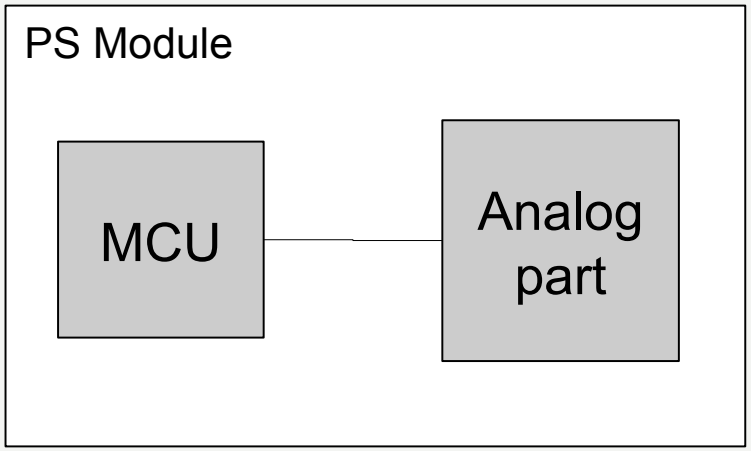
- Distributed system
- Connected via Ethernet
- Each sub-detector provides a producer

Power supply system



Power supply module

- Tasks on MCU
  - Continuous reporting to PS control (~10Hz)
  - Error handling
  - Error messages in case of failures
  - Receive messages from control
  - Readout currents/voltages
  - Set voltages and currents
  - Start and stop sequences



- Interface to outer world ETH
- Interface to analog section (SPI, I2C)

- Looked into various MCU architectures – identified ARM Cortex – e.g. STM32F as interesting

First contacts with TUM-INF

- TUM – computer science chair for “Robotics and Embedded Systems” with strong background in safety critical systems, embedded systems, real time applications...

- First exploratory discussion with Prof. Knoll

- Showed interests in the software part of the PS slow control (embedded part and PC)

Open issue

- Overvoltage protection
  - For low currents – no problem – can be made on PS level
  - *Wishlist: High current OVP on patch panel*
    - Radhard solution requiered
    - Currently looking into ATLAS-SCT solution

- Maybe we can relax this:
  - DHP core: Vdc max-Vnom = 400mV
  - DHP IO: Vdc max-Vnom = 1.7V
  - PS voltage at 1A: Vnom+300mV (AWG12 15m + 150mOhm flex)
  - → OVP @ PS is able to limit the voltage to safe regions

Summary

- Requirements on voltages, transient behavior are converging
- PS development at LMU has started, first circuitry tested
- Results under realistic conditions – cable length, various loads can be expected till next B2GM

Backup

Simulation

- Simulation of regulator response with delays
- Delay at least L/c c~0.6c0 → 55ns for 10m cable
- Investigated model:

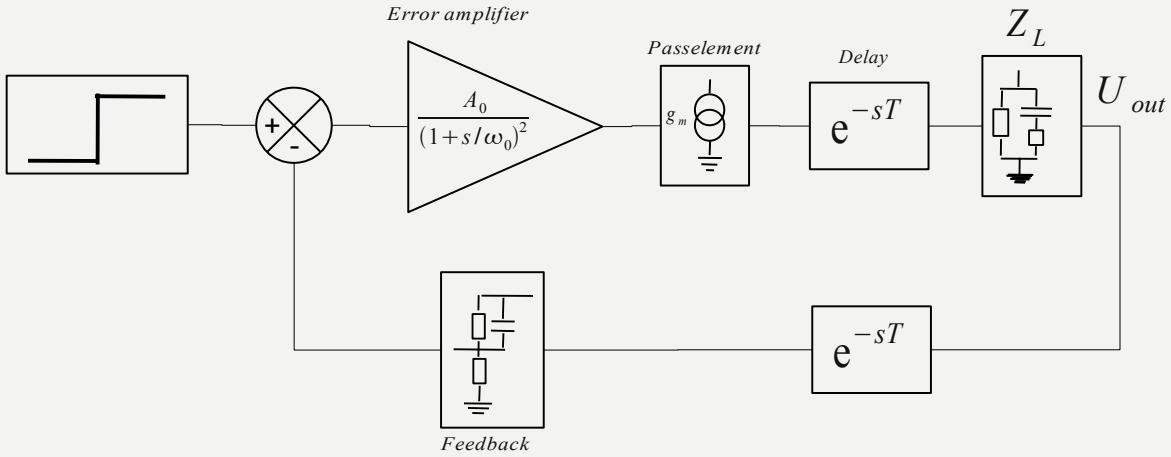
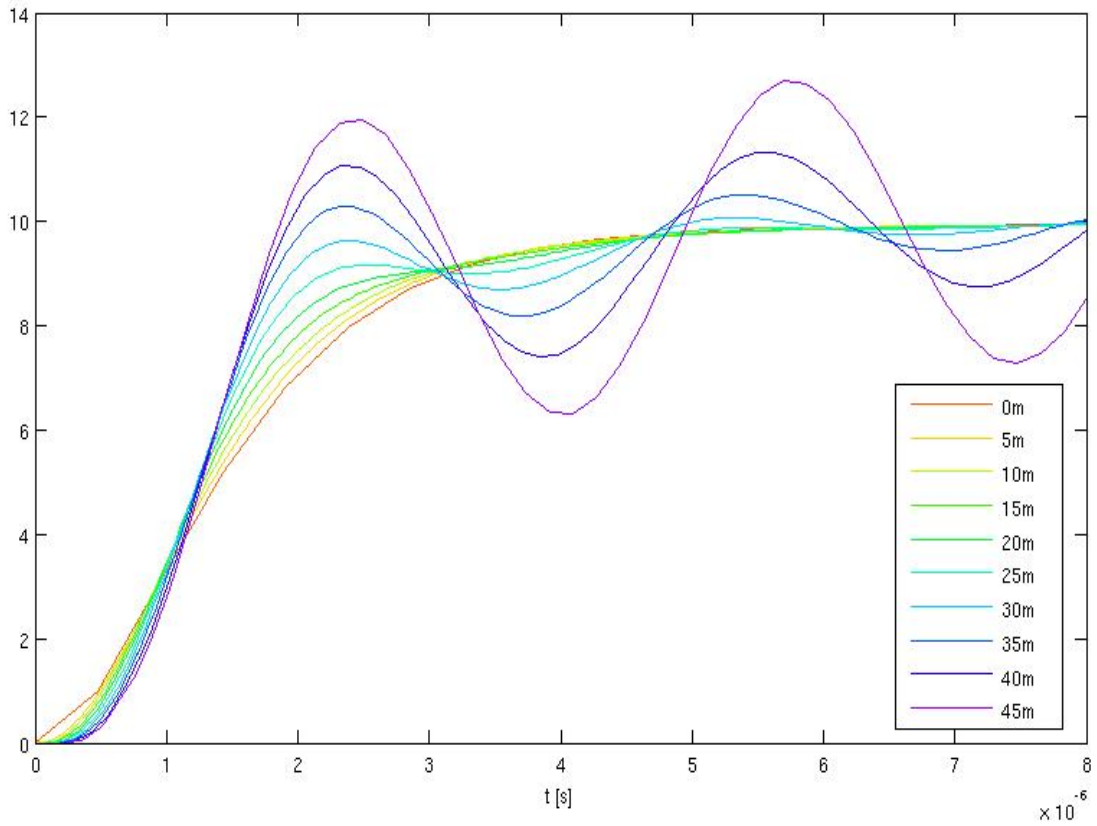


Figure of merit:

- Step response
- Settling time, over shoot, rise time...
- Phase margin

Simulation – first example



Setup

Erroramp.:
A0 4k
w0 50kHz

Passelement:
Gm: 2S

Feedback:
R1/R2: 1/10
Cfb: 150pF

Load:
Cload: 10µF
ESR: 0.1Ω
Rload: 1Ω

C/C0 0.6