UNIVERSITÄT
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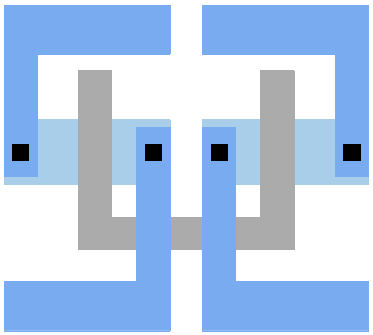
DCDB Based DEPFET Readout System



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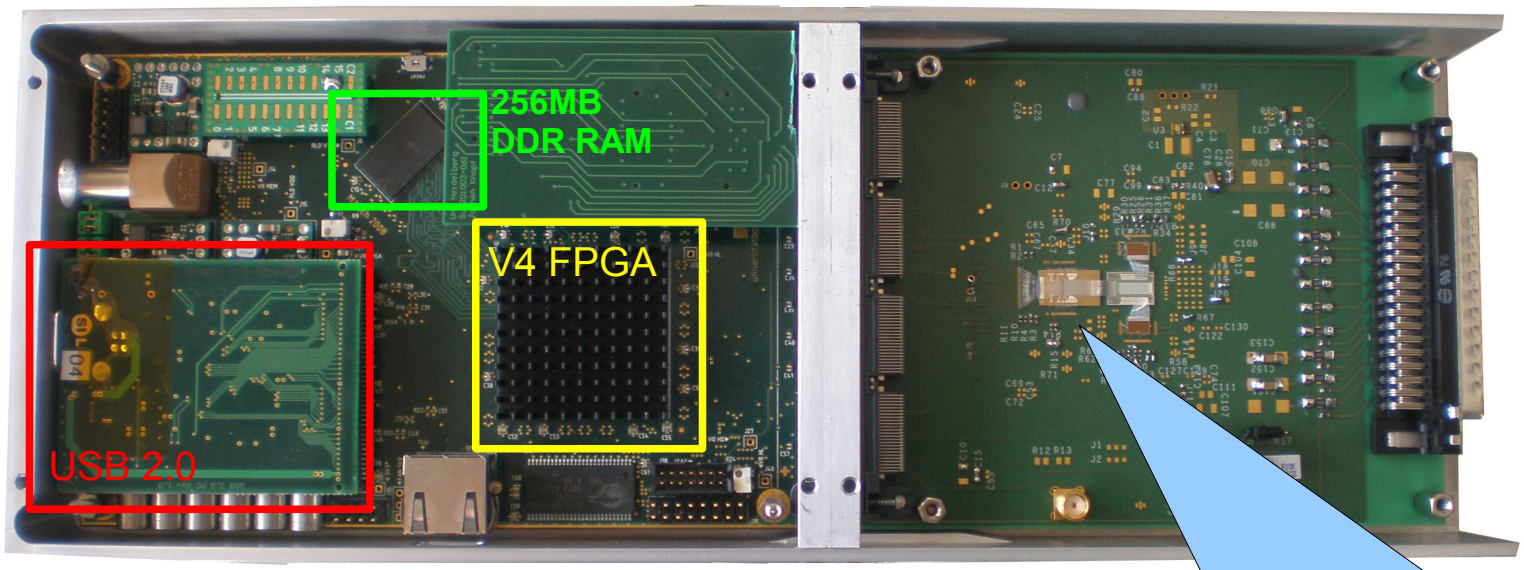
5th International Workshop on
DEPFET Detectors and Applications

Valencia, Spain

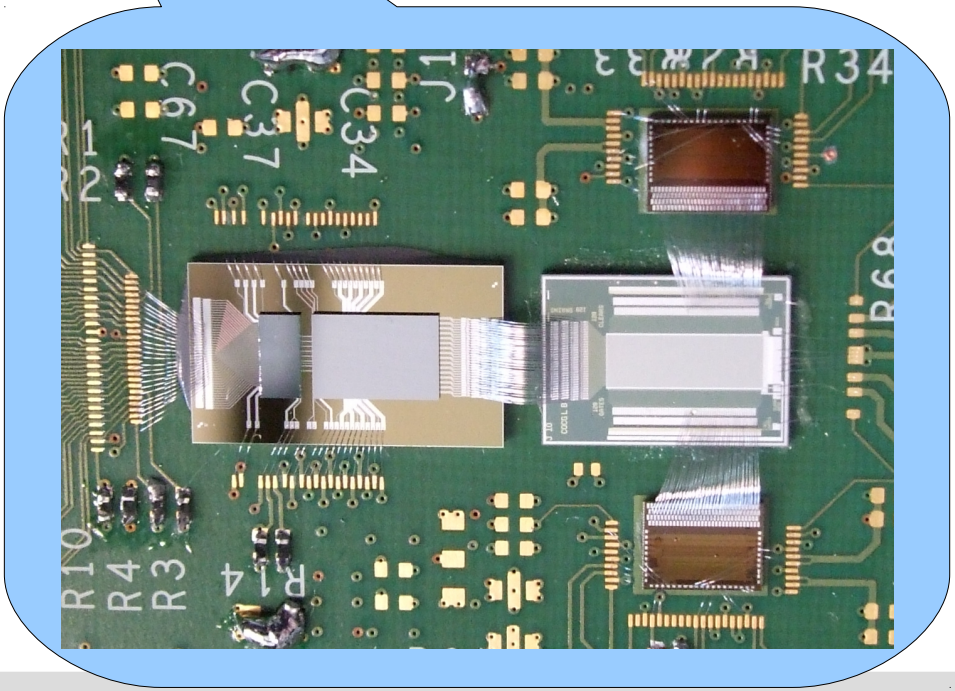
September, 2010

DEPFET Readout Setup: Picture

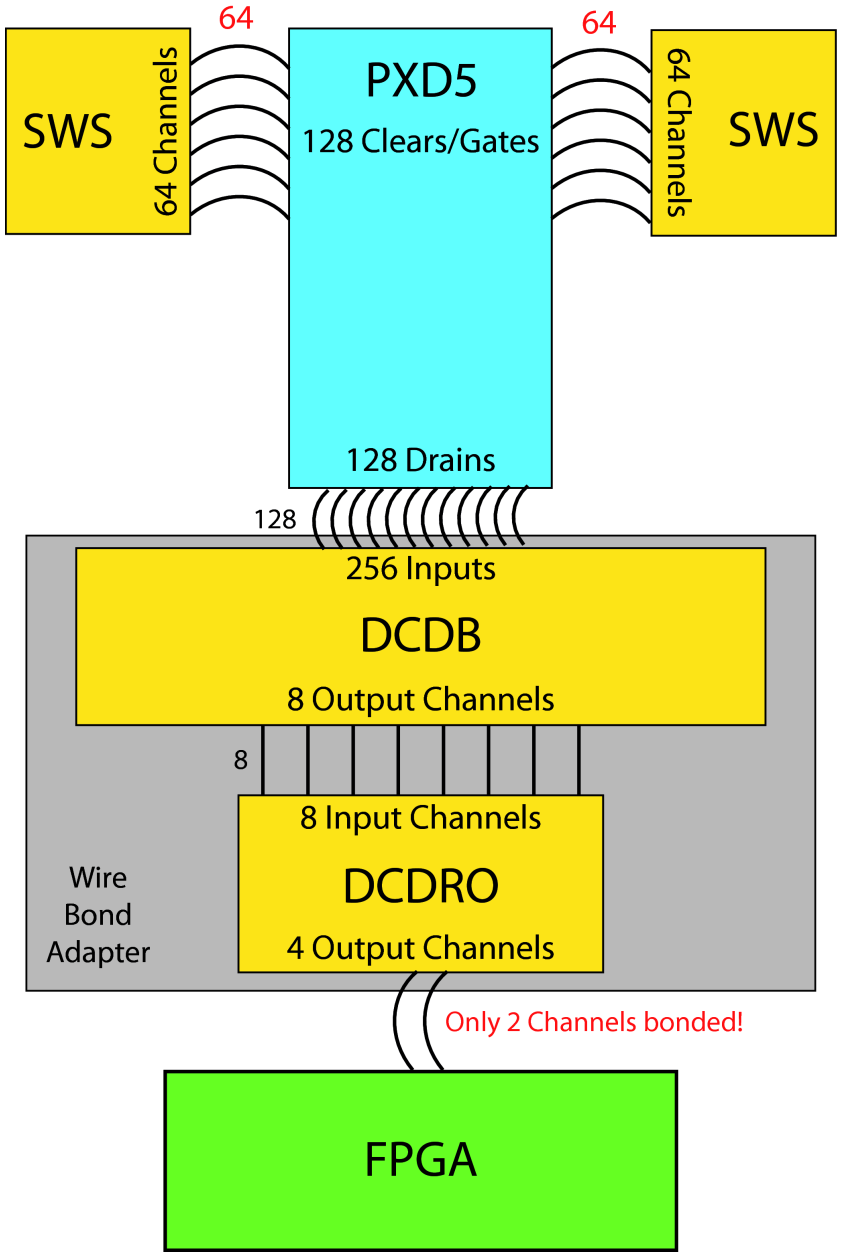


Components:

- Virtex4 FPGA Board (SiLab, Uni Bonn)
- Hybrid 3.0 (HLL, MPI Munich)
  - PXD5 DEPFET Matrix
  - 2x SwitcherS
  - DCDB/DCDRO mounted on the Wire-Bond Adapter



DEPFET Readout Setup: Schematic

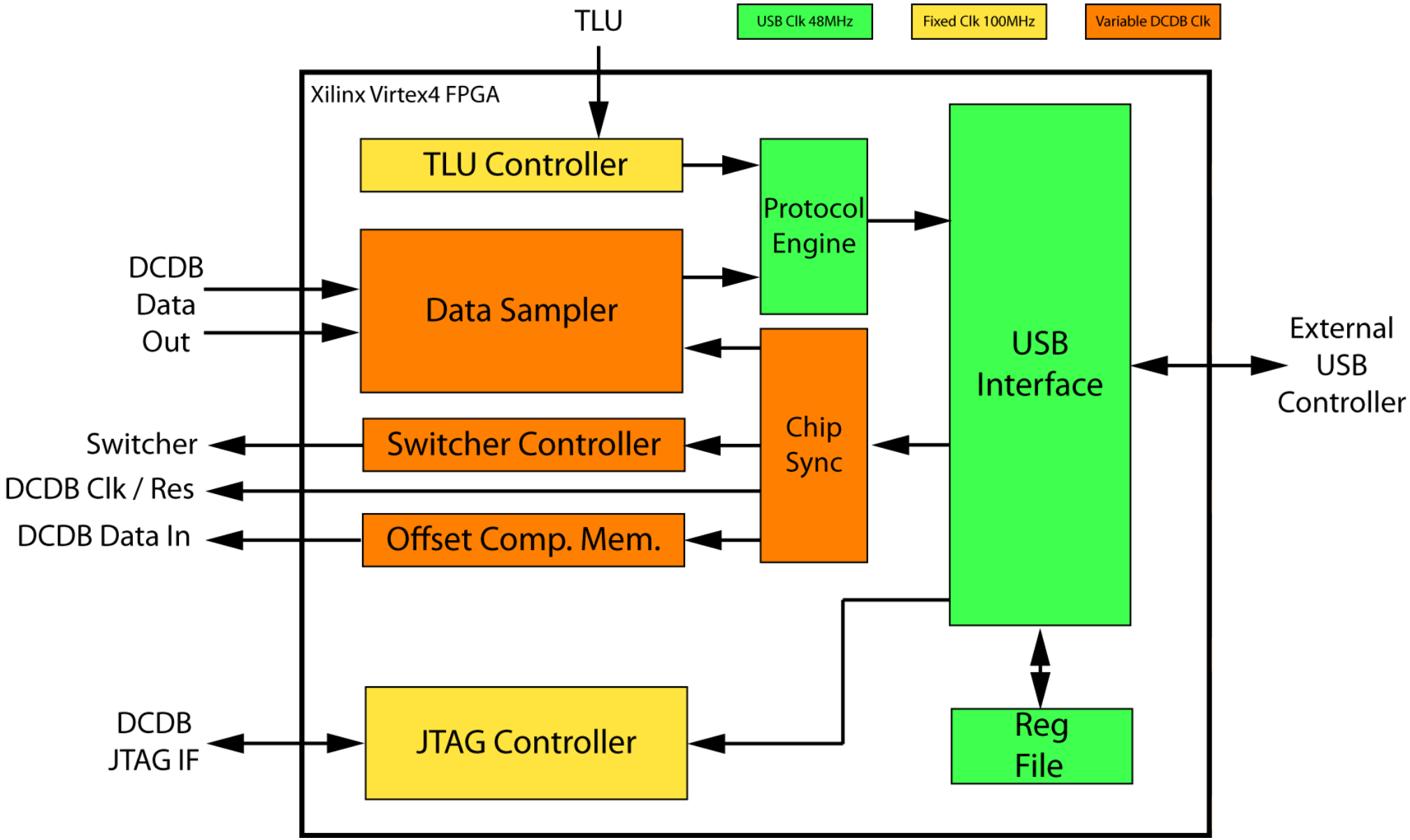


The components are not completely interconnected:

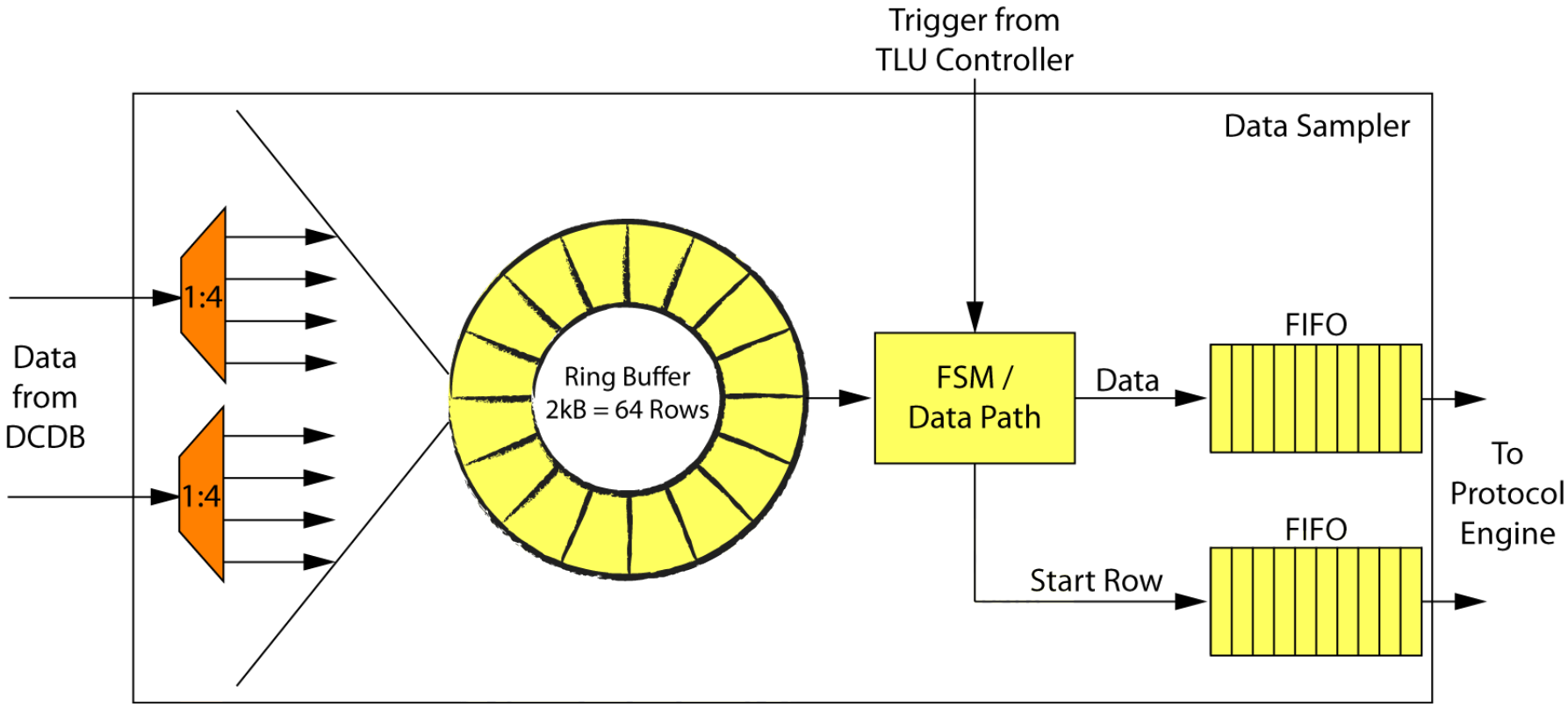
- ✗ 64 of 128 Matrix rows are connected
- ✗ 2 of 4 DCDRO output channels are connected

→ Only 25% of the DEPFET Pixels are connected!

FPGA Firmware - Overview



Firmware Details: Data Sampler



Data flow:

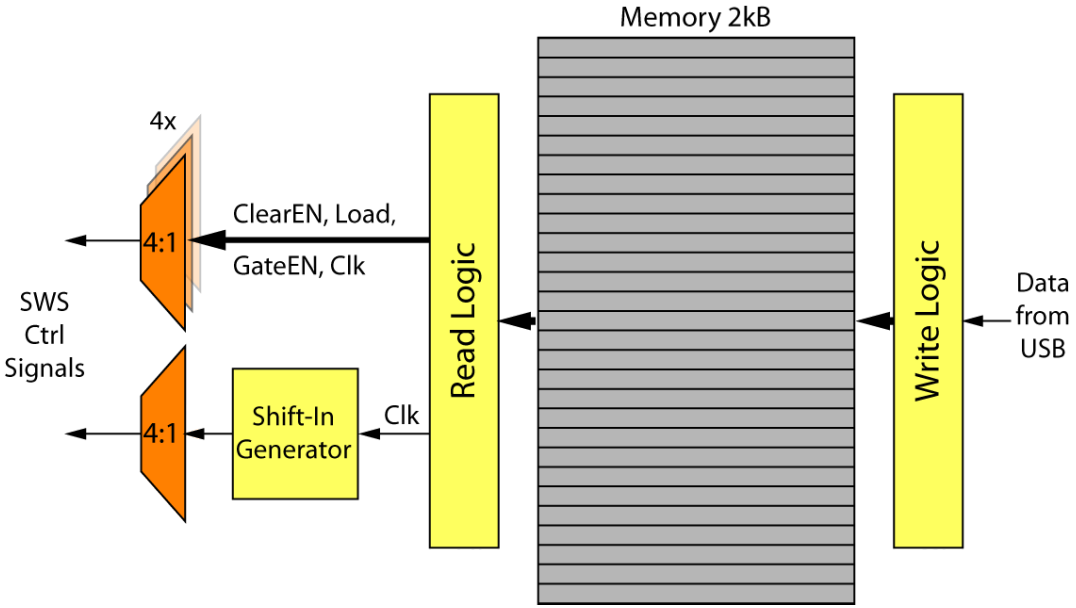
a) Incoming data is deserialized and continuously stored to the ring buffer.

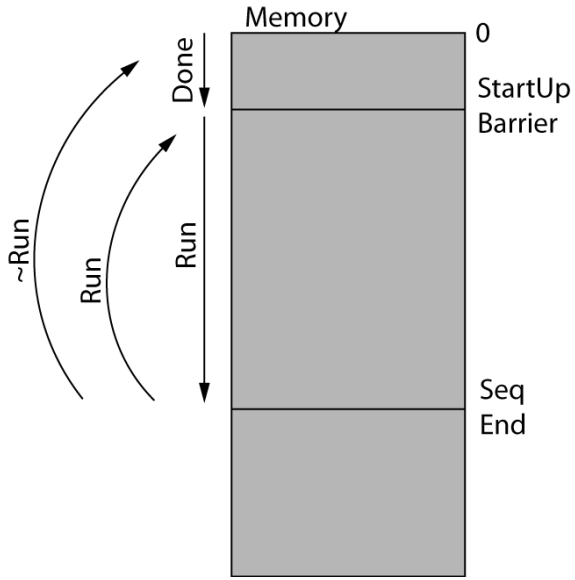
b) On trigger, the data is transferred from the ring buffer to the data FIFO.

c) The corresponding start row is stored to the start row FIFO.

Ring Buffer: The system is aware of processing triggers coming **after** the data!

Firmware Details: Switcher Controller





Mode of operation:

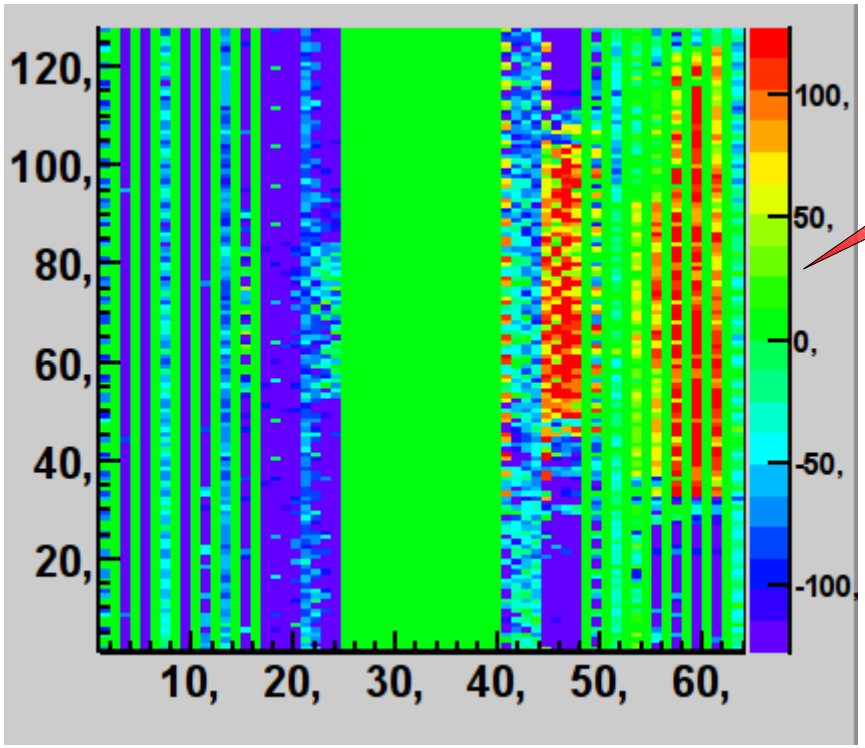
- Control signal sequence is stored to a memory inside the FPGA (ClearEN, GateEN, Load, Clk)
- Sequence is driven on the Switcher's signals synchronously to the DCDB
- “Shift In” signal is generated internally

Algorithm:

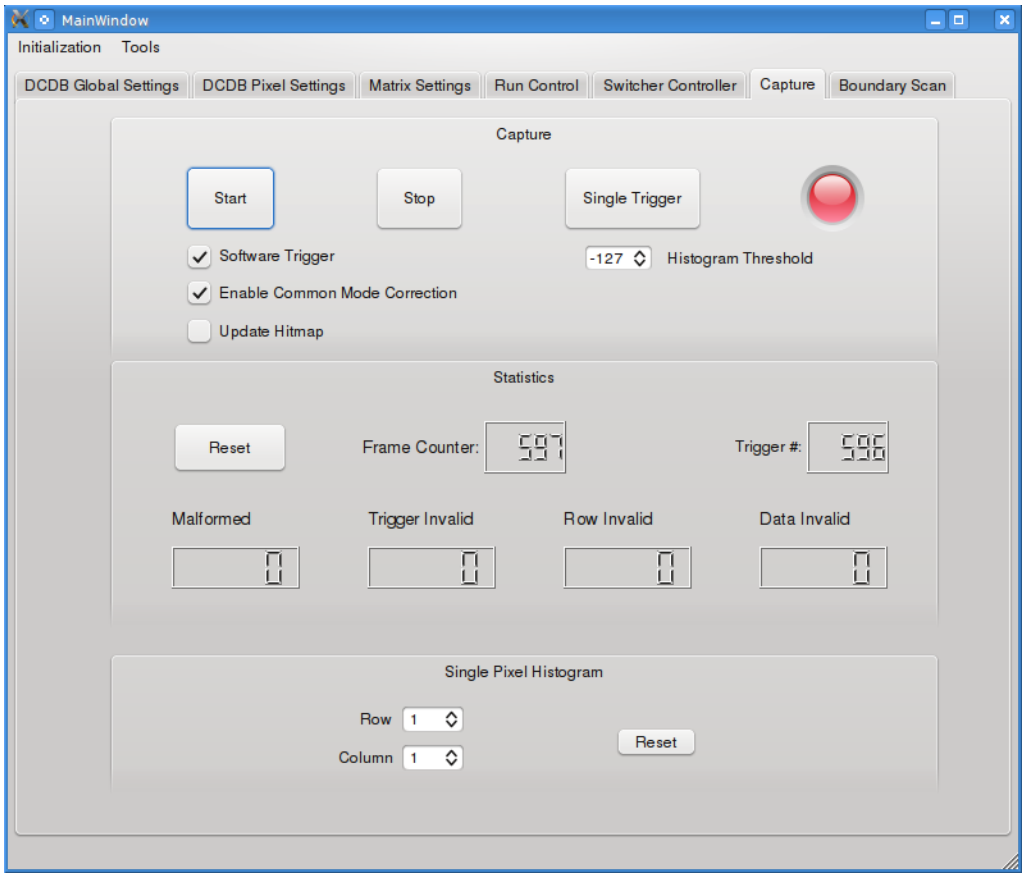
- Processing starts as soon as the memory is programed
- StartUp-Sequence brings the Switcher into a defined state
- Wait at StartUp-Barrier until DCDB is running
- Start Run-Sequence synchronously to DCDB
- Loop through the Run-Sequence until system stops and leave the Switcher in a defined state at the StartUp-Barrier

Measurement Results

Readout Software / First Read Frame



Note:
Measurements were taken at 100MHz DCDB clock frequency



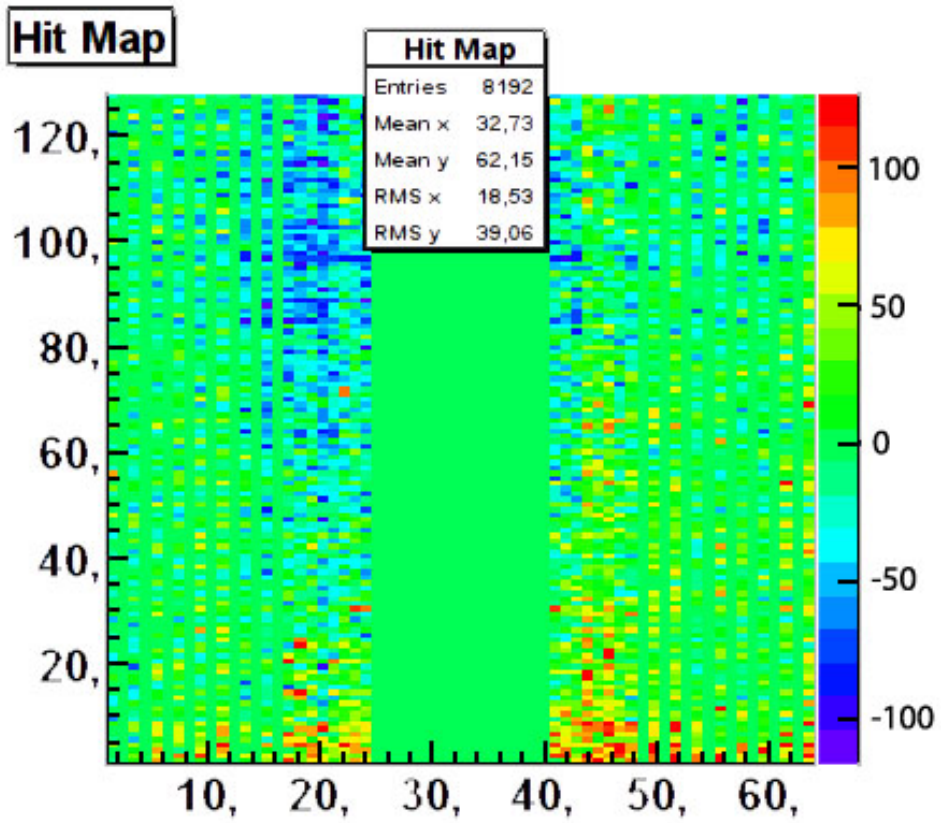
DCDB test software was extended in order to read and display DEPFET matrix frames.

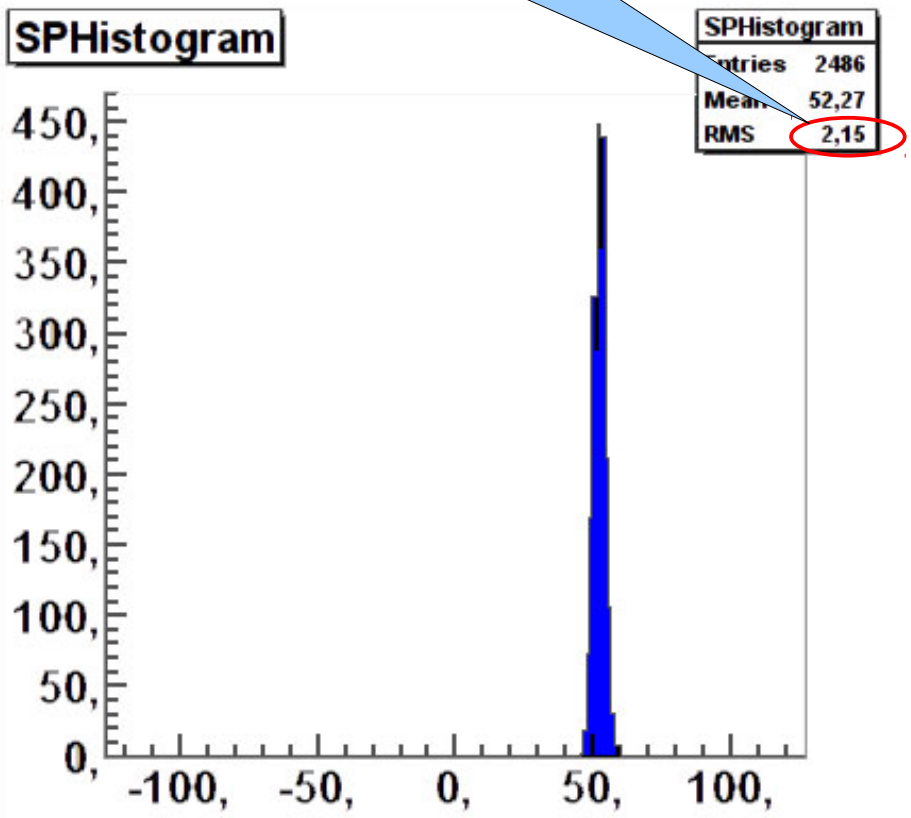
Data processing features:

- Common Mode Correction
- Pixel tuning (subtraction of pixel's mean value)

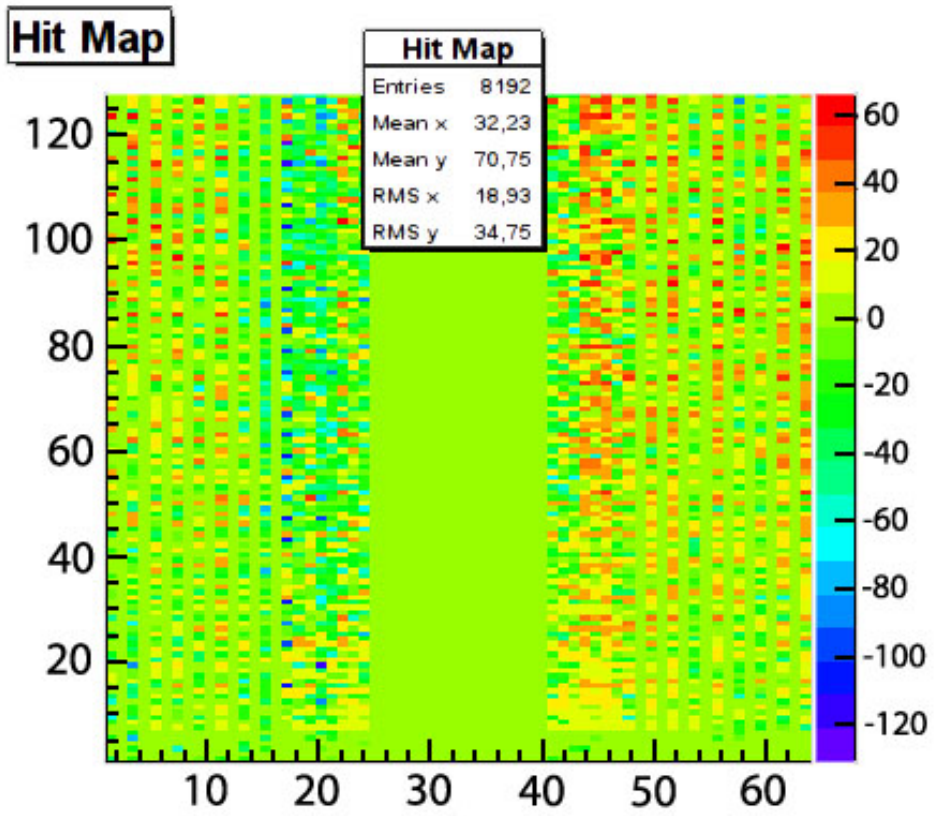
Noise Measurement Without Common Mode Correction

Noise (RMS): 2,15 ADU
@ 33nA/ADU Gain
→ 70,95nA Noise

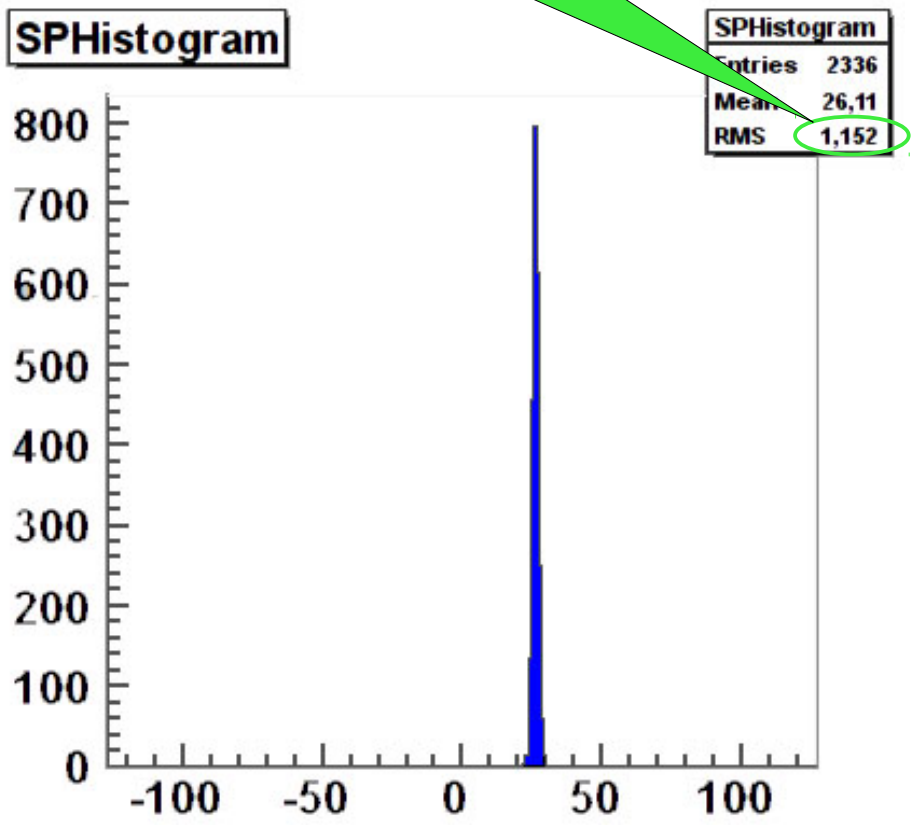




Noise Measurement With Common Mode Correction



Noise (RMS): 1,152 ADU
@ 33nA/ADU Gain
→ 38nA Noise



DEPFET Readout Summary

- ✔ PXD5/DCDB/SWS readout firmware is available and tested.
- ✔ First measurements have been performed – with success:
  - ✔ Response to light
  - ✔ Noise Measurements with/without Common Mode Correction
  - ✔ Radioactive source detection with Cadmium (Cd-109)

Next steps:

- ➢ Hybrid 3.1: Larger frame size induces slight changes for the firmware
- ➢ Integration into DAQ!
- ➢ Preparation for Testbeam 2010

Thank you!