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Flex Test Structures
Update

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Challenges

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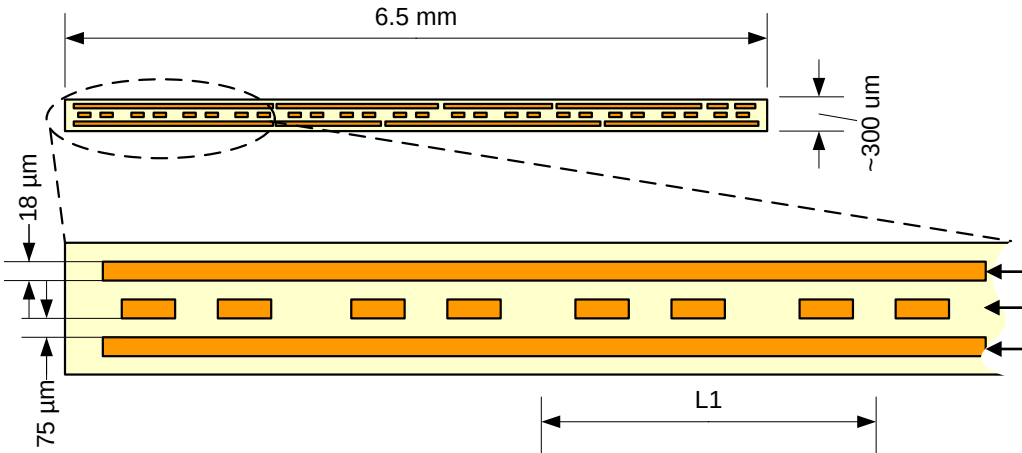
- need to cover 12-15m between module and DHH with combination of flex- and TWP cables
- active repeater circuits not recommended (radiation hardness, space, power consumption)
- no bulky connection between kapton and TWP and power cables
- make kapton part as short as possible
  - signal integrity issues with kapton flex: dielectric loss of the polyimide, resistive loss of the narrow signal traces
  - standard S/FTP (shielded foil twisted pair cable, Cat-6) has better HF performance (but needs to cover 12-15m still)

Proposed layer stackup



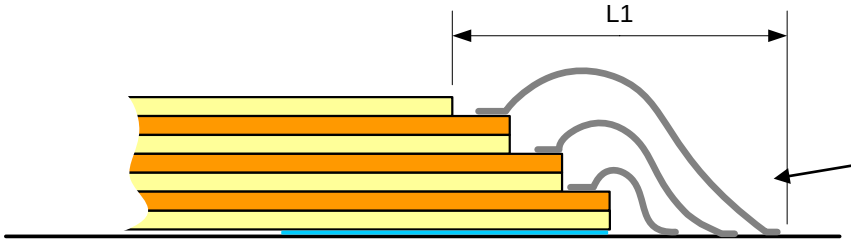
perpendicular cross section a)

cross section zoom in (not to scale) b)

(split) power plane

differential strip lines

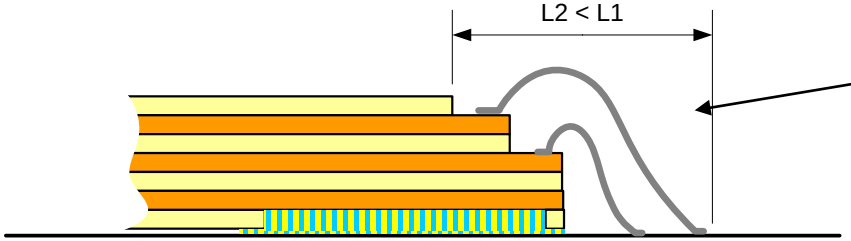
(split) ground plane



c)

three wire bond rows, flex glued to substrate (electr. passive)

longitudinal cross section at module end



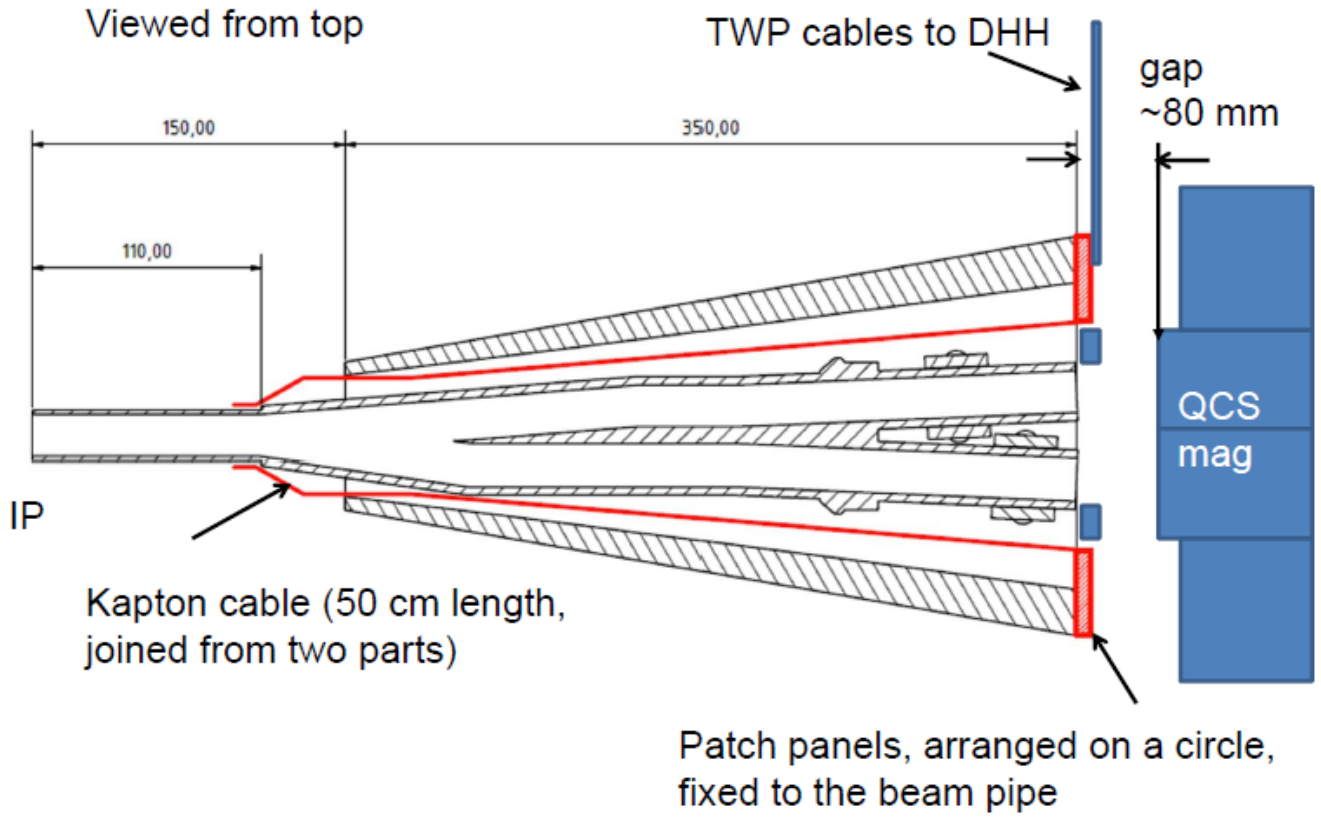
d)

alternative option:

two wire bond rows for signal layer and top layer and z-axis glue (or solder or silver epoxy) for bottom layer

Length Constraints

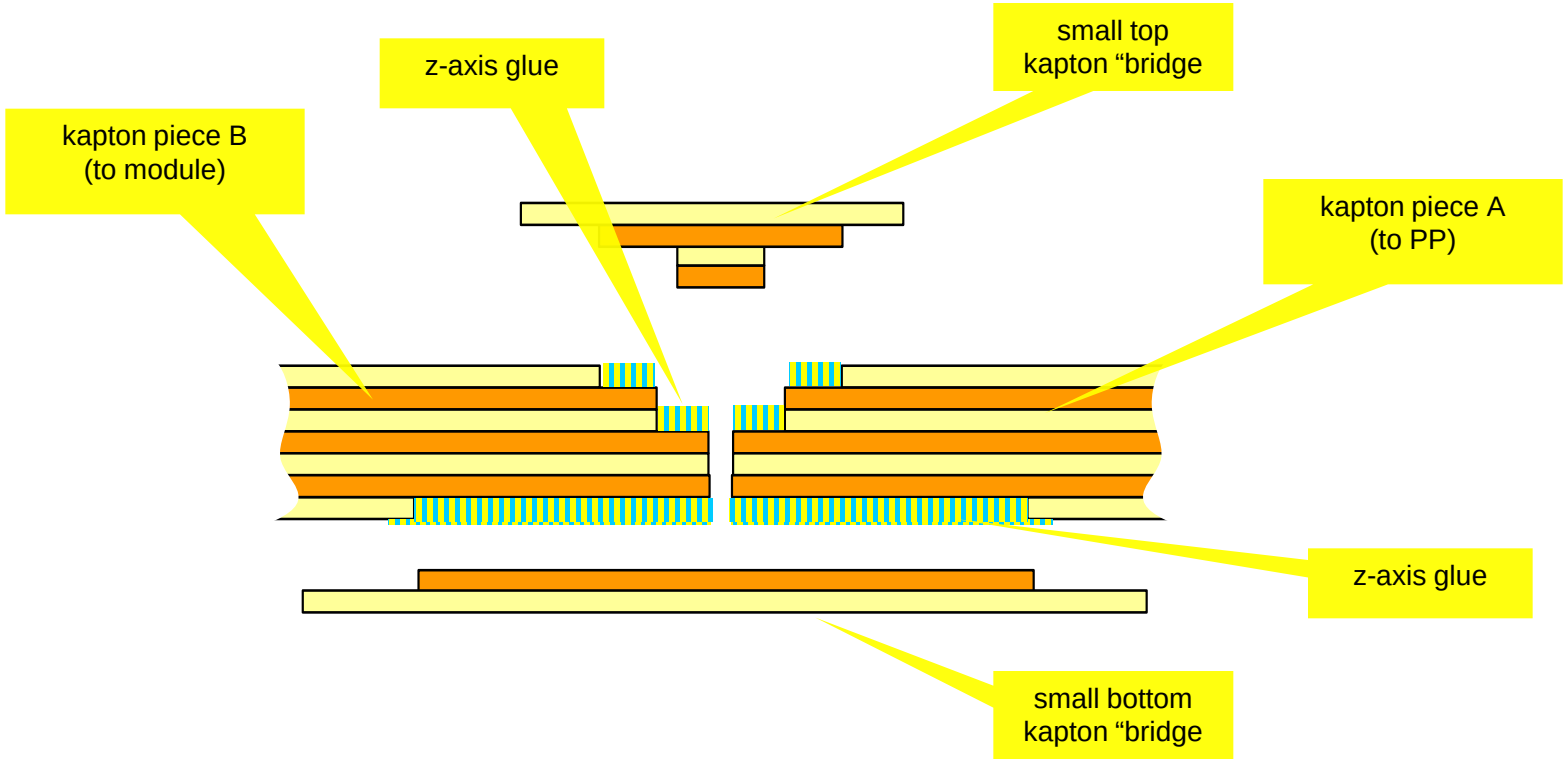
- place patch panel outside of the shield
  - better handling during installation
  - more space for patch panel



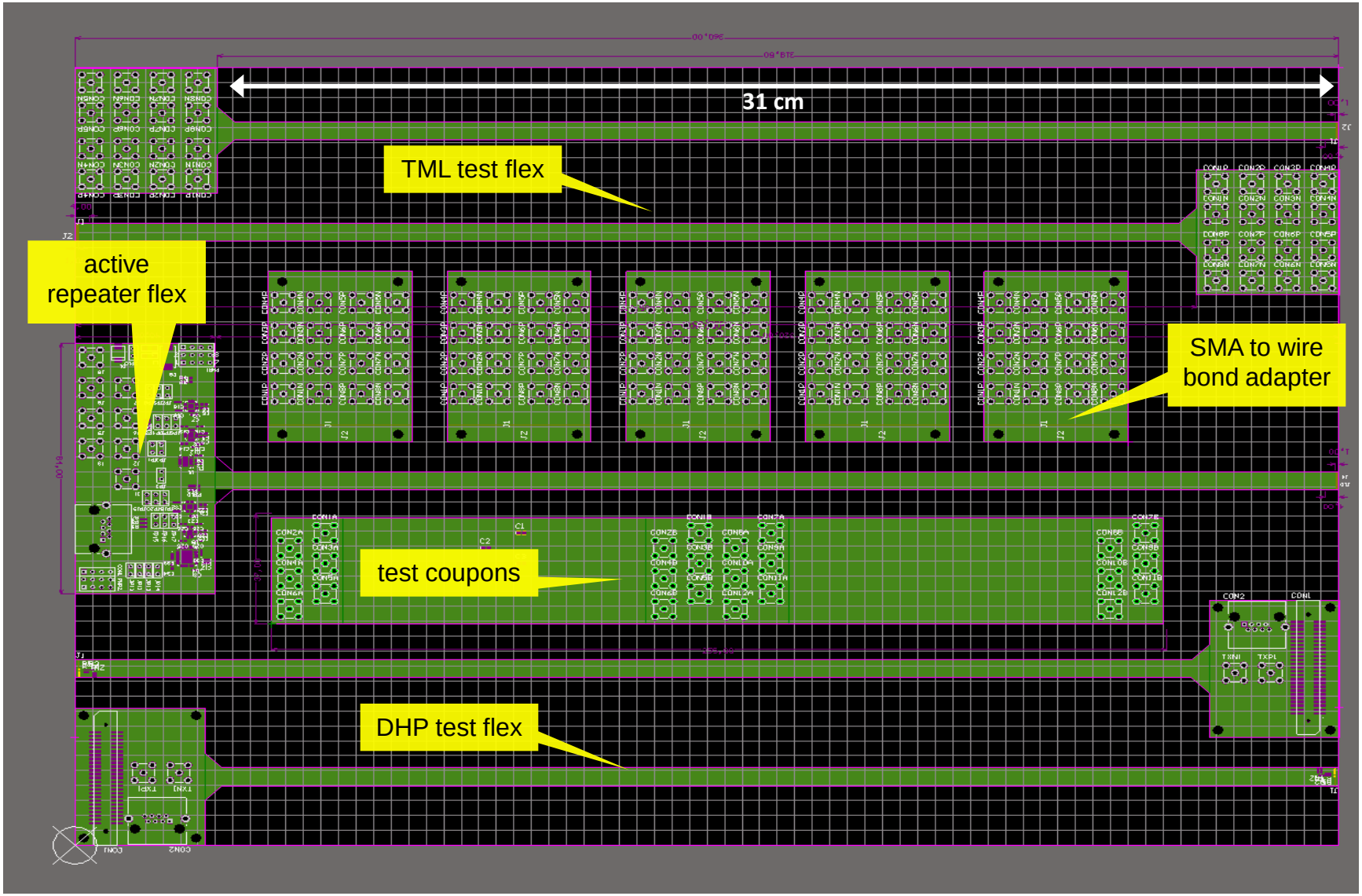
Length Constraints

min. length to have the PP just outside the shield is ~50 cm

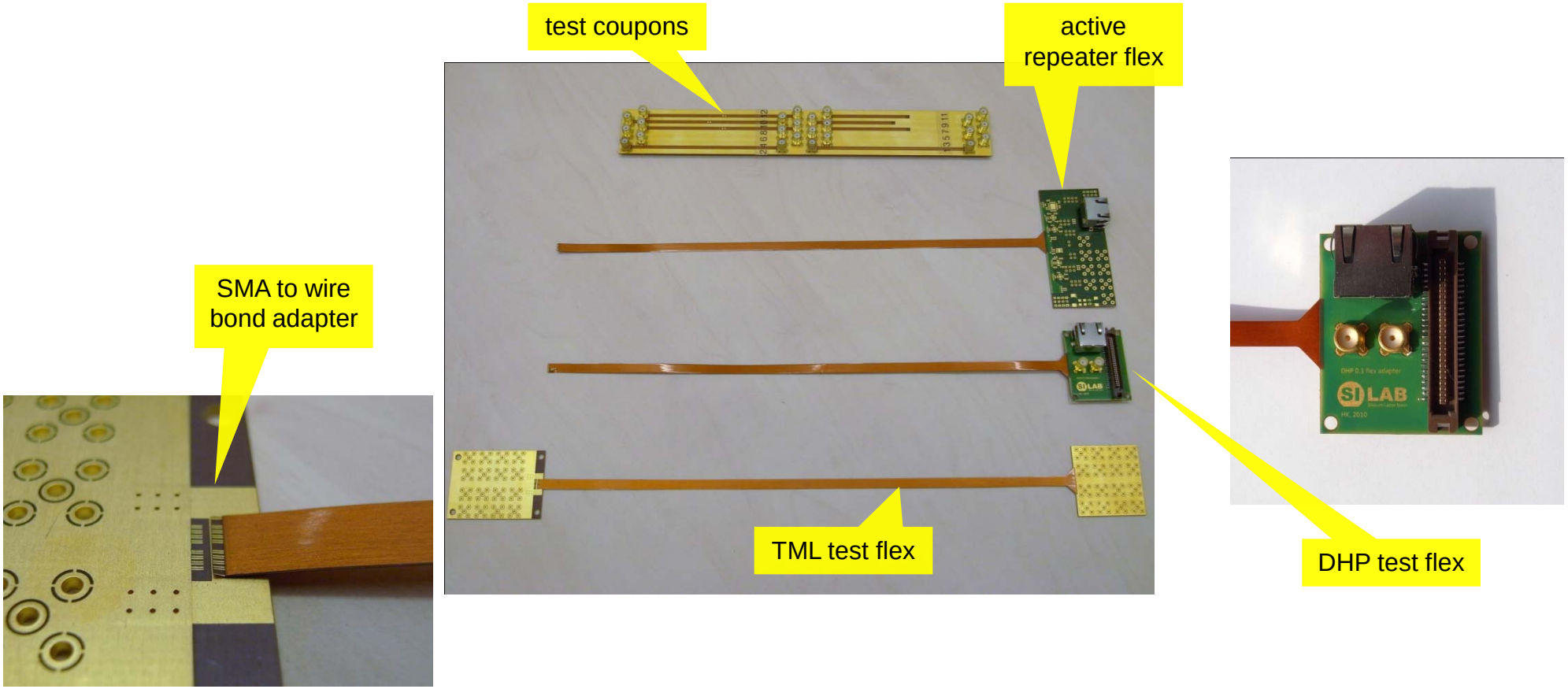
➔may have to stitch two kapton parts to extend the length > 40cm (production limit)



Flex Test Structures



Flex Test Structures



- first samples received beginning of September
- had to be reworked by the manufacturer (solder mask missing)
- TDR (time-domain reflectometry) measurements on the way

Outlook

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- understand TDR equipment & measurement results
  - use test structures with simple patterns (test coupons)
  - compare with simulation
- measure the **line impedance and damping** for different TML configurations
  - TML test structures with differential strip-lines, varying linewidth w = 60, 65, 75, 80, 85, 90, 95, 100µm, spacing s= 100µm
- measure **signal integrity** with ideal driver and with DHP 0.1
  - special flex to be used with DHP 0.1 test system
  - allows to test 30 cm flex-kapton + arbitrary (O(m)) length of coax or TWP cable.

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backup

Data Rates (per half module)

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- raw data rate: **10.24 Gpixel/sec** (1024 pixel columns x 10 MHz row rate)
- Simple data format:
  16 bit add + 8 bit ADC data **= 24 bit/hit**
- hit pairing (one address per two pixel cluster):
  16 bit add + 8 bit ADC data1 + 8 bit ADC data2 + 1 bit pos **= 33 bit/hit pair**
  (→ 32 bit with red. ADC resolution)
  data reduction factor: 2/3 – 4/3, depending on cluster size distribution
- trigger data reduction factor: 5.5 for 10 kHz trigger rate, 2.2 for 30 kHz (simplified assumption of Possonian trigger distribution)
- Usable link bandwidth: ~5 Gbps (4 x 1.55Gbps – framing/coding overhead)

occupancy (hit pixels)	***hit pixel rate***	***un-triggered data rate***		***triggered data rate (no hit pairing)***	
		24 bit/pixel	***32 bit/hit pair***	***10 kHz***	***30 kHz***
1%	100 Mpixel/sec	2.4 Gbps	1.6 – 3.2 Gbps	0.44 Gbps	1.1 Gbps
2%	200 Mpixel/sec	4.8 Gbps	3.2 – 6.4 Gbps	0.87 Gbps	2.2 Gbps
4%	400 Mpixel/sec	9.6 Gbps	6.4 – 12.8 Gbps	1.7 Gbps	4.4 Gbps

Event size (per half module)

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- pixels per half module: **256 kpixel** (1024 pixel columns x 250 pixel rows)

event size per frame:

occupancy	***# hit pixels***	***event size***	
		24 bit/pixel	***32 bit/hit pair***
1%	2.56 kpixel	7.68 kByte	5.12 – 10.24 kByte
2%	5.12 kpixel	15.36 kByte	10.24 – 20.48 kByte
4%	10.24 kpixel	30.72 kByte	20.48 – 40.96 kByte

Signal & Power lines

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- Digital signals between DHH and DEPFET module (DHP)

Signal name	Type	Description	Comment
GCK	LVDS in	system clock = 1/8 rowClk (~100 MHz)	generated from RF clock F0 adjusted by additional factor on the DHH
FCK	LVDS in	99.2 kHz frame clock	synchronous to the beam gap
TRG	LVDS in	trigger	10-30 kHz
TMS	LVDS in	JTAG mode select	
TCK	LVDS in	JTAG clock	
TDI	LVDS in	JTAG data in	
TDO	LVDS out	JTAG data out	
RST	LVDS in	reset	for all chips? polarity?!
DO[3:0]	CML out	DHP data out	one per chip

1.25 Gbps

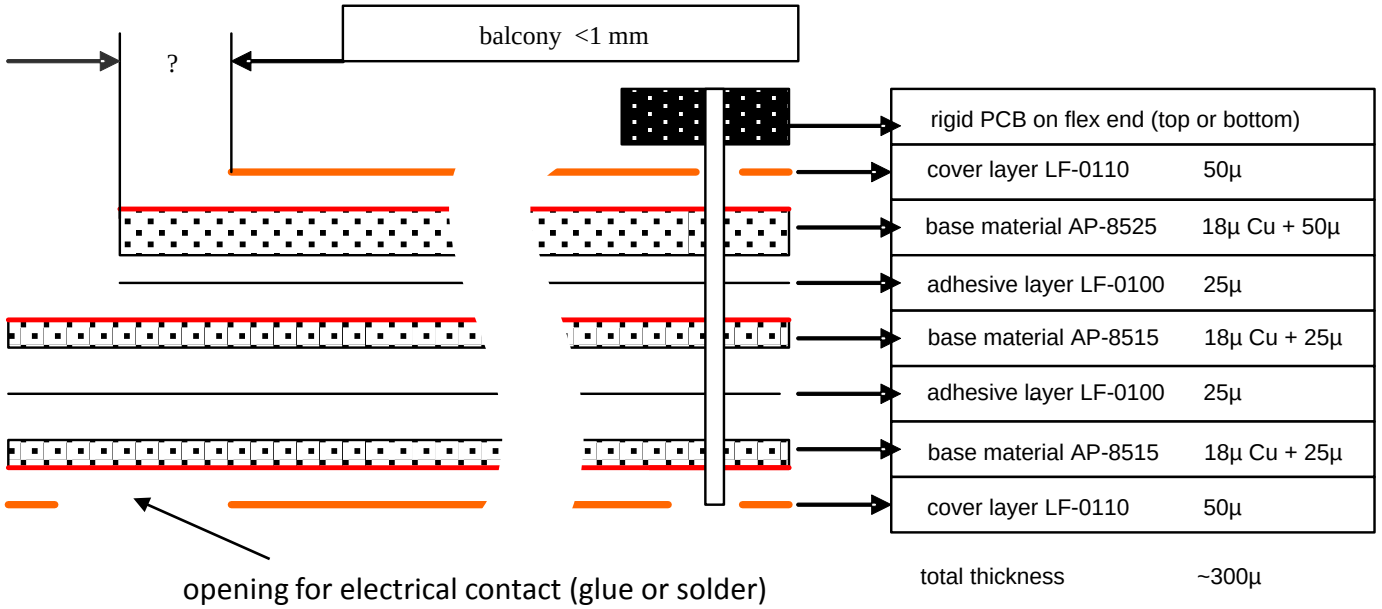
- Power lines
  - DCD (3x analog + digital)
  - DHP (digital IO + core)
  - Switcher (4x analog + digital)
  - DEPFET bias (5x)

Power / bias lines

	name	type	voltage [V]	current [mA]	comment	diff.	thin	thick	width [mm]	voltage drop [V]
power supplies	VDDA	DCD analog	1,8	2300	sense line		1	6	3,48	0,35
DCD	VDDD	DCD digital	1,8	800	sense line				1,21	0,35
	REFIN	DCD analog ref	1,1	100	sense line		1	2	0,15	0,35
	DGND	common digital ground	0	800	common					
	AGND	analog ground	0	2300	sense line		1	6	3,48	0,35
	AMPLOW		0,35	1500	sense line		1	4	2,27	0,35
DHP	VDDIO	DHP IO rail	1,8	100	sense line		1	2	0,15	0,35
	VDDC	DHP core	1,2	500	sense line		1	5	0,76	0,35
	DGND	digital ground	0	600	common					
SWITCHER	VDDS	digital supply	3,3	4				1	0,01	0,35
	DGND	digital ground	0	4	common					
	VJTAG	JTAG IO rail	1,8	4	common					
common	VDDIO	common IO rail + DCD digital	1,8	904	sense line		1	4	1,37	0,35
	DGND	digital ground	0	1404	sense line		1	6	2,12	0,35
bias voltages	Vclear_on	clear on	~17	30			1			
	Vclear_off	clear off	~8	30			1			
	Vgate_on	gate on	~4	30			1			
	Vgate_off	gate off	~13	30			1			
	Vsource	source	7	100			1	1		
	Vccg	common clear gate	~7	0			1			
	Vbulk	bulk	~17	0			1			
	Vguard	gurad ring (edge)	?	0			1			
	Vbias	backplane	-20	0			1			
					signal pins:	24	17	37		
		power current		4956	total sum:			78	15,00	

- min. copper width (17µm copper) for ΔU < 0.4 V (10A, 50 cm length): 15 mm
- total flex width (including digital, bias and sense lines): ~24 mm ➔ 3 layer flex, 6 mm wide
- still some safety factor if 35µm instead of 18µm copper for power layers would be used

Layer stackup for test flex

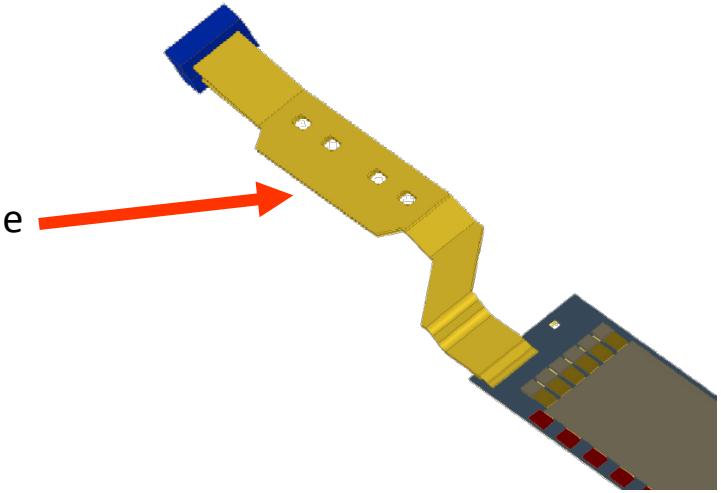


- design rules (for 18µm copper):
  - 100µm line width & spacing (80µ line width?)
  - 200µm/400µm via hole/outer ring diameter
  - dielectric constant: 3.4 – 3.6 for all isolation layers
- 75µm dielectric above and below the (inner) signal layer
- bottom layer “upside-down” for glue attach area

Signal integrity simulation - outlook

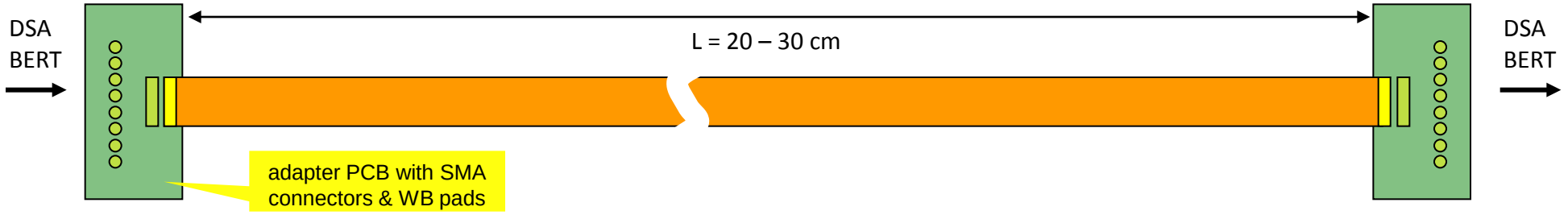
work in progress:

- define simulation model for DHP CML driver
- layer stackup for routing on silicon substrate (2 or 3 metal layers)
- simulate different receiver components
  - repeater ICs
  - TWP or coax cables (for passive patch panel option)
- board level simulation
  - import flex design and re-simulate
  - will be important for designs with complex flex outline



Prototype flex designs variants

A) diff. TML pairs with line width / spacing variations, WB balcony on both ends



B) diff. TML pairs, patch panel on one side with different board equalizer ICs (repeaters) + connectors

C) similar to B) but width different patch panel & flex layout for DHP 0.1 test system