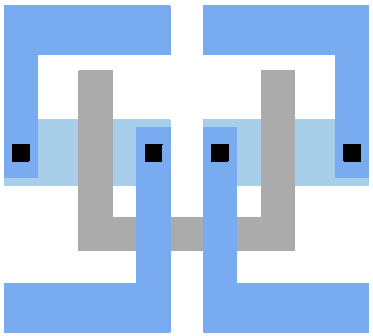
UNIVERSITÄT
HEIDELBERG

Switcher-B



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5th International Workshop on DEPFET Detectors

and Applications

Valencia

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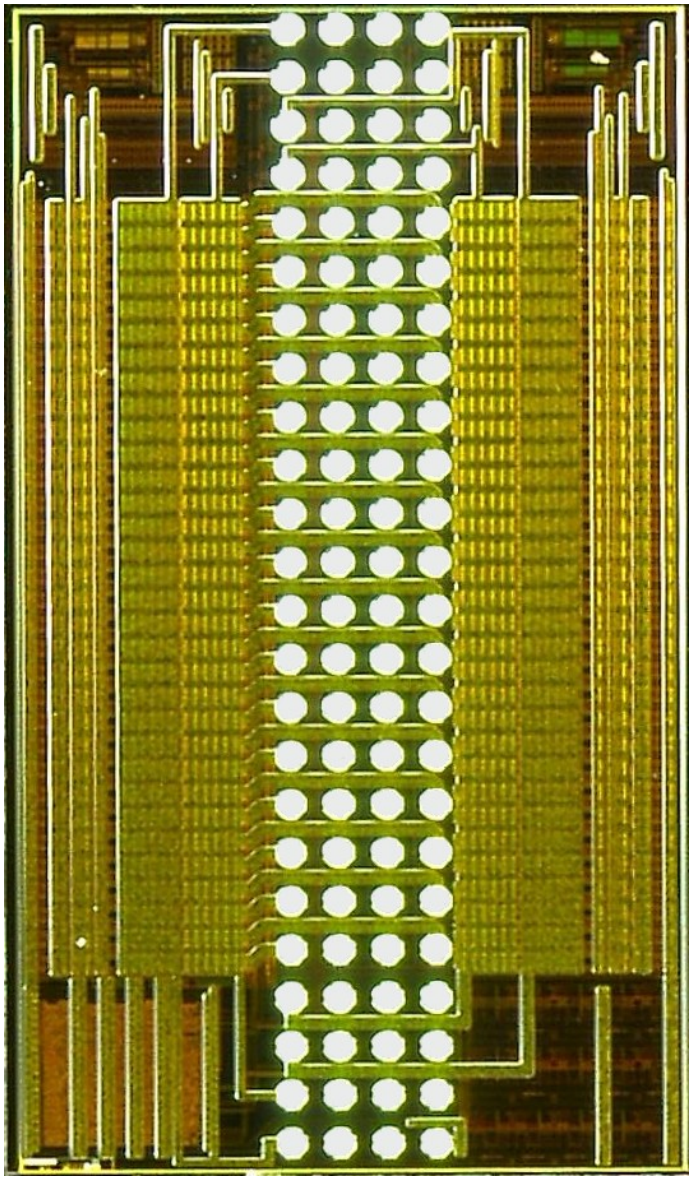
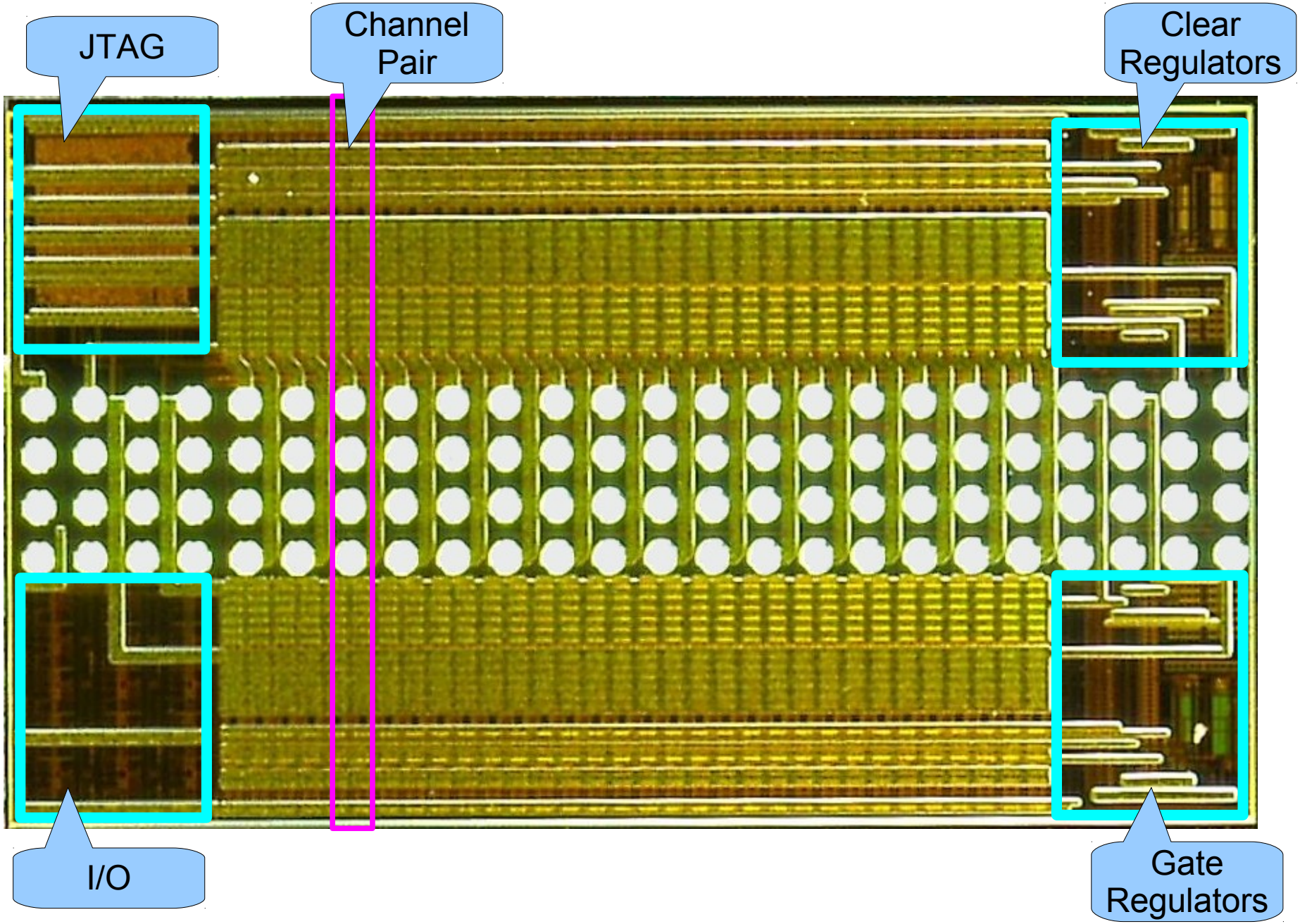
Overview

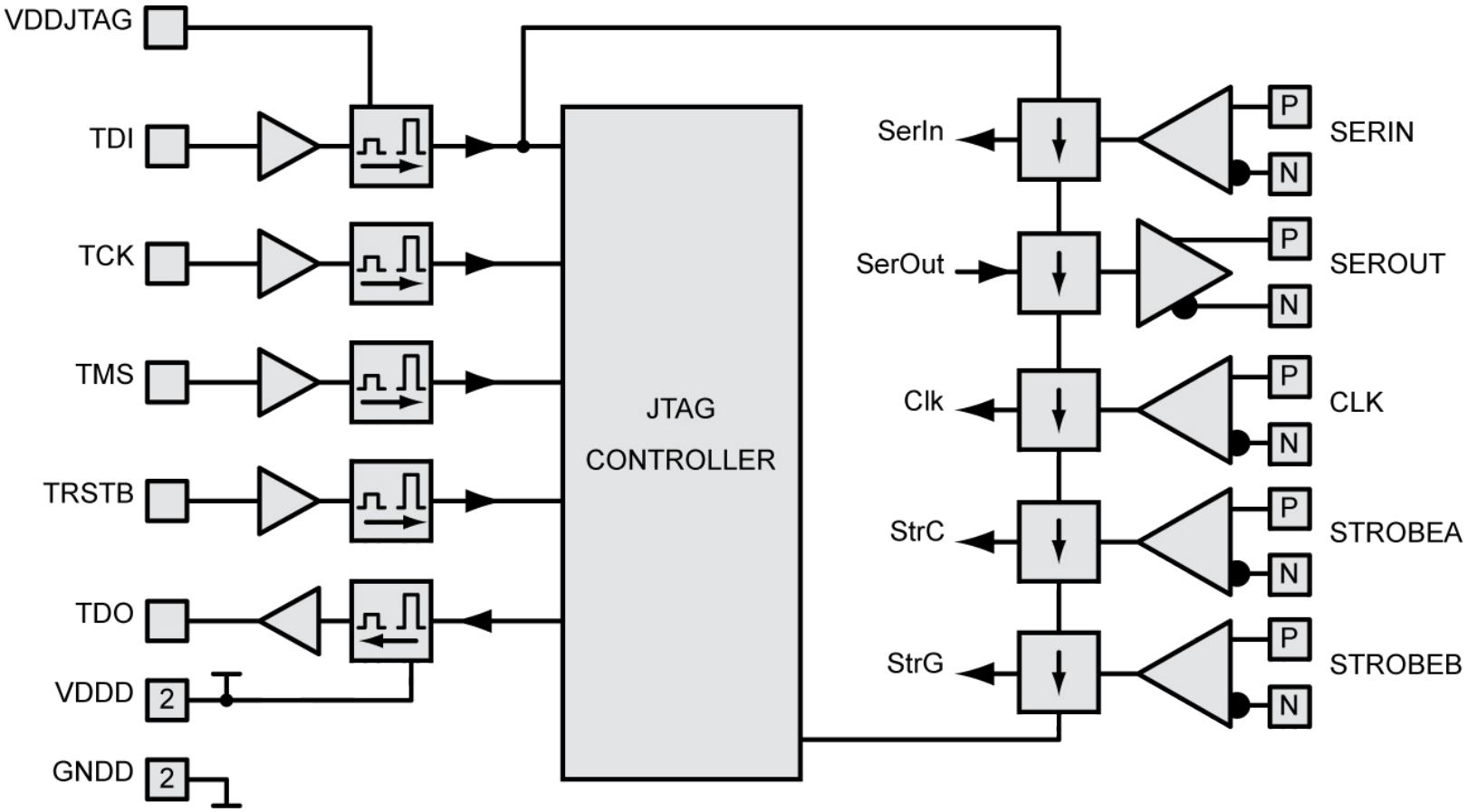
- 32 rows
  - each row with clear and gate output
  - shift register to enable rows (LVDS)
  - gate and clear strobe signals (LVDS)
  - sleep and boost states for power saving
- AMS H35B4 technology
- radiation hard design
- floating digital 3.3V supply
- JTAG slow control and boundary scan
  - 1.8V capable I/Os
- bump bond only
- designed size: 2100µm x 3600 µm
- measured size: 2170µm x 3660µm
- see Reference Manual for more details!



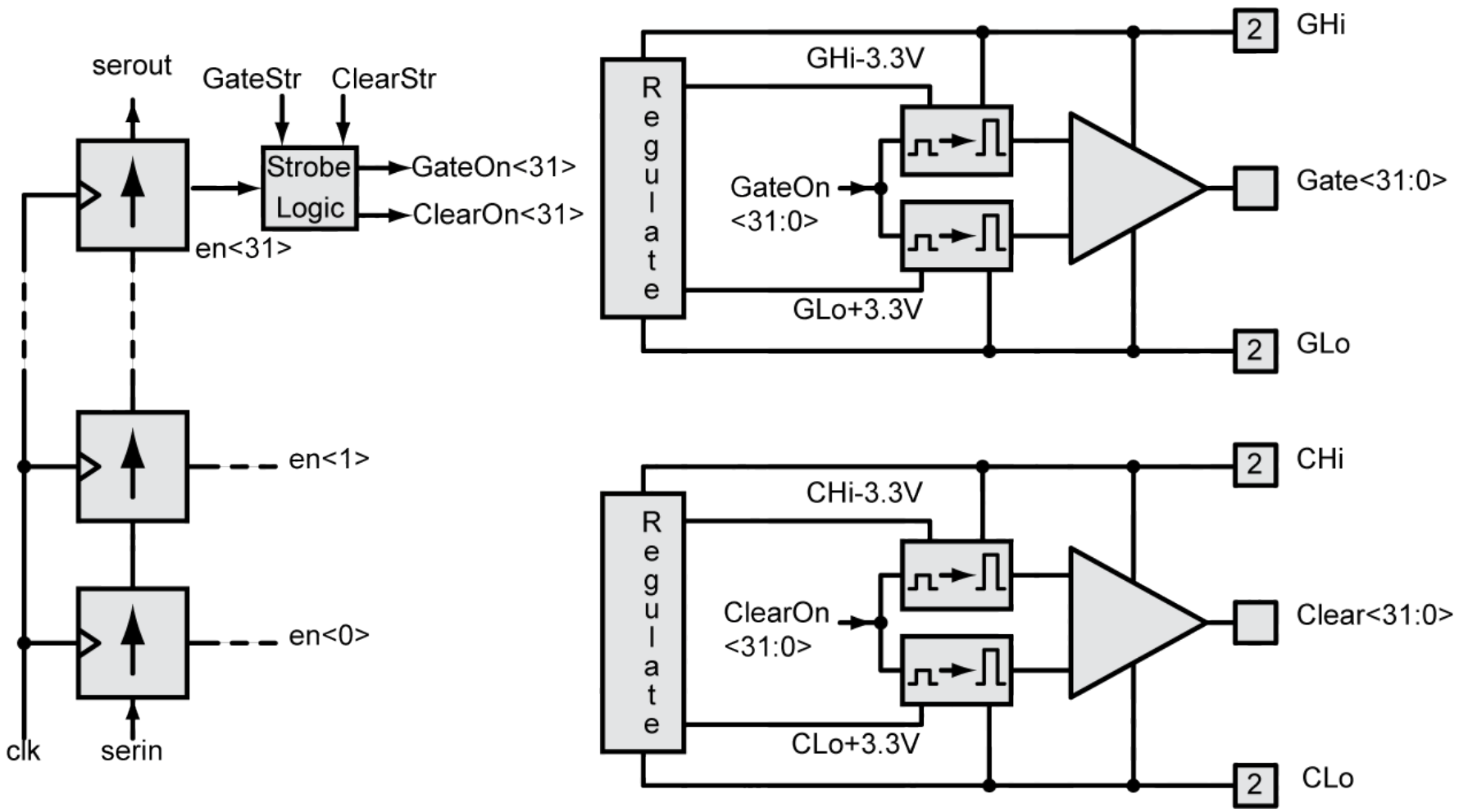
Chip Layout



Blockdiagram JTAG

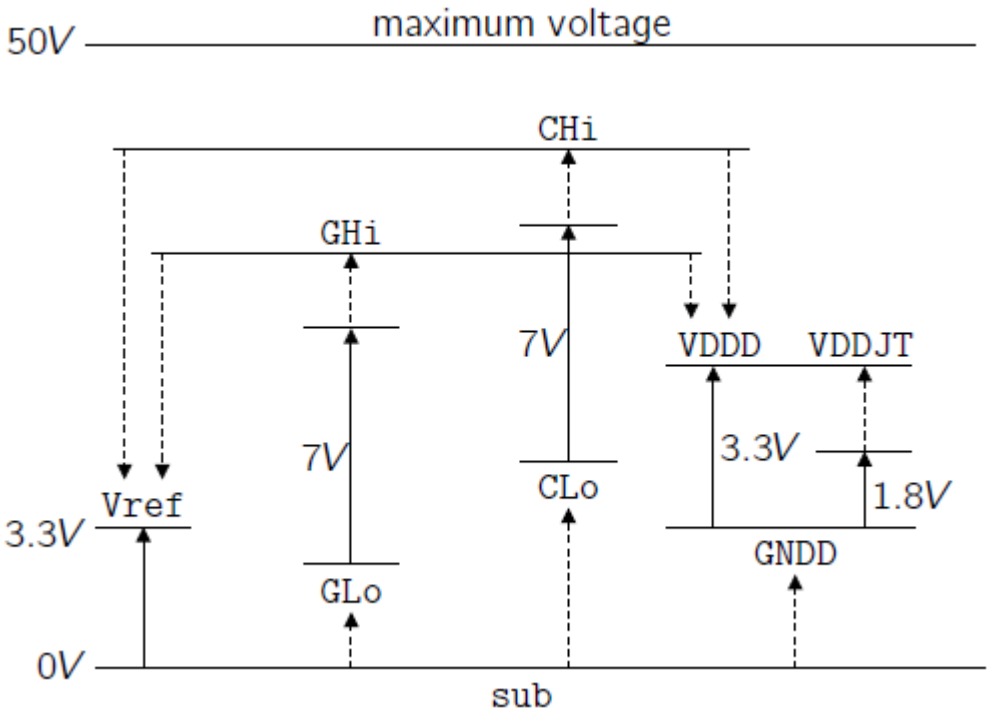


Blockdiagram Switches



Supply Voltages

- floating supplies
  - sub has to be the lowest voltage
  - any voltage must not exeed 30V relative to sub (50V not yet tested)
  - Vref has to be sub+3.3V
  - VDDD and VDDJT relative to GNDD
  - VDDJT supports from 1.8V to 3.3V supply (1.8V tested)
- measured power consumption
  - VDDD@12.5MHz: 4mA
  - GNDD@12.5MHz: -8mA
  - VDDJT: 60µA
  - Vref: 170µA
  - sub: 12µA



JTAG / Slow Control

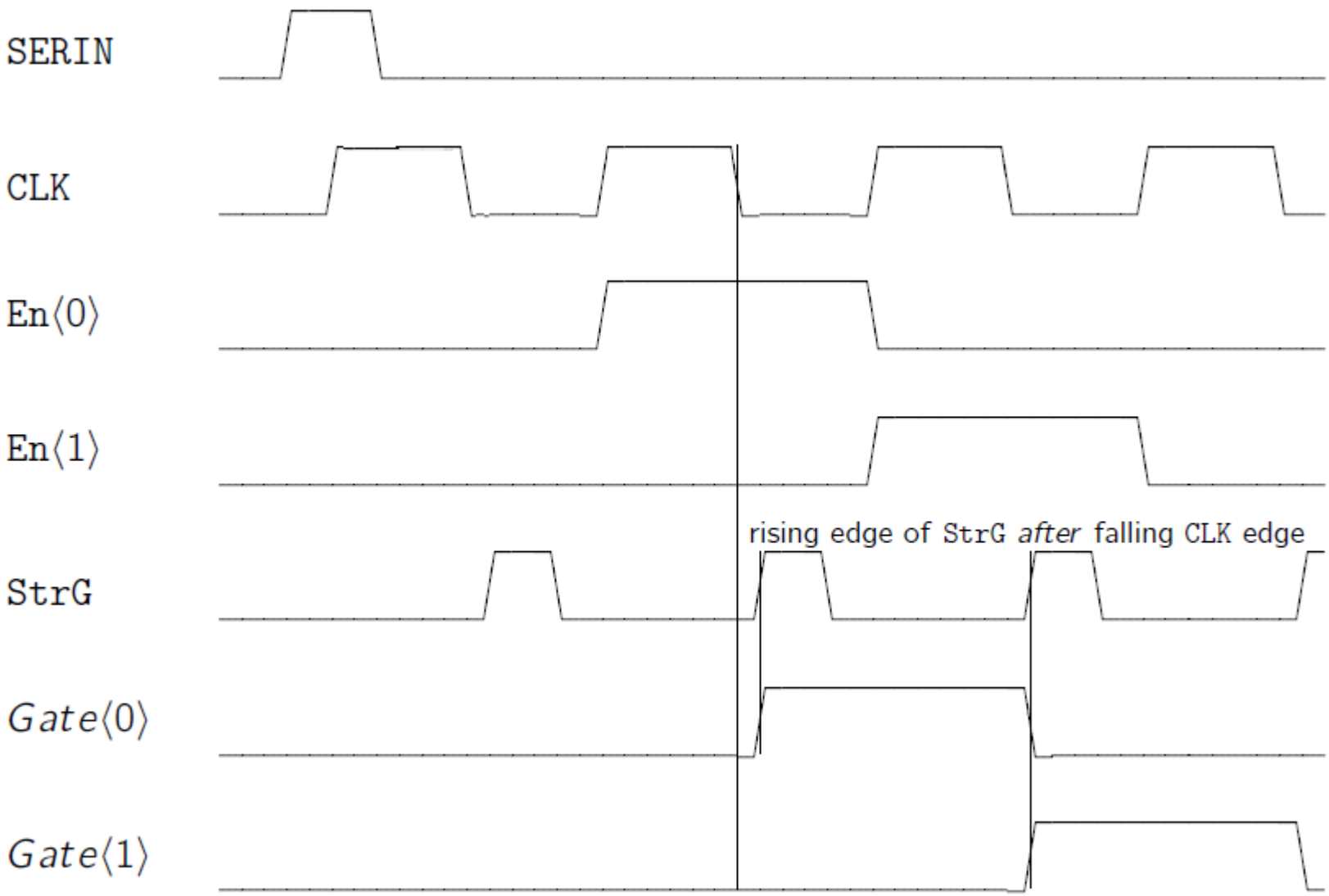
- Slow Control
  - Configuration Register
    - Bias Current setting for sleep and boost states of level shifters
    - reserved bits for features not implemented in this chip revision
  - majority voter
    - triple redundancy in configuration bits
    - register can be read back to check for SEU
- Boundary Scan
  - read value of input pads and set output pads
    - allows to check connectivity of bumps
  - read and set I/Os from and to logic core

- All features have been tested ok @ 1.8V I/O voltage

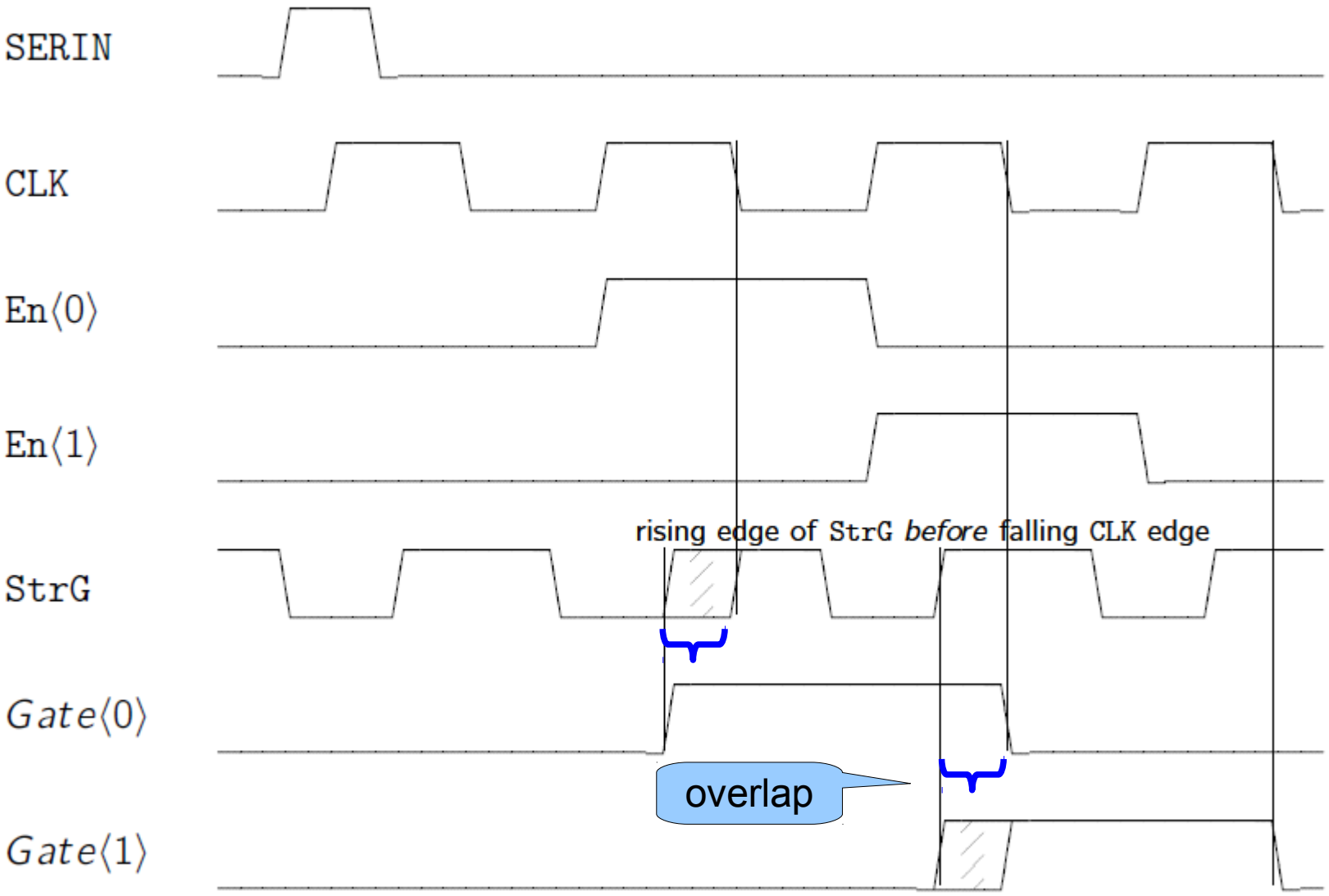
Strobe Logic

- The strobe logic allows 2 modes for gate outputs:
  - non-overlapping gate
  - overlapping gate
- controlled by timing of strobe signal relative to falling clk edge
  - strobe can only switch gate on
  - gate is switched off automatically when gate of next row is switched on
- row skip
  - omit strobe signal while keeping clk running
  - last active row stays active
- clear strobe
  - gate has to be switched on
  - full control of clear output: switch-on and switch-off

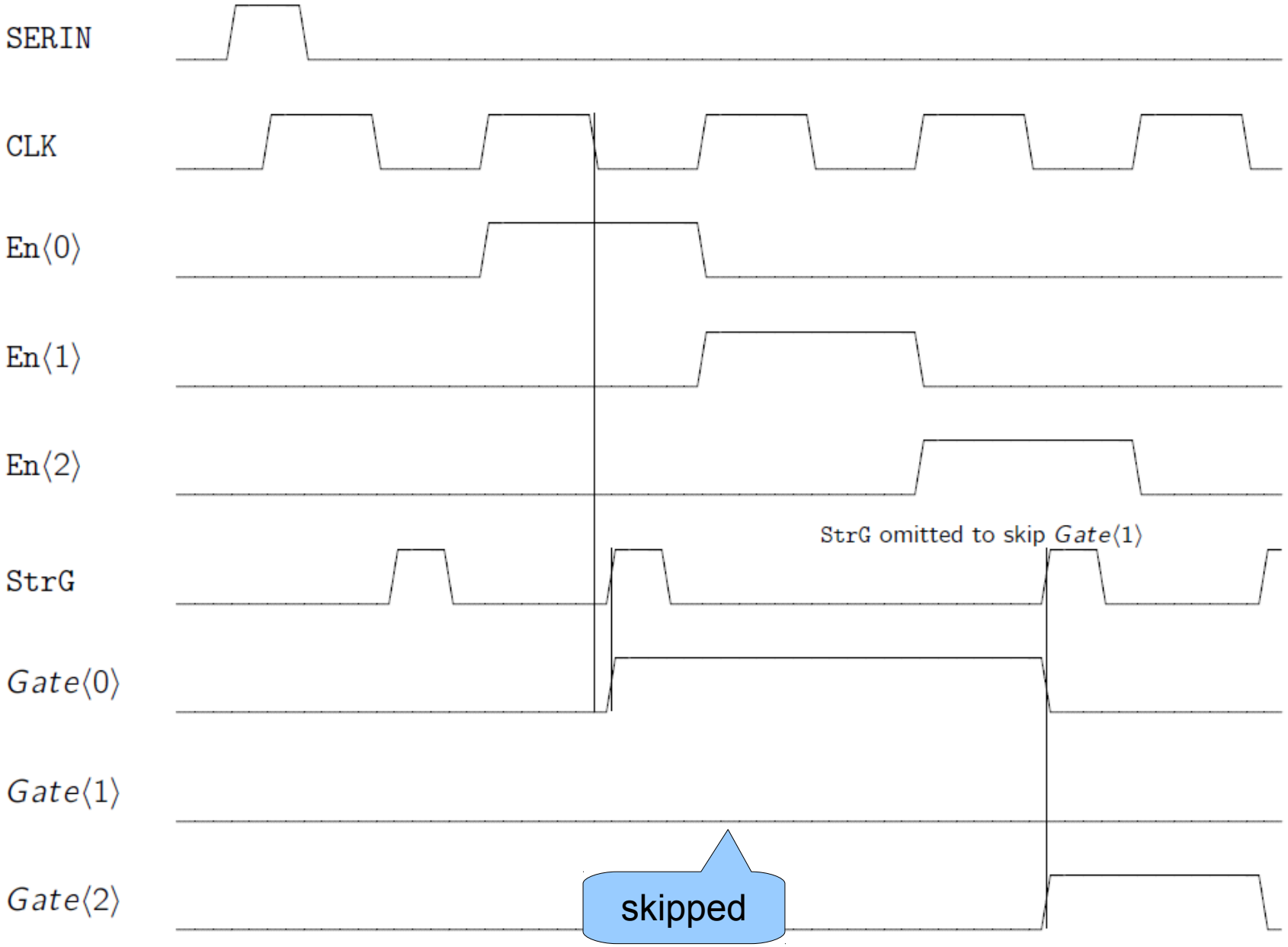
non-overlapping gate



overlapping gate

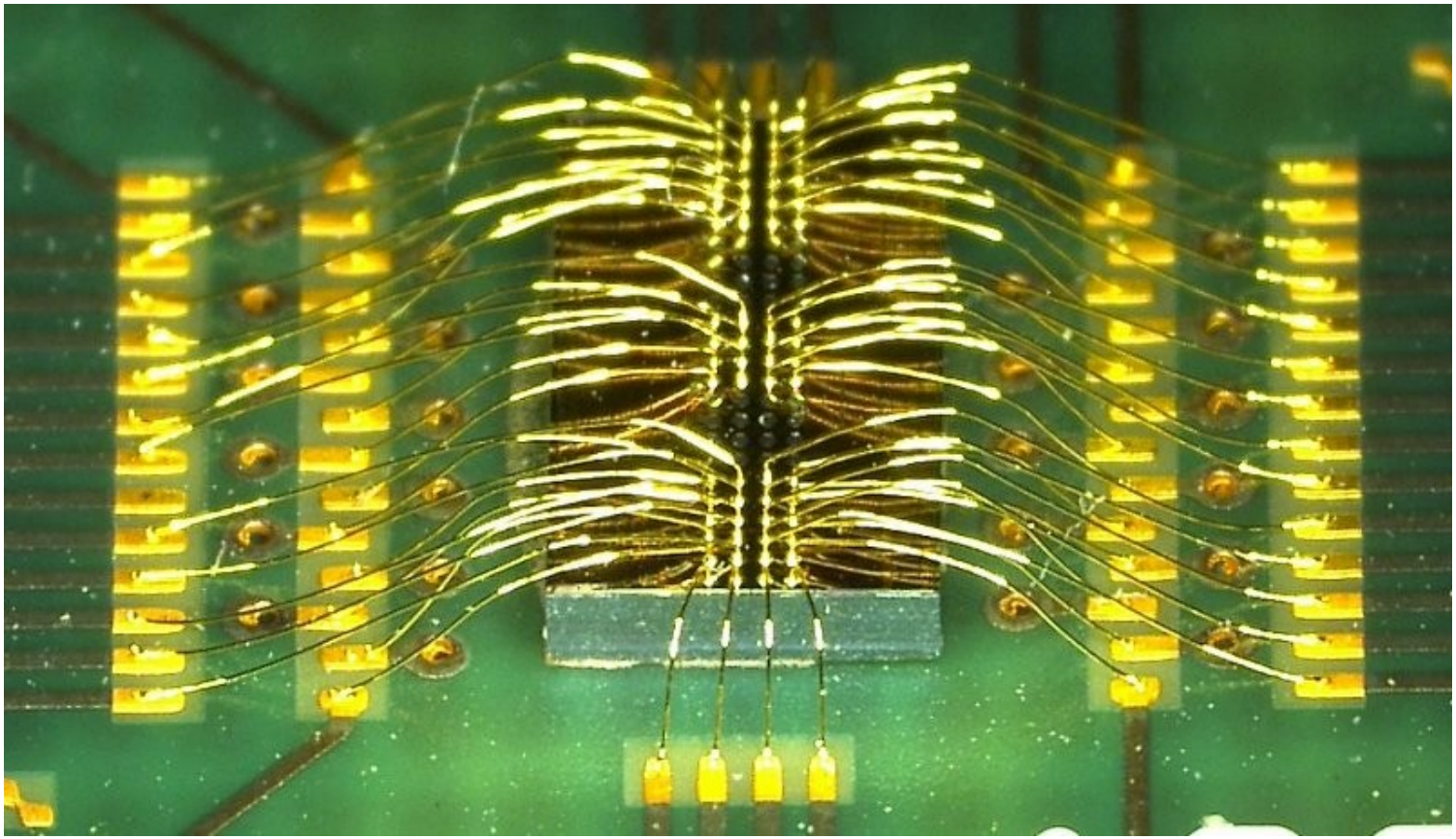


row skip

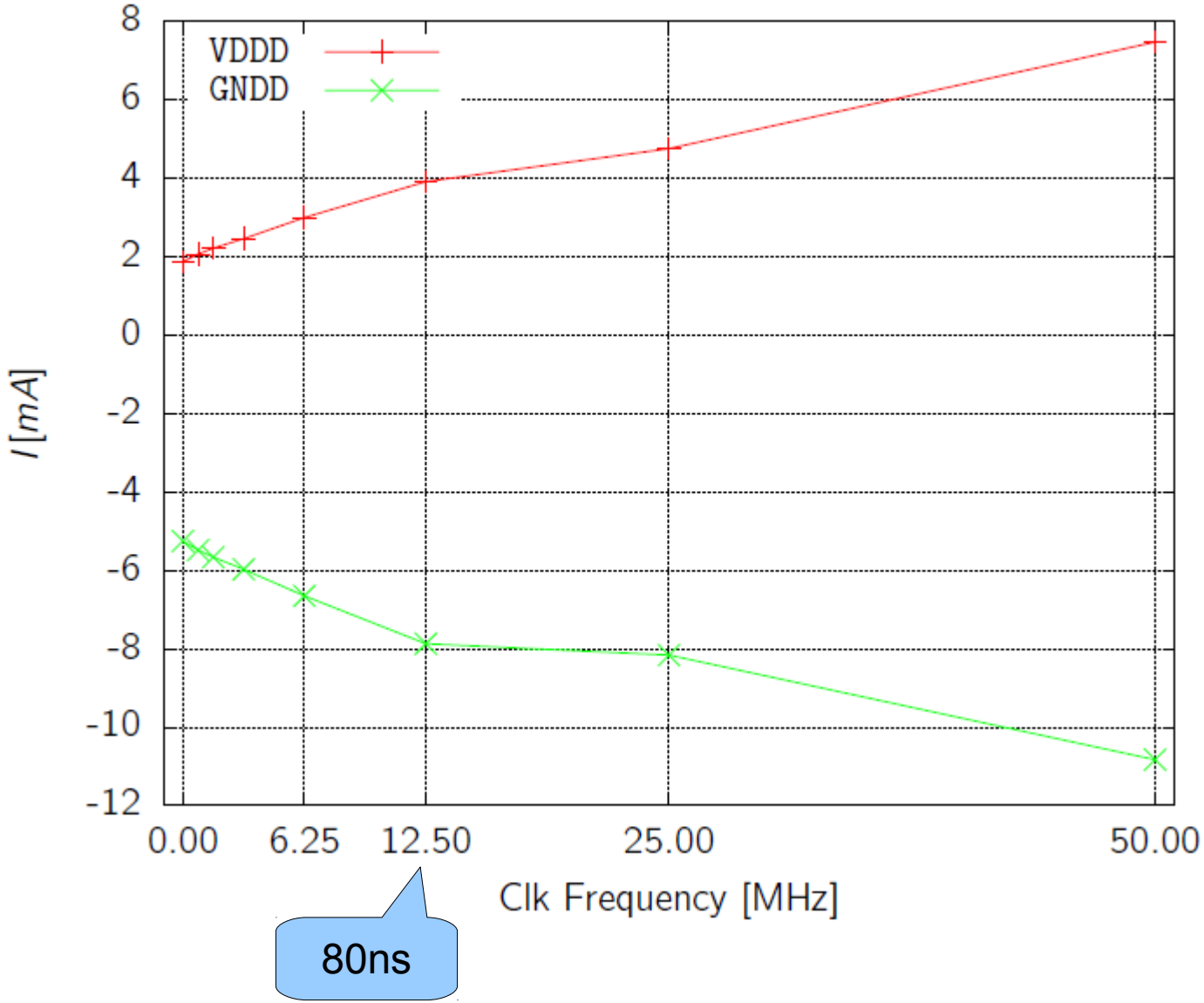

SERIN
CLK
En⟨0⟩
En⟨1⟩
En⟨2⟩
StrG omitted to skip Gate⟨1⟩
StrG
Gate⟨0⟩
Gate⟨1⟩
Gate⟨2⟩
skipped

Test PCB

- TestPCB for DCD-B and Switcher-B
- connects to FPGA board from Bonn
- Switcher-B wirebonding of I/O signals and some outputs (tricky!)
- load capacitors of 22pF, 47pF and 68pF

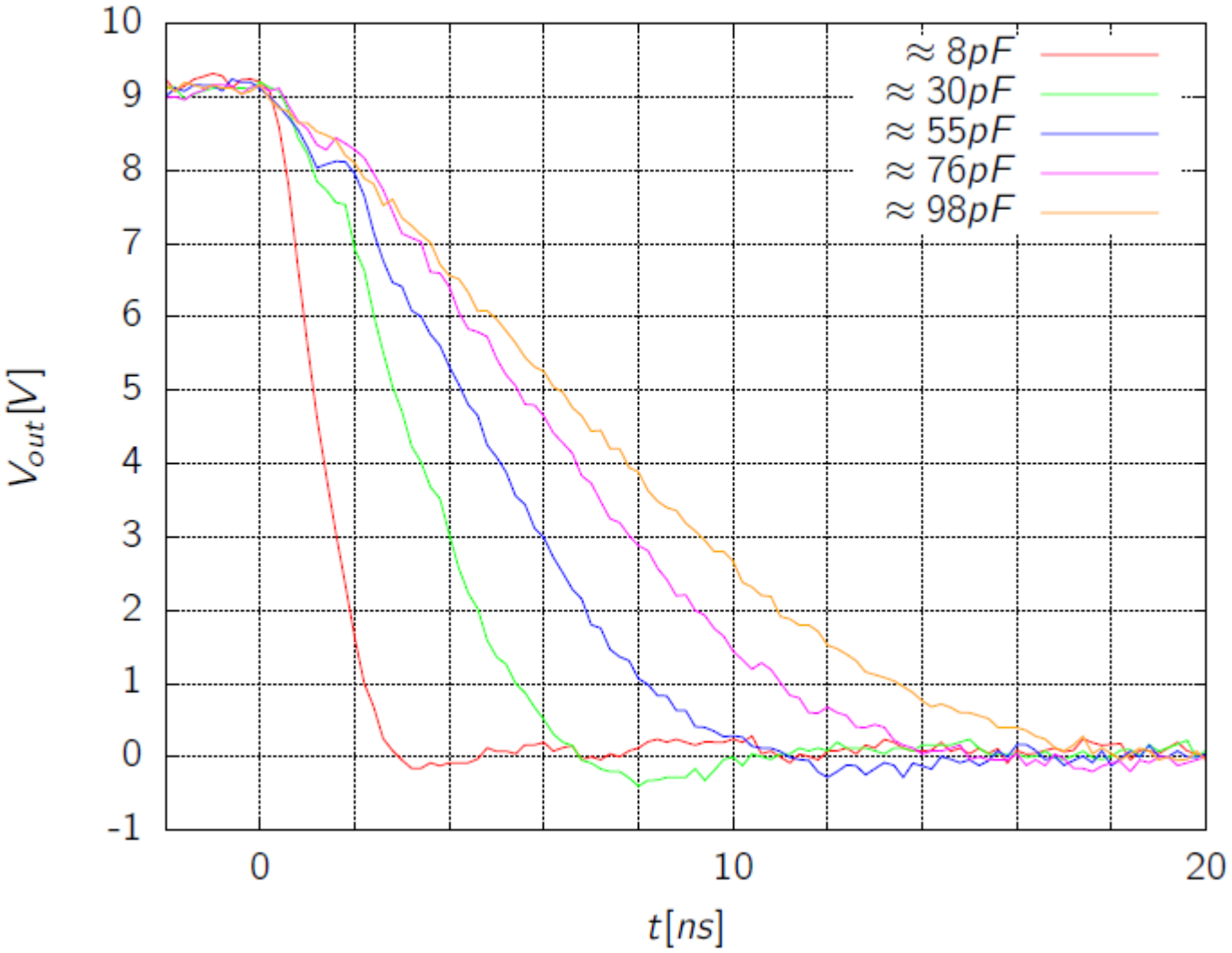


Measured current in digital supply



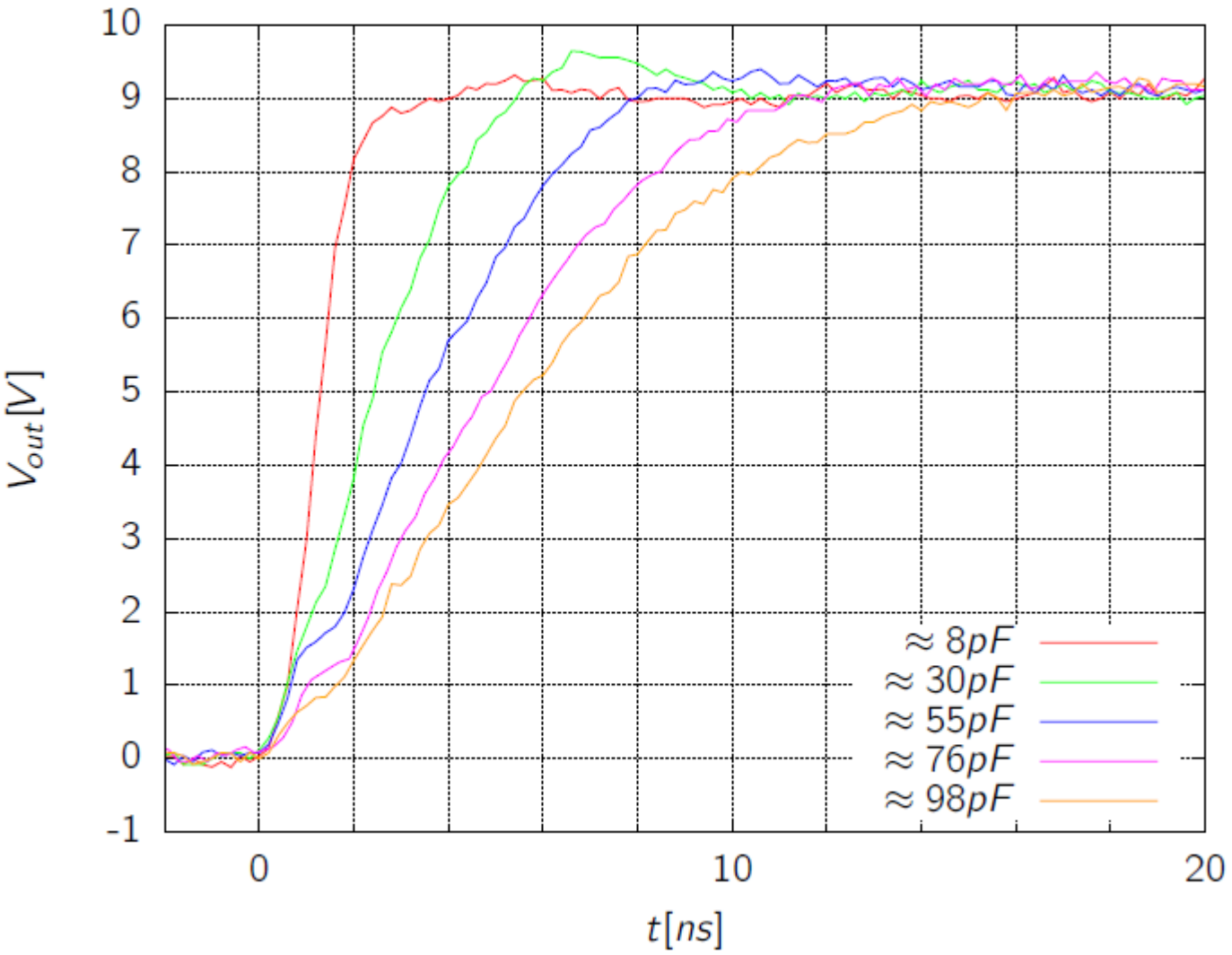
falling edge

- 9V swing
- 10%-90%
  - 8pF: 1.9ns
  - 30pF: 5.3ns
  - 55pF: 7.9ns
  - 76pF: 9.8ns
  - 98pF: 12.1ns

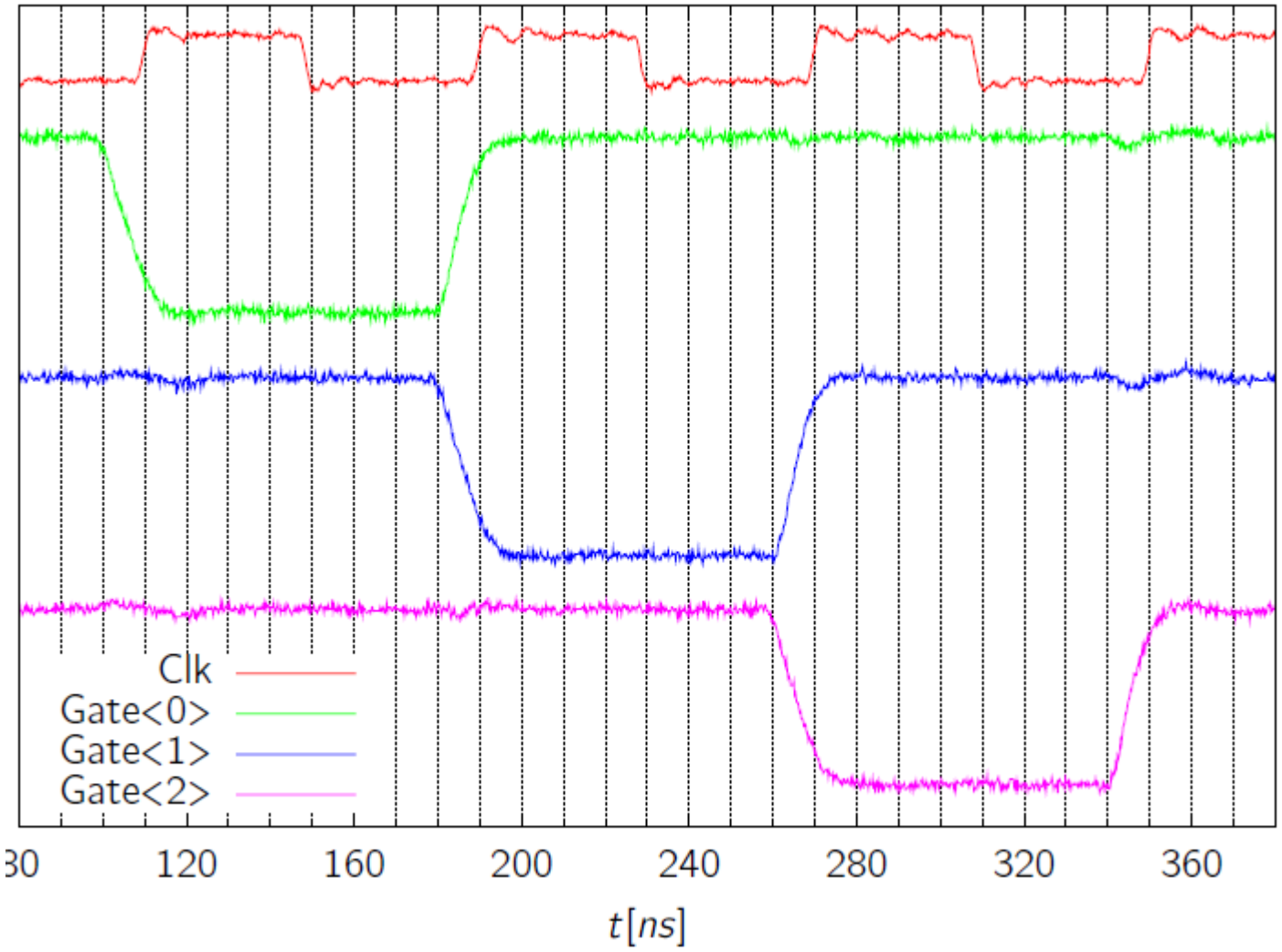


rising edge

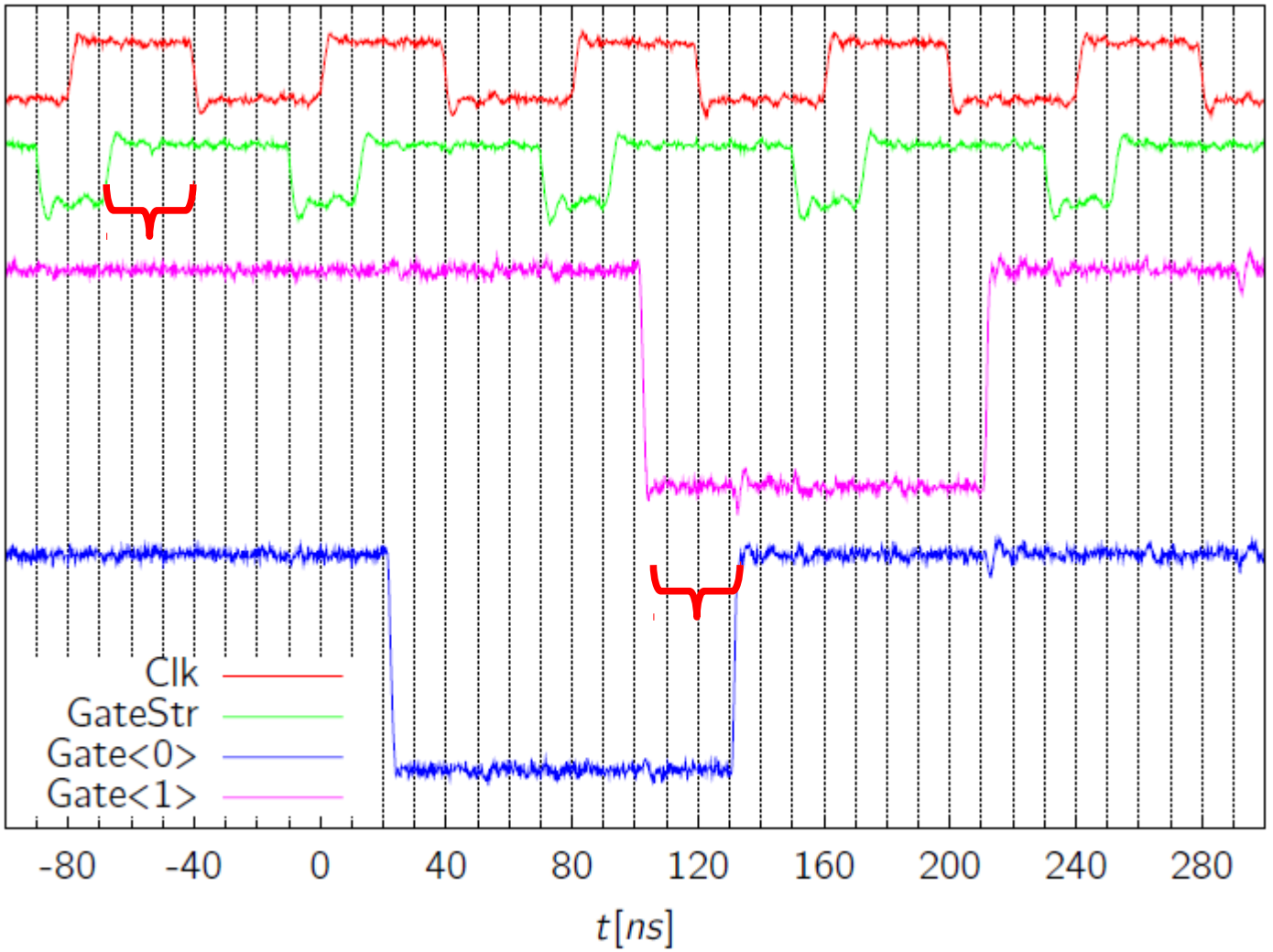
- 9V swing
- 10%-90%
  - 8pF: 1.9ns
  - 30pF: 5.1ns
  - 55pF: 7.8ns
  - 76pF: 9.8ns
  - 98pF: 12.6ns



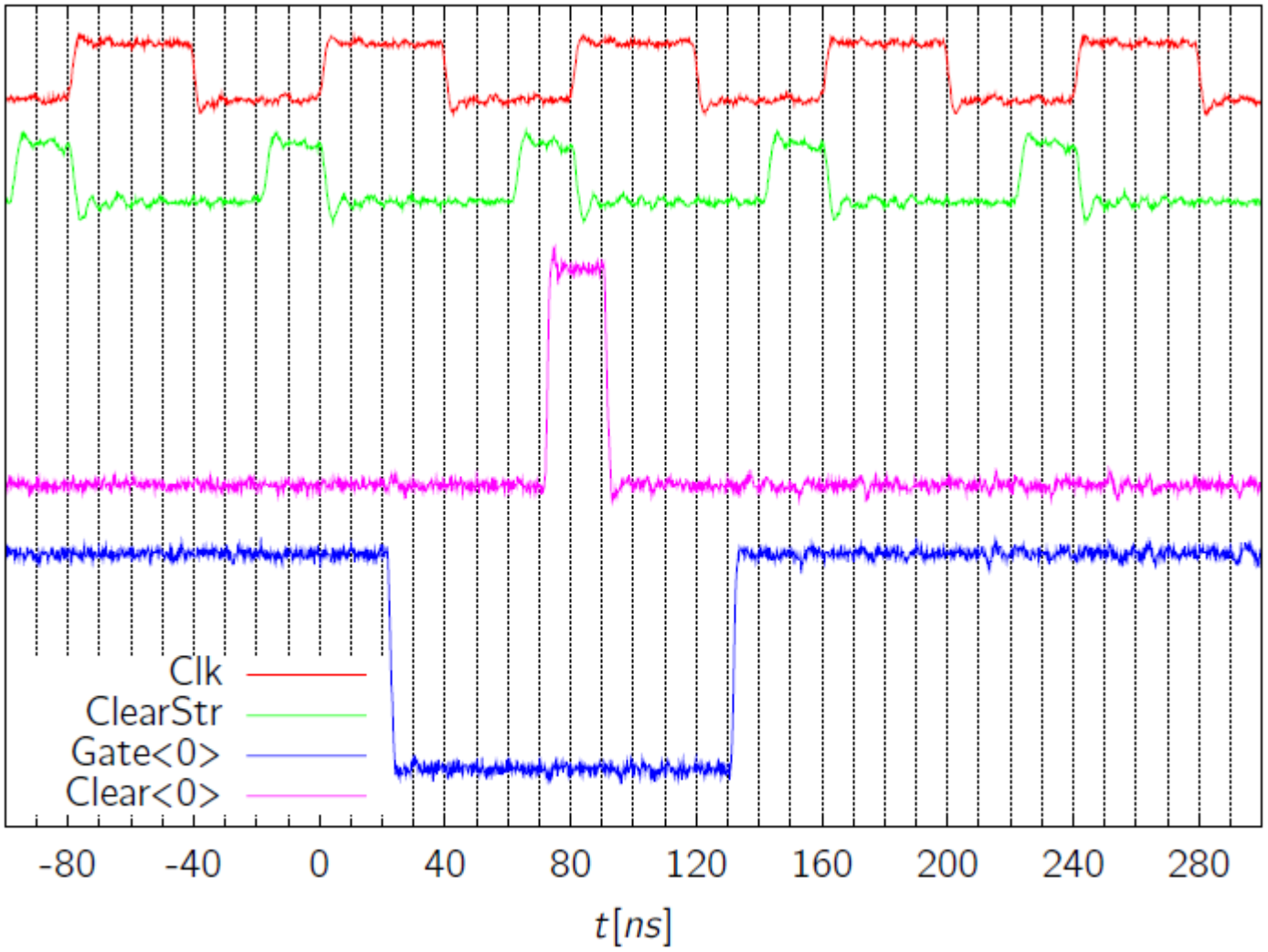
80ns row time, 98pF load



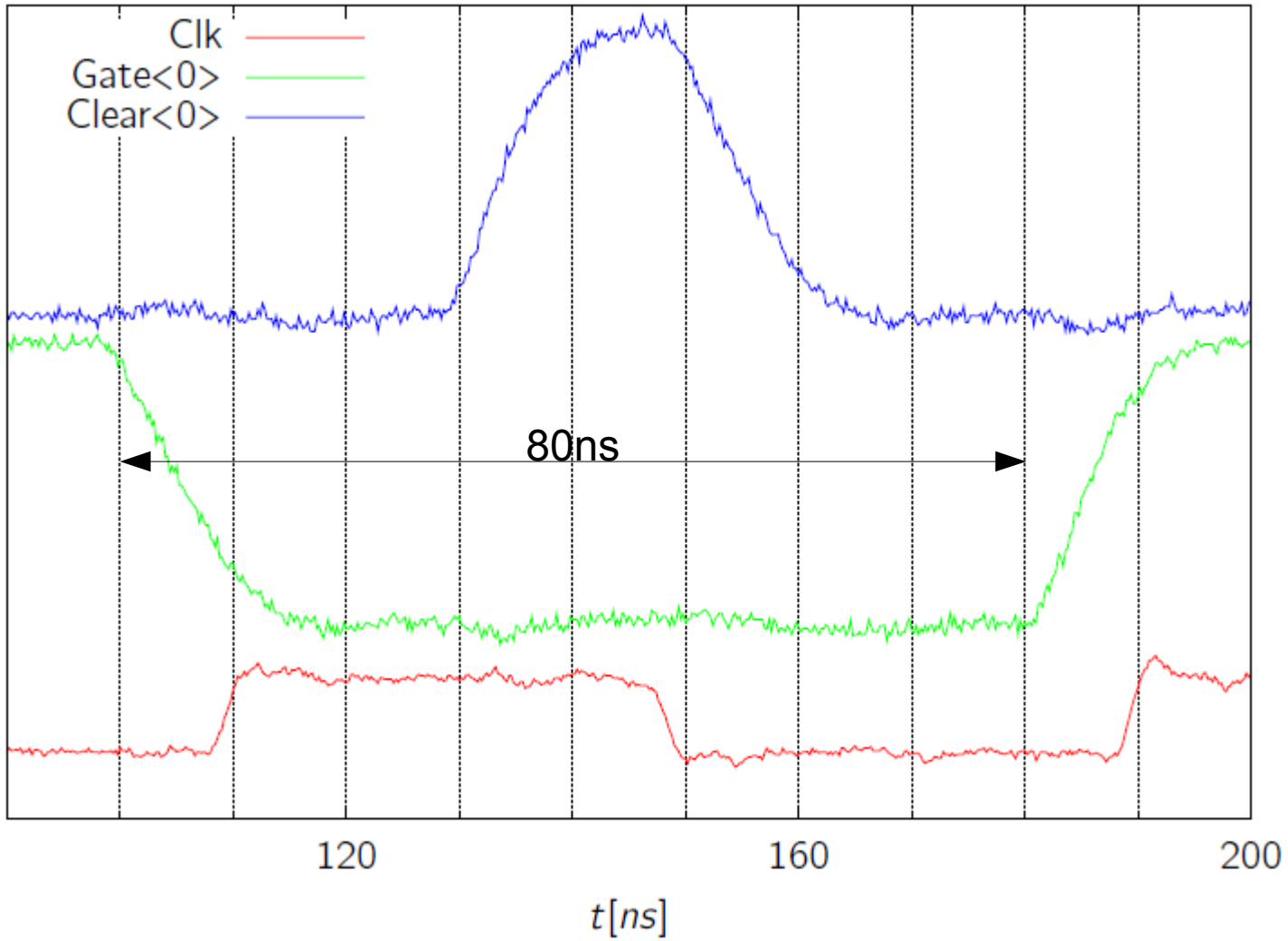
overlapping gates



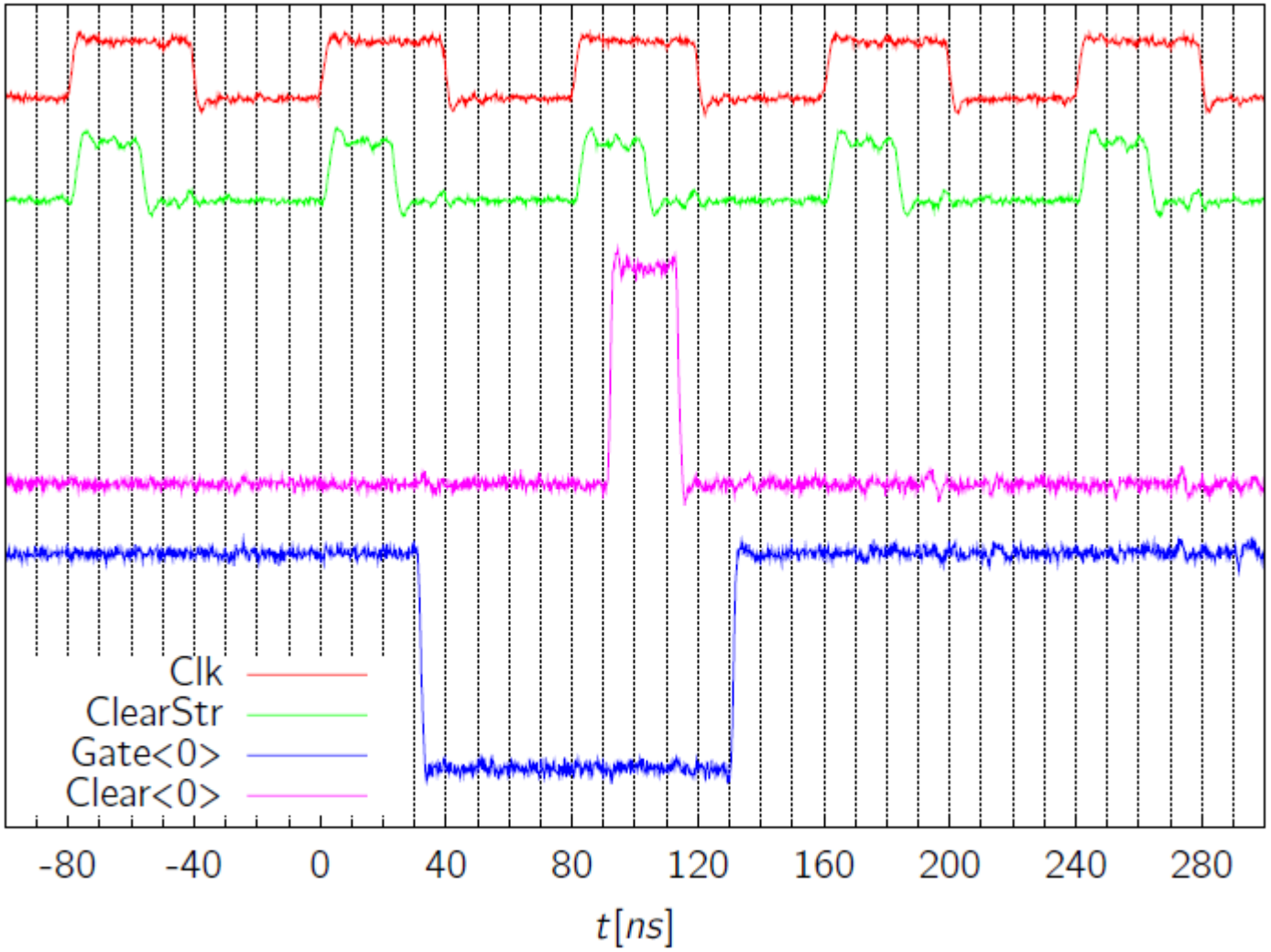
sample-clear-sample



sample-clear-sample 98pF



single sampling



Bias Settings

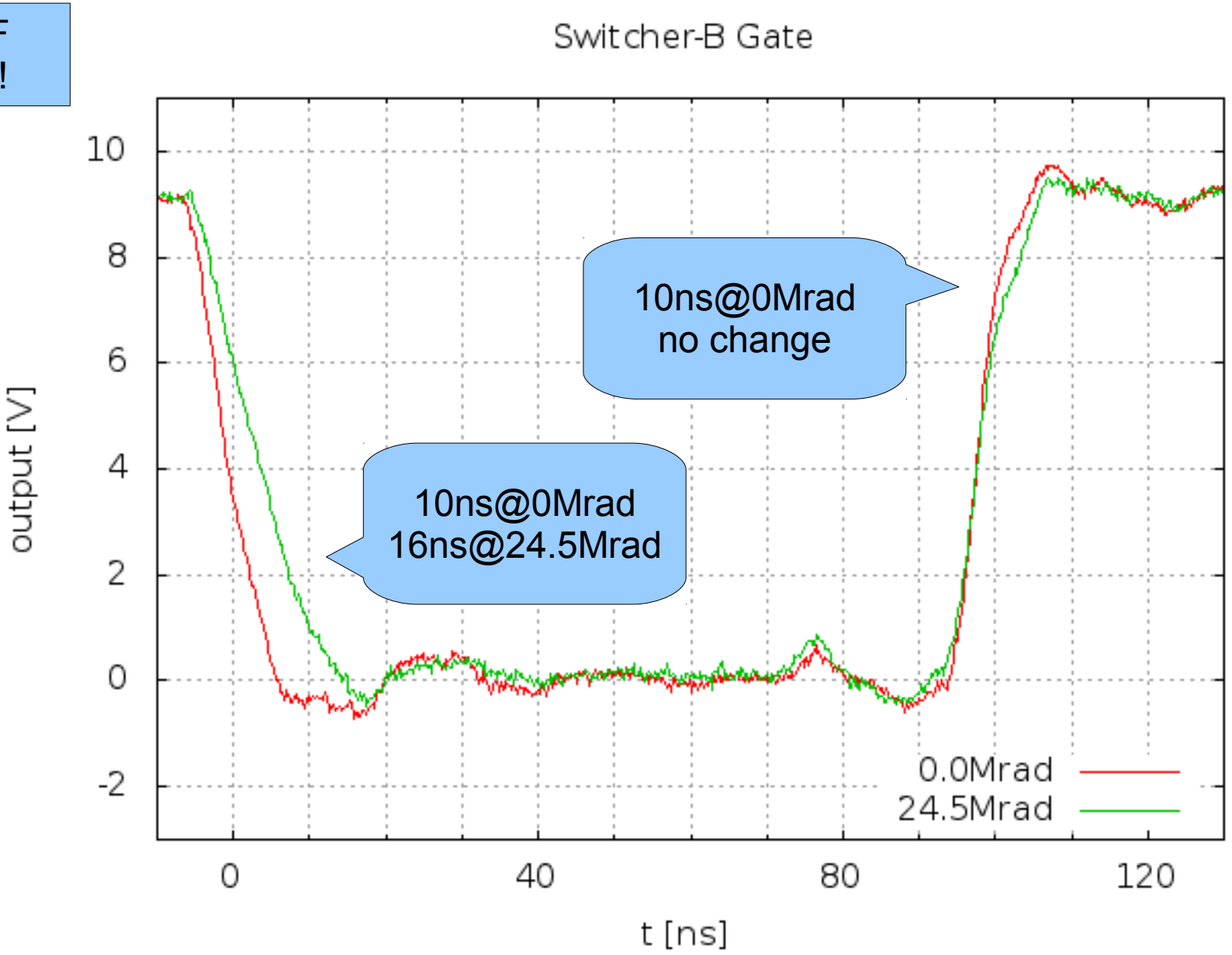
- set via JTAG
- delay between strobe signals and output
- influence on power consumption
- see manual for details

Irradiation

- Karlsruhe X-ray
  - 60kV; 33mA; Fe-filter; 115mm distance
  - 636krad/h
  - 24.5Mrad irradiated
- Switcher-B settings
  - 12.5MHz row frequency
  - VDDD=3.3V
  - VDDJTAG=1.8V
  - Ibias=6.6µA
  - IbiasBoost=210µA
  - GateHi=ClearHi=9V
  - Load Capacity=76pF

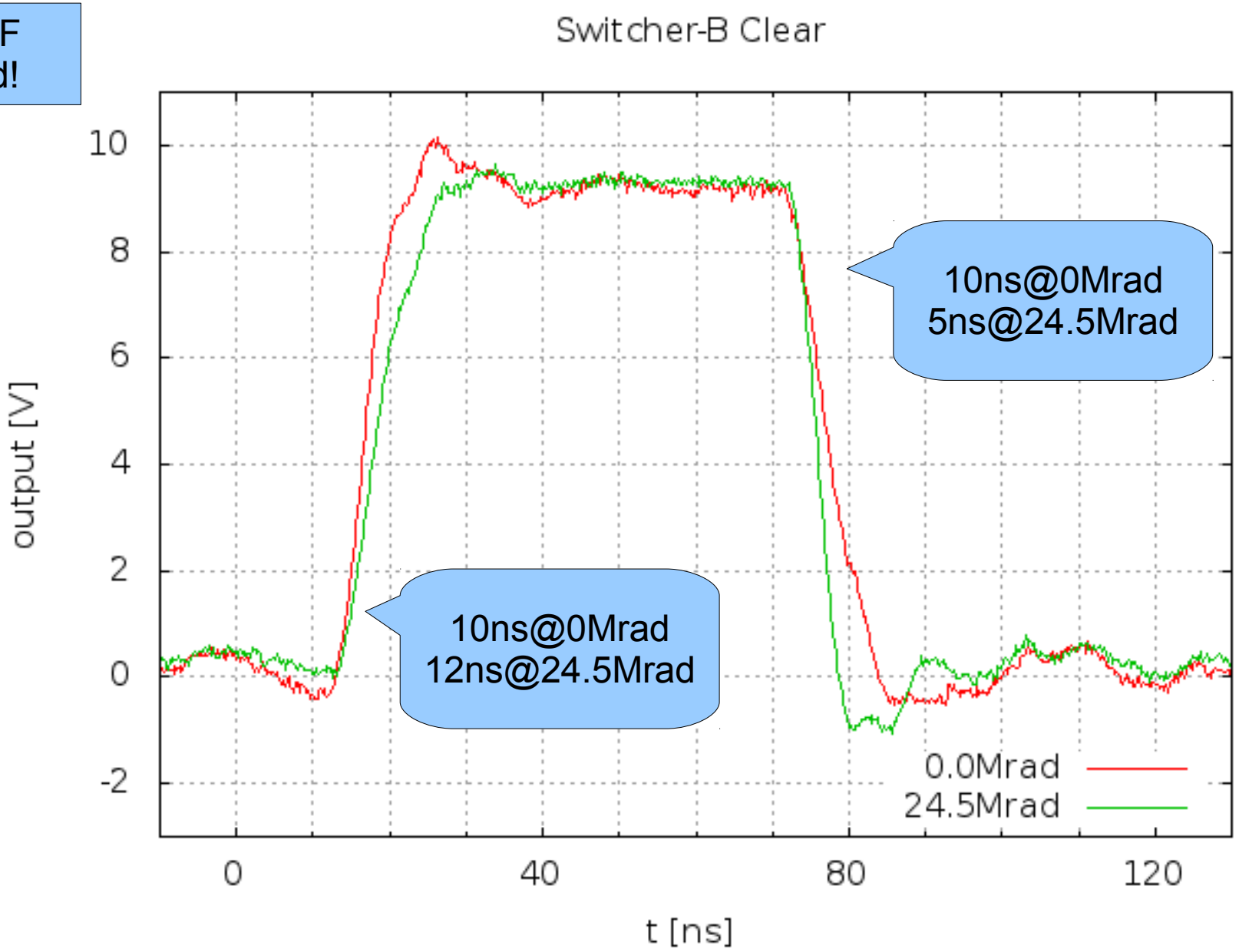
Gate Output

76pF load!



Clear Output

76pF load!



Power Consumption

- running at 12.5MHz (80ns)
- Irradiation:
  - within first 500krad
    - VDDD: **5mA** → 35mA
    - Vgate+Vclear: **13mA** → 26mA
  - within next 6Mrad back to normal
  - 24.5Mrad
    - VDDD: **4mA**
    - Vgate+Vclear: **11mA**

Conclusion

- Switcher-B working at 80ns row time
- JTAG slow control & boundary scan working
- Chip works after 24.5Mrad irradiation

- Next chip revision
  - add onchip termination resistors
  - adjustable current in LVDS
  - real LVDS output
  - decoupling capacitors to Vsource

- See Reference Manual for details
  - will be released next week

Thank you!