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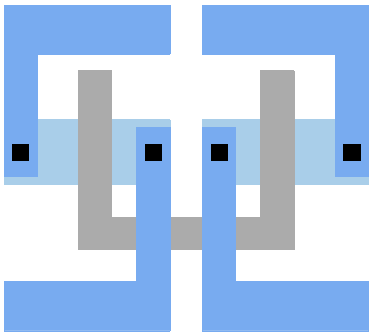
Update: DCDB Test Results



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DEPFET Detectors and Applications

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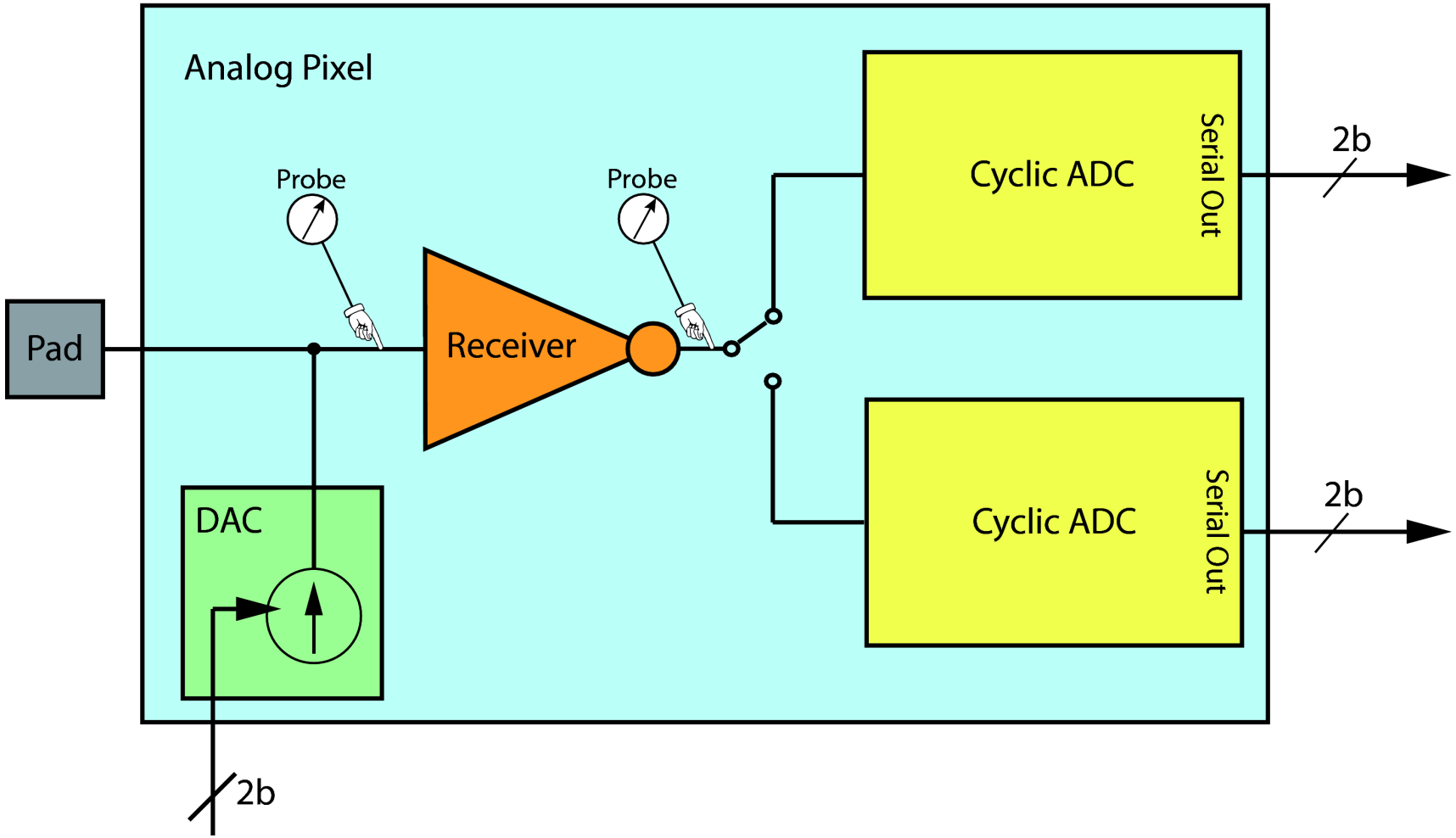
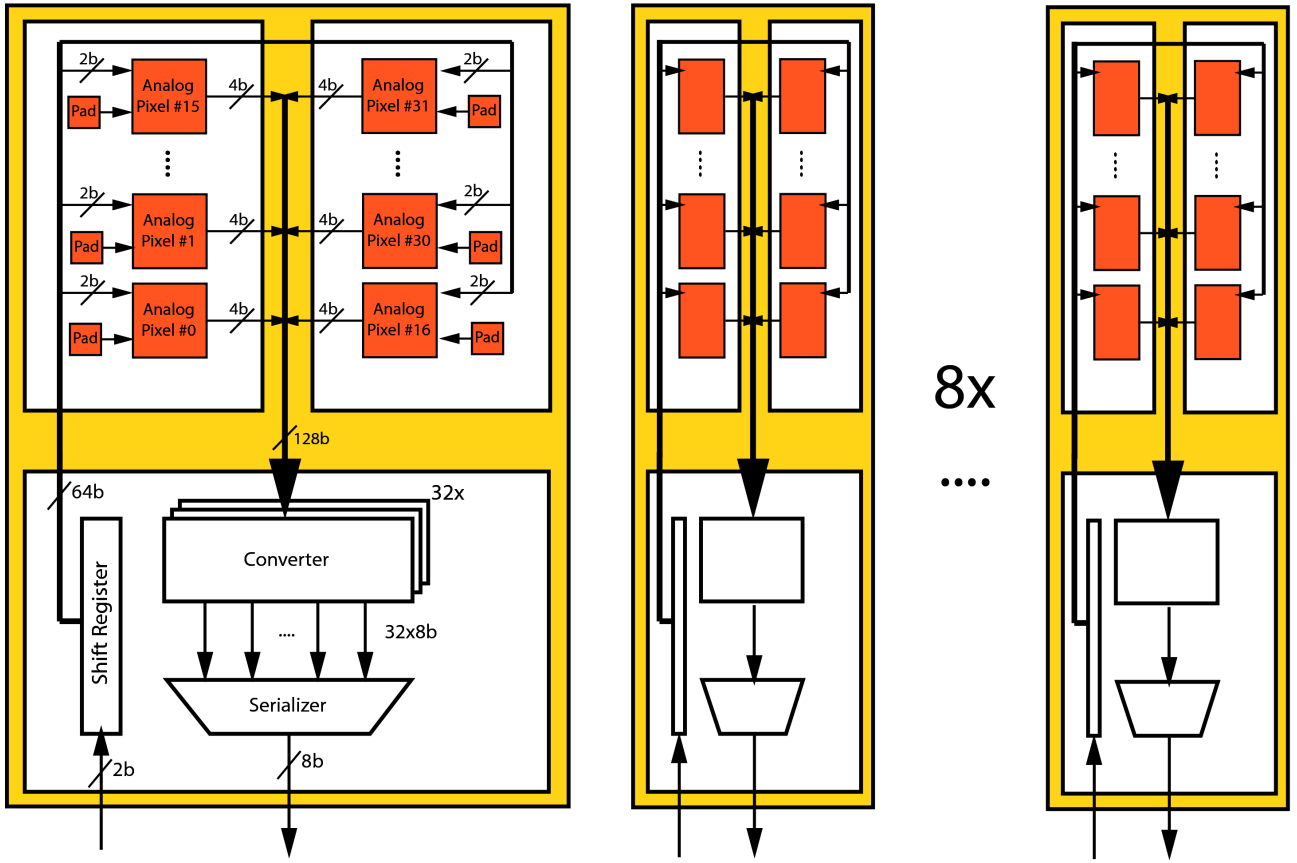
DCDB Introduction

DCDB's Analog Pixel (simplified!)



- DAC: Dynamic offset correction by adding a variable current to the input node
- Receiver: Trans-Impedance Amplifier for amplification of the input current
- Two Cyclic ADCs: Alternating conversion of analog input current to digital value
- Probes: The input and output node of every pixel's receiver is accessible via the monitor pin

DCDB Main Features



256 Channels:

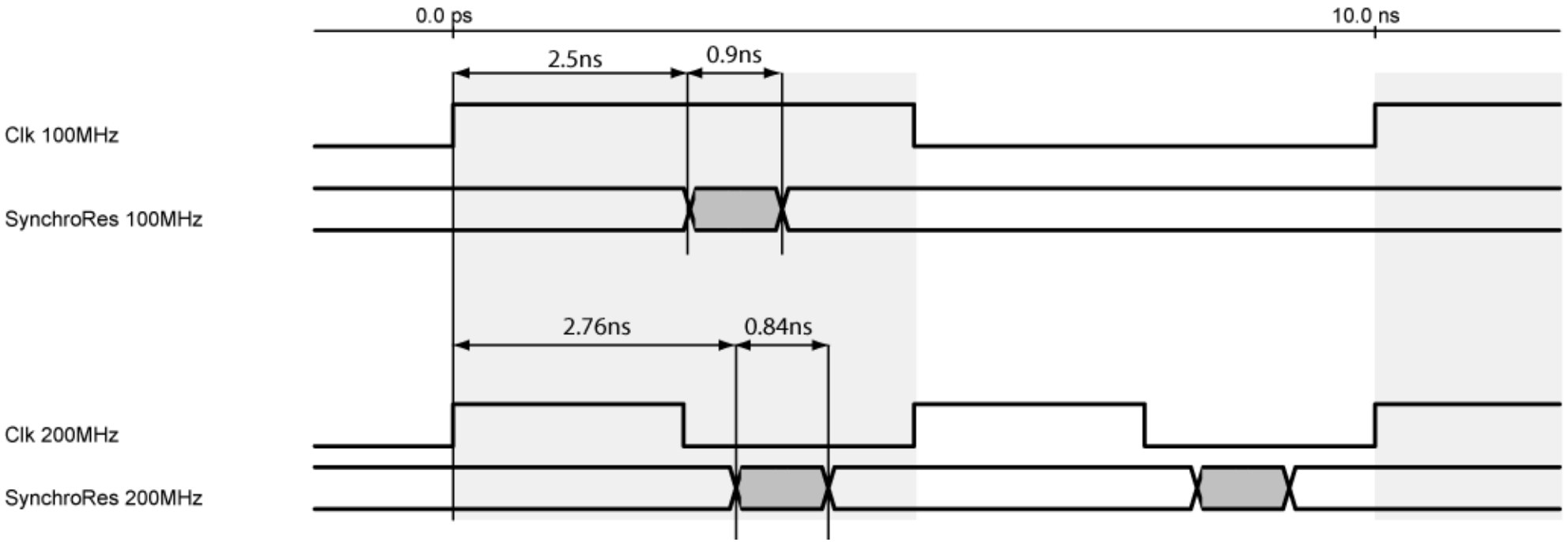
- 8 bit data output
- Dynamic offset adjustment
- 80ns target sampling period
- Power: ~4mW per channel (analog + digital)

Fully synthesized digital readout:

- 8x 8 Bit data output @ 300-400MHz
- JTAG configuration interface
- Using self-made standard cell library

Measurement Updates

Reset Timing Measurements



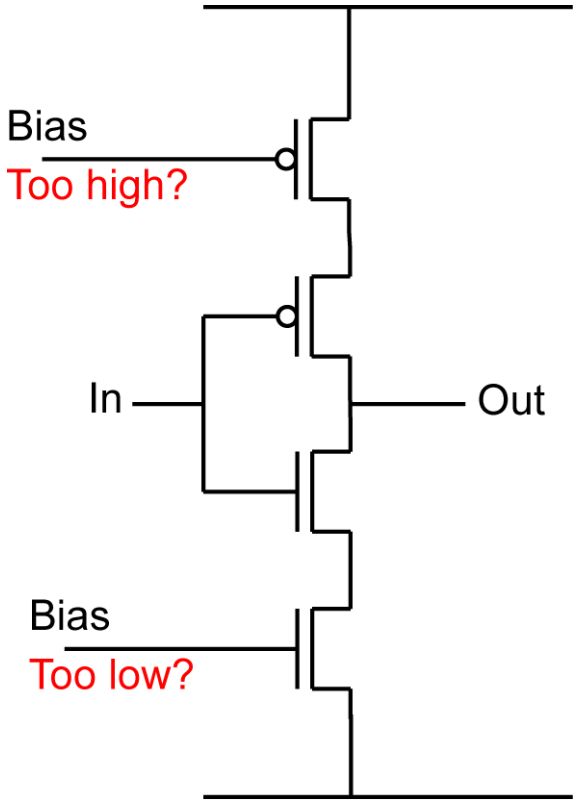
- Complicated Reset structure: Synchronous Reset needs to be synchronized to 3 clock domains → Timing potentially critical!
- Measurement: Reset timing violation window of ~1ns @ ~2.5 – 2.8ns **after** a rising clock edge

  → Usual setup time, no issue here!

DCDB Speed Tests

Measurements show:

- DCDB is operating well with 100MHz clock frequency
- 200MHz: Still working ~2-3x noise
- >250MHz: No satisfying operation

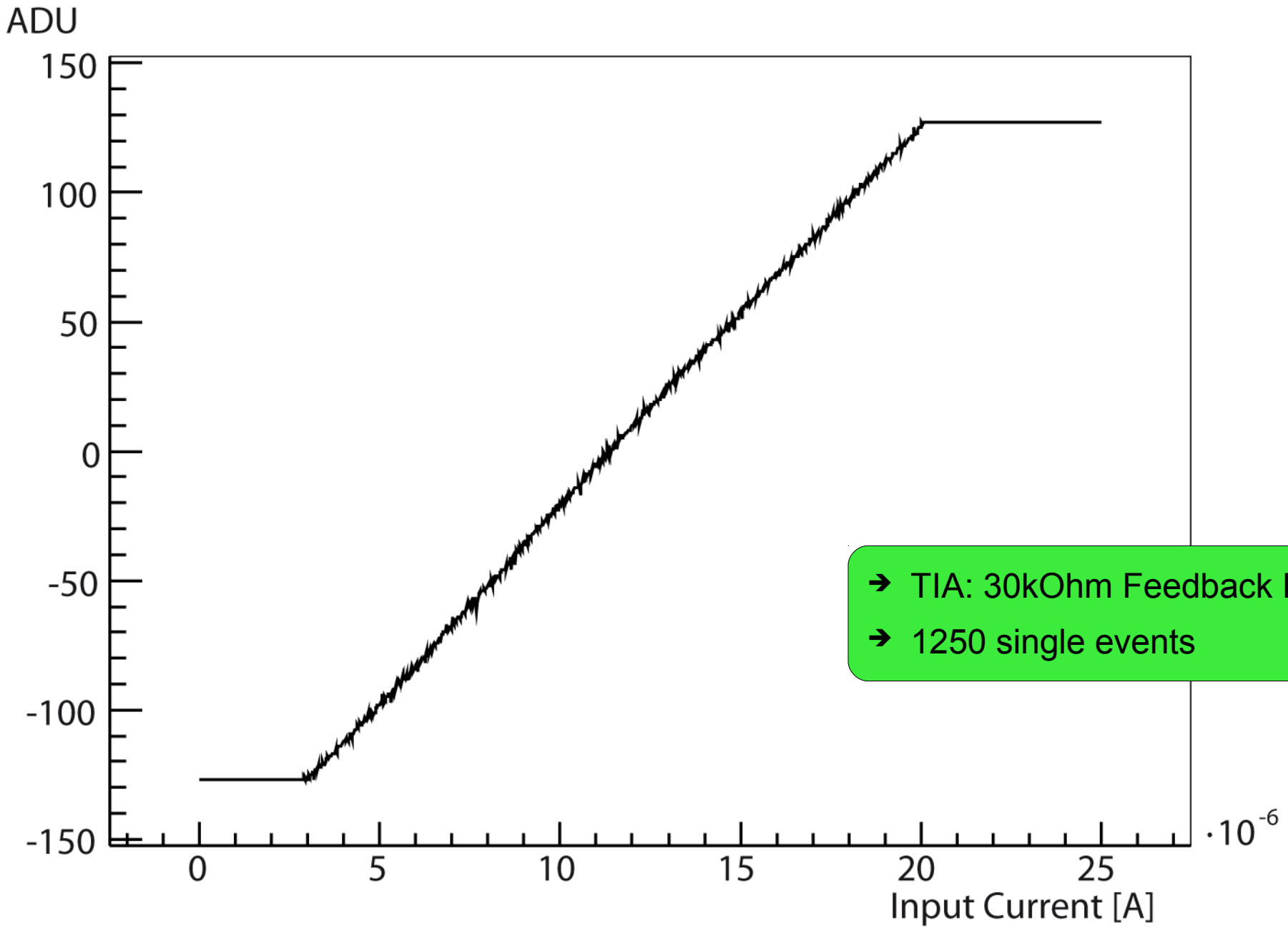


Reason:
Bug in an analog delay element for the steering signals of the current memory cells

→ Needs to be fixed in the next chip revision!

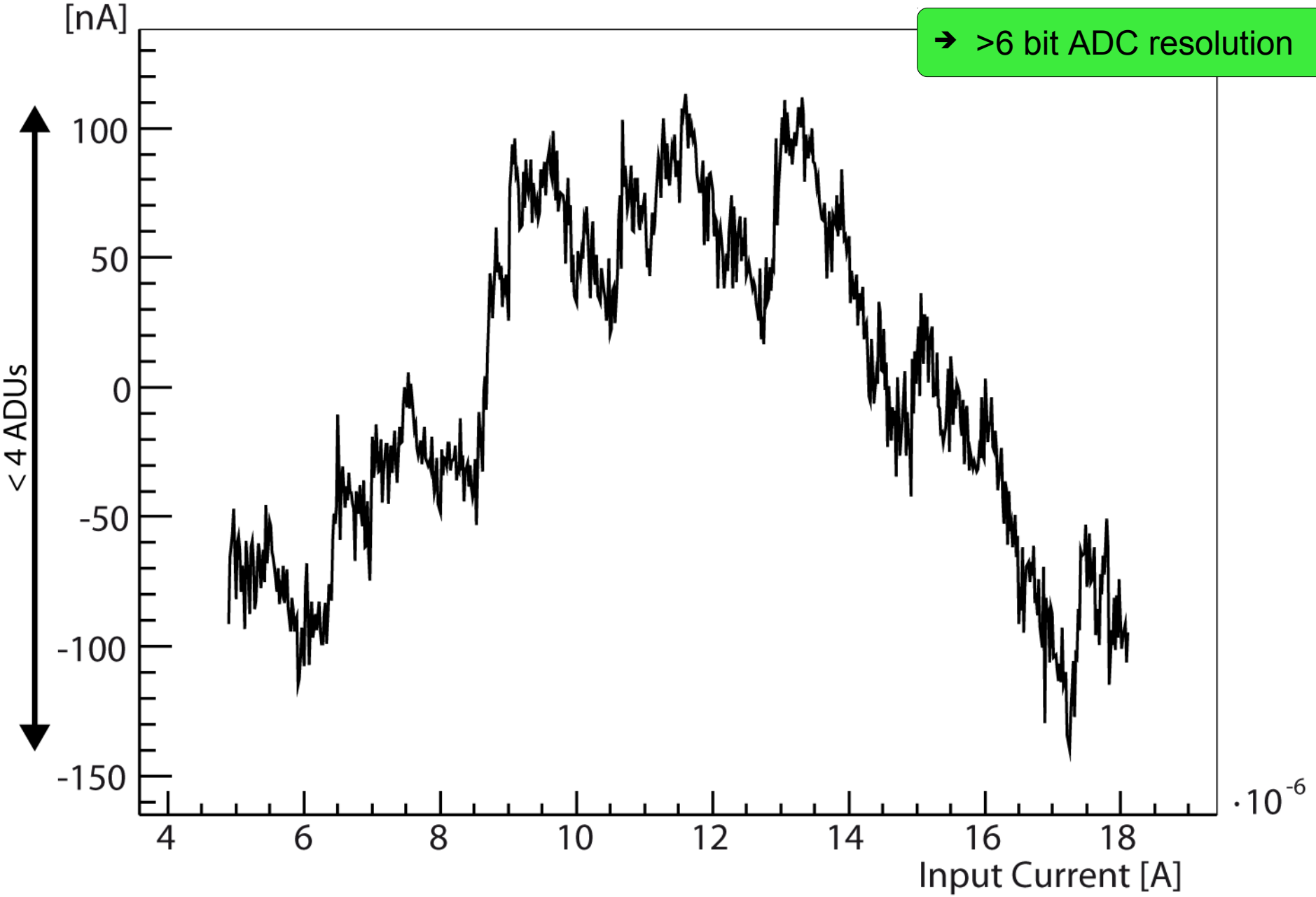
Default frequency: 100MHz → 3.125MHz ADC sample rate

ADC's Transfer Characteristic



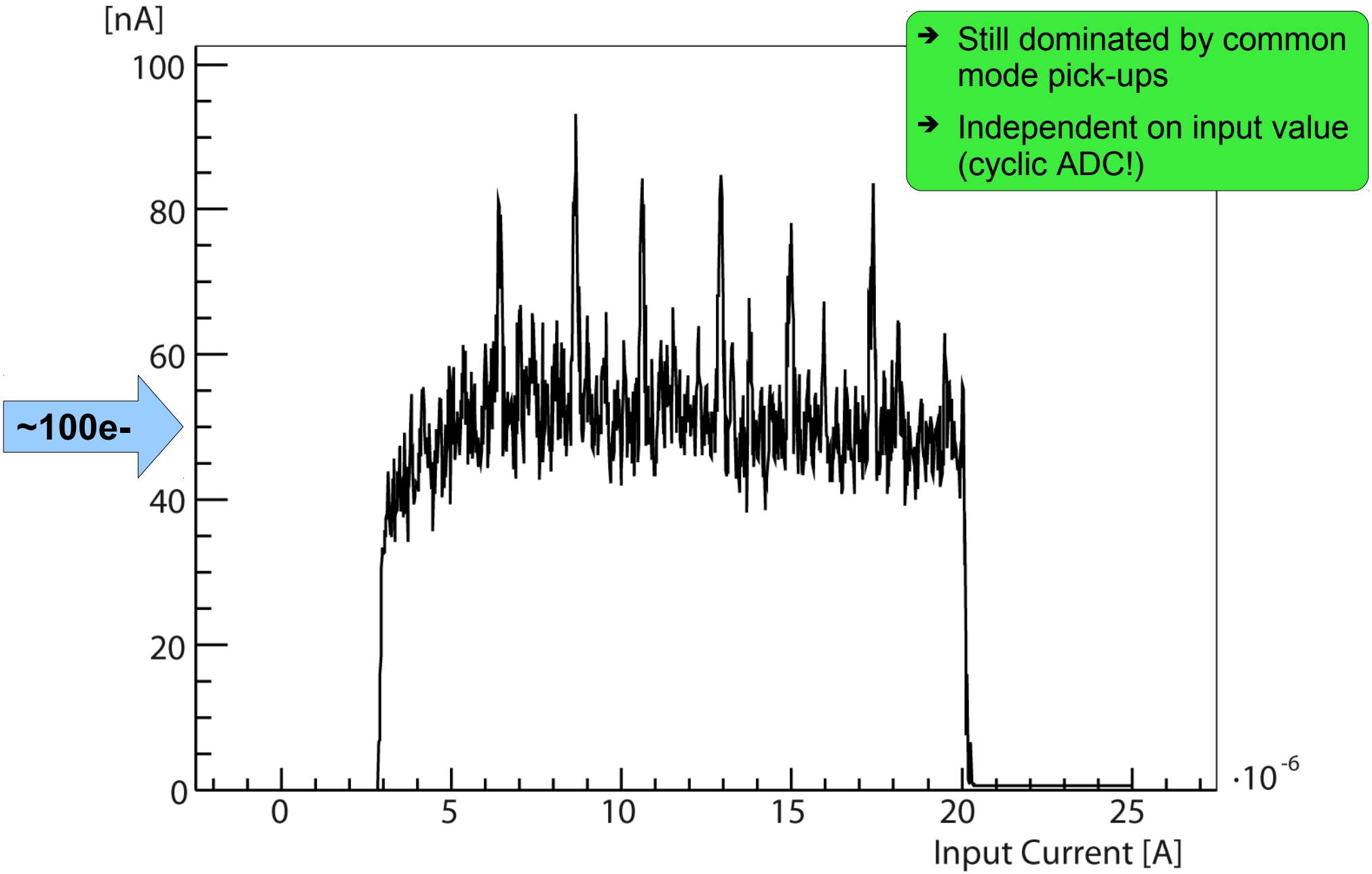
- TIA: 30kOhm Feedback Res
- 1250 single events

ADC's Integral Non-Linearity



➔ >6 bit ADC resolution

ADC's Noise (RMS)

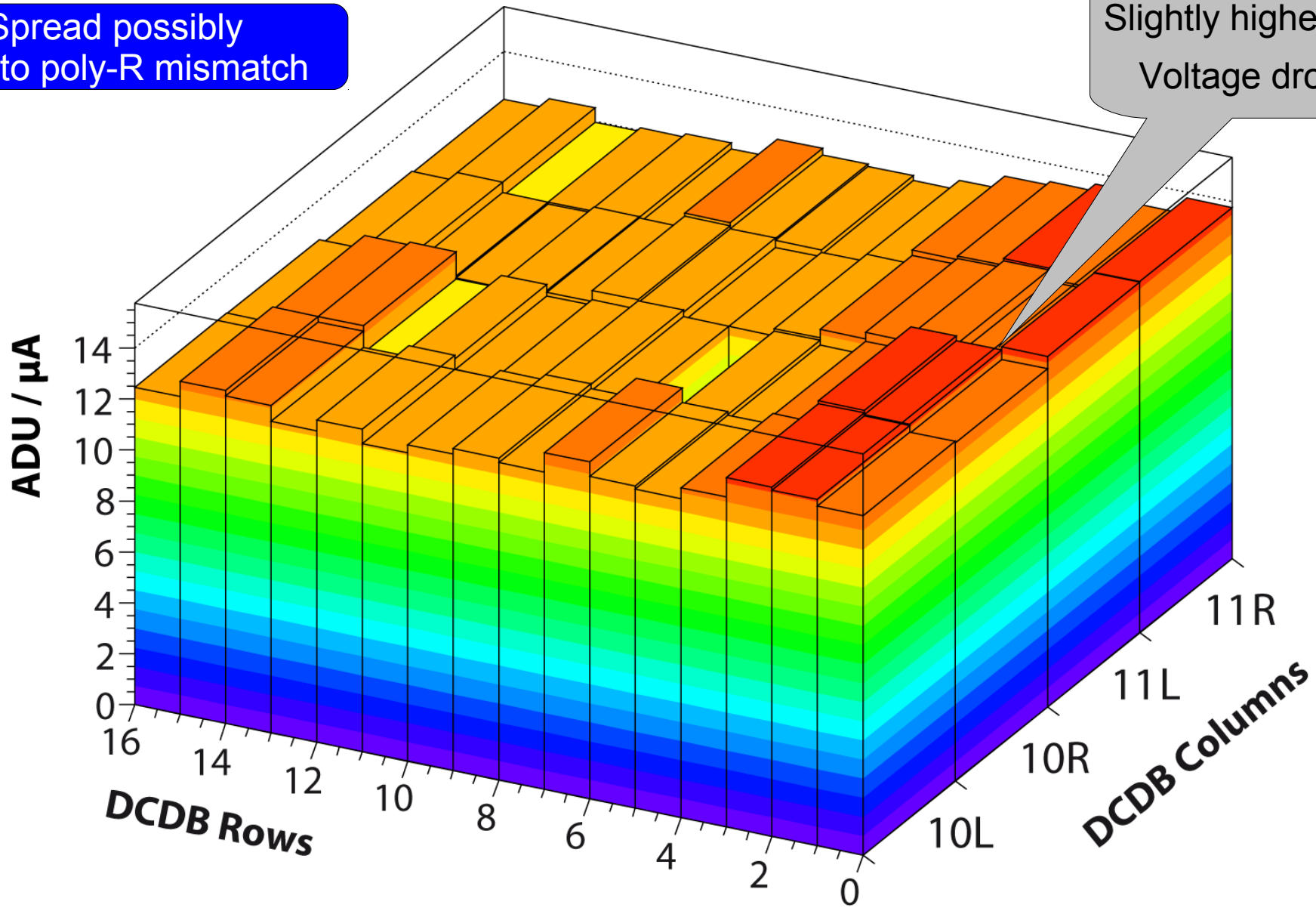


- Still dominated by common mode pick-ups
- Independent on input value (cyclic ADC!)

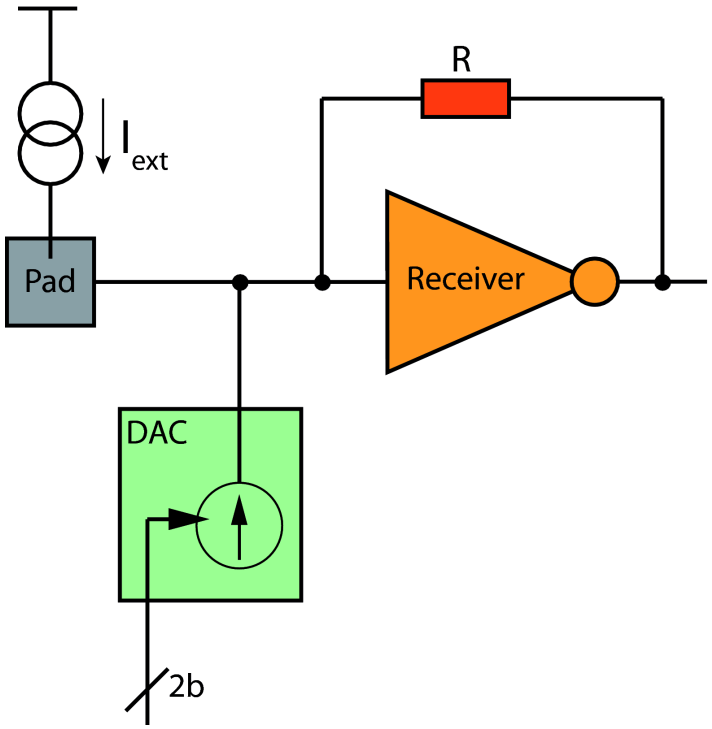
Gain Map

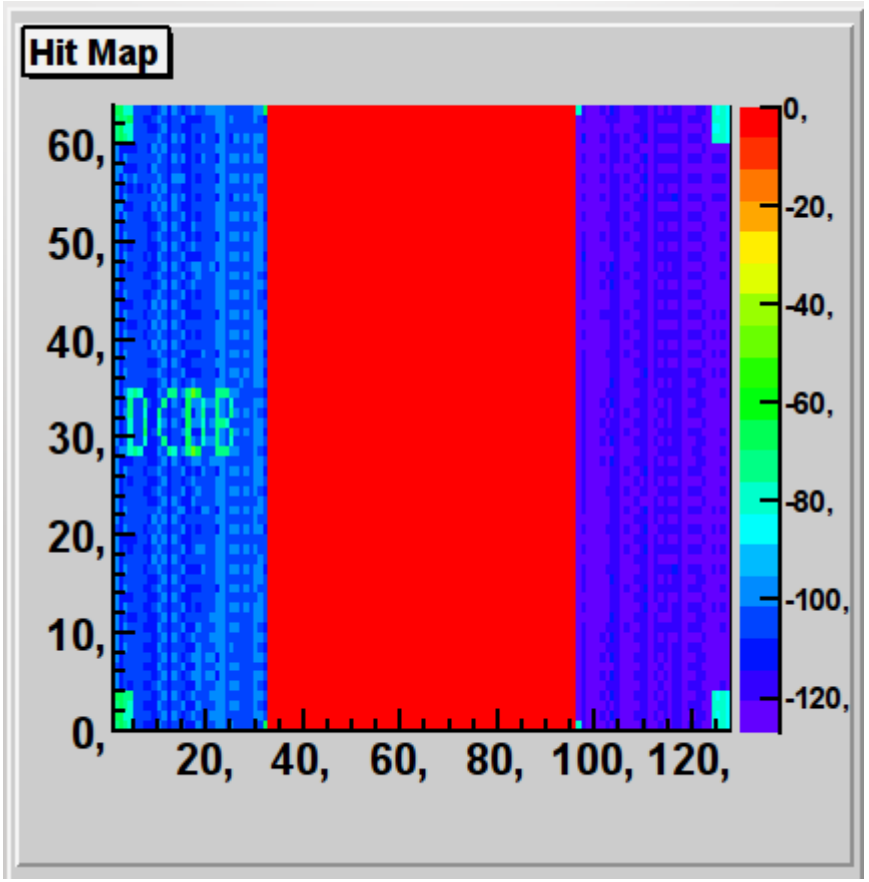
Spread possibly due to poly-R mismatch

Slightly higher gain. Voltage drop??



Dynamic Offset Correction





DCDB-Controller is operating in Frame Readout Mode:

- A frame is assembled by a number of lines
- Every line is an entire DCDB conversion cycle
- New offset values from a predefined map for each conversion cycle

DCDB Test Summary

- ✔ DCDB production is finished. The 7th metal layer / bump bond process seems to work
- ✔ Test environment is set up: DCD-RO, bumping, PCB, FPGA firmware, software
- ✔ Power consumption within the expected range
- ✔ JTAG configuration interface is operating
- ✔ JTAG Boundary Scan is operating
- ✔ Digital data conversion and serialization is working
- ✔ ADC's point of operation is found
- ✔ Reset timing issue investigated: No issue!
- ✔ Dynamic offset compensation mechanism is operating

- ✗ Double correlated sampling mode needs externally generated strobe signal
- ✗ There is a gain variation that needs to be understood
- ✗ The maximum operation frequency is limited to 100(200)MHz due to a bug in a delay element

Thank you!