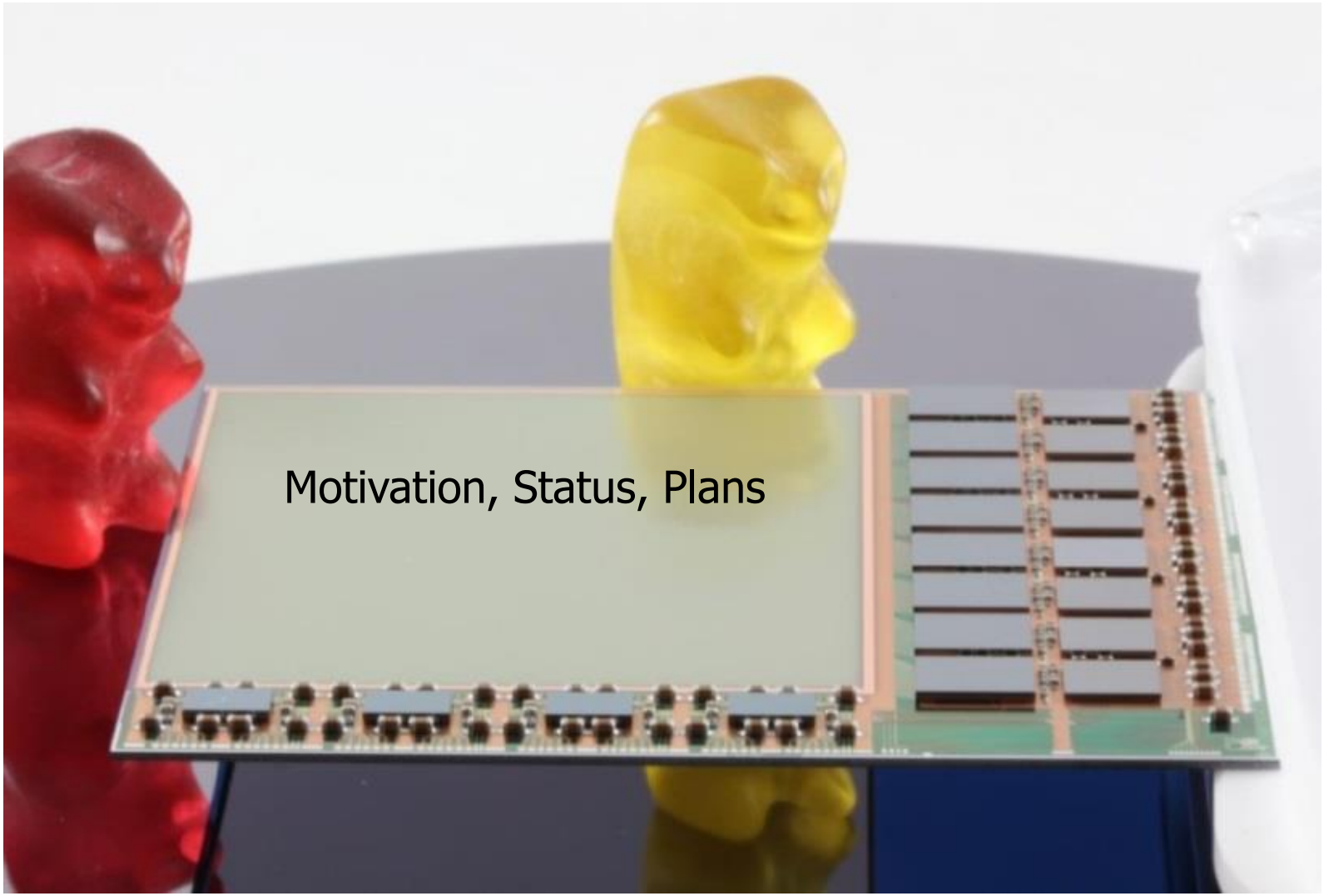
Circuit Simulation of Sensors at HLL

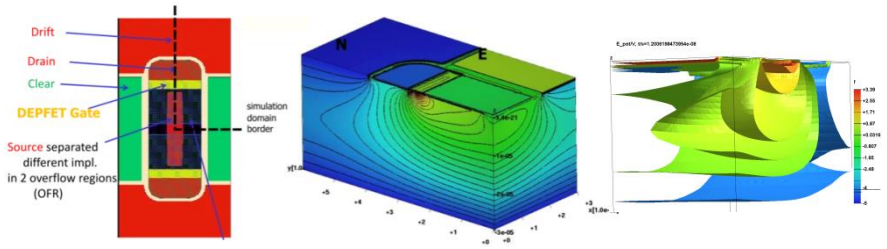


Circuit simulation

Difference to process an device simulation on single devices often called a technology simulation

To distinguish to circuit simulation

Simulation of circuits (interplay of many devices)



input signals -> output signals

Based on design data

layer layout (Cadence: Virtuoso)

design rule check (DRC) verification ? Comply with technology ?

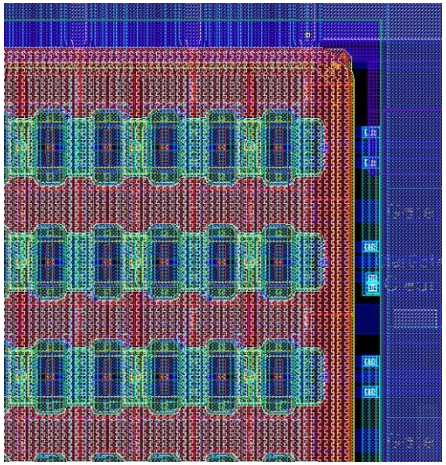
layout vs schematic (LVS) verification ? Comply with schematic ?

(2 HLL Progress Reports given recently)

schematic of circuit (Cadence)

mathematic models of all components and (single) devices

most interesting one: DEPMOS model has to be provided by us



Motivation for circuit simulation

In the past:

it was enough to invent and produce unique sensor devices
pnCDDs, drift detectors, DEPFETs (difficult enough …)

Today: competition by CMOS pixel sensors (produced in adapted technologies)
especially for DEPFETs and pnCCDs

Design and production cutting edge sensors by making use of the full potential of our sensors

What can we gain by sensor circuit simulation?

- better understanding of limitations on sensors itself
  speed, S/N - crucial parasitic components, design and/or technology adaptions ?

- optimization of interplay with control and readout electronics
  Goal: develop kind of **global models** of our most important sensors
  -> ASIC designers that they can provide tailored solutions

- easier interpretation of measurements

Goal for DEPFET Simulation

electric simulation of the entire signal path:

Switcher Read pulse -> signal propagation at gate line -> Depfet onset
-> signal propagation at drain line -> DCD amplification

What do we need and what we have ?

Simulation models for switcher driving stages and DCD input stage (Ivan Peric, KIT)

RCL- model for gate/clear lines – extraction of parasitics (-> Andreas)

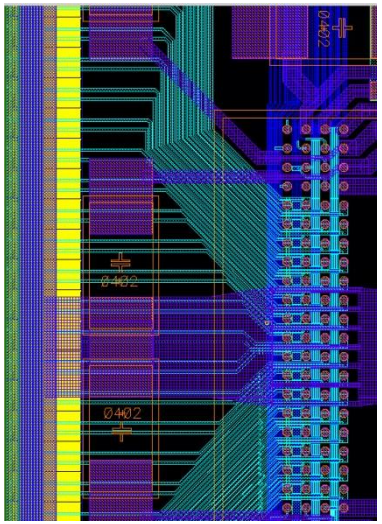
Depfet Model - Alex, Tuna, Sebastian started with a new model
we gained some experience with an old quick and dirty approach

Put all things together (mixed technology simulation)

RCL parasitic extraction (metal and poly lines)

From layout data – Cadence tool: PEX

developed for planarized topologies what we do not have ☹

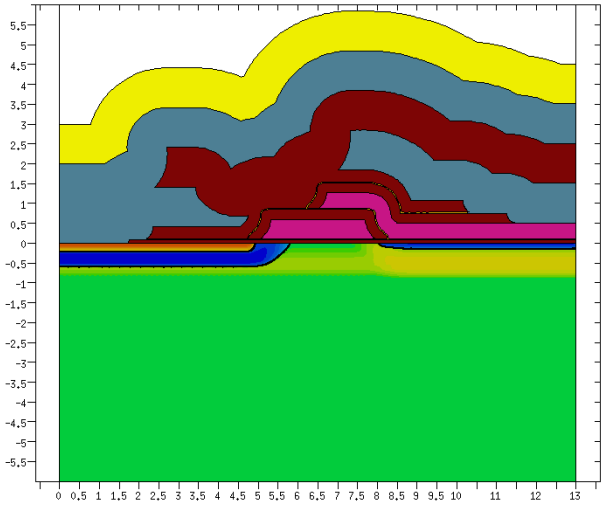


We assume that is usable for fanin/fanout connections
small errors: not many crossings, the bulk of capacitive load is the matrix

Depfet Matrix: much more topology

PEX extraction formulas will not work

different solutions



Looks more crucial
as ist is
y-scale / x-scale about 2

DEPFET Model

Components

MOS transistor model

+

internal amplification
clear process (further transistor)
line (external) capacitances + resistances
junction (internal) capacitances + resistances (contacts)

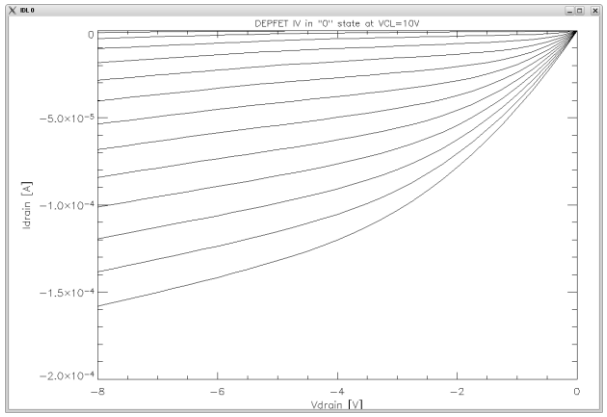
Requirements

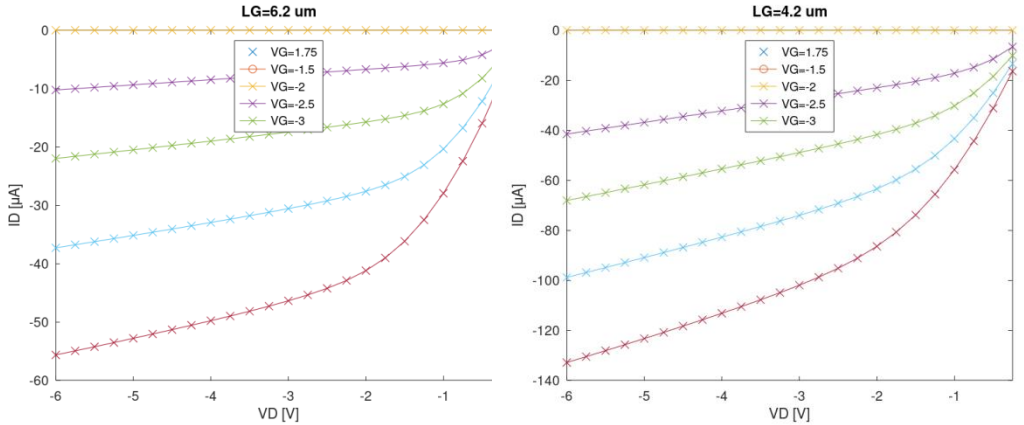
numerically fast and clean
precise (10% ?)
physically motivated equations
(predictive power over a large design and technology parameter space)

We started already and can learn from old attempts

Old Model
MOST look up table

New Model
Real MOST Parameter model

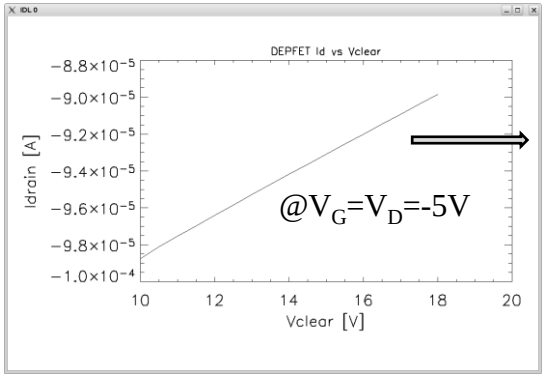




(last Progress Report by Alex)

Measured at $V_{cl\ high}$ (to keep internal Gate empty during static measurements)

For read mode $V_{cl\ low}$: correction of currents for Clear voltage needed



New lookup table for V_{cl}^{lo} :

$g_m^{Cl} = 1.1\ \mu S$

$$I_{"0"}^{CLLo} = I_{"0"}^{CLHi} + \sqrt{\frac{I_{"0"}^{CLHi}}{I_{"0"\,Ref}^{CLHi}}}\, g_m^{CL} \left(10\,V - V^{CLLo}\right)$$

$$I_{"0"\,Ref}^{CLHi} = I_{"0"}^{CLHi} \quad @\ V_G = V_D = -5\,V$$

Taking into account the amount of signal electrons N_{SIG}

Old model:

‘Filling‘ the Internal Gate

$$I_{"1"}^{CLLo} = I_{"0"}^{CLLo} - \sqrt{\frac{I_{"0"}^{CLHi}}{I_{"0"\,Ref}^{CLHi}}}\, g_q \; N_{SIG}$$

g_q = 400pA/electron - internal amplification @V_G=V_D=-5V

New model: $g_q = f(w,L,tox,Id)$

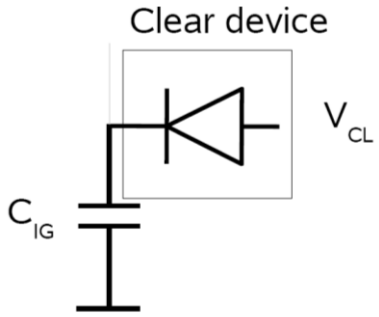
Old Clear Modul

Ebers-Moll like diode eq.

$$\frac{\Delta Q}{\Delta t} = I_{C0}\left(e^{y} - 1\right)$$

$$y = k\left(V_{CL} - V_{ON} - V_{IG}\right)/V_T * \frac{V_{IG}^{"0"} - V_{IG}}{V_{IG}^{"0"}}$$

stops clear current when the Internal Gate is empty



$V_{IG} = \frac{Q + \Delta Q}{C_{IG}}$ Internal Gate Potential

$V_{IG}^{"0"}$ empty Internal Gate Potential

I_{C0} saturation current

k constant

V_{ON} onset voltage for the clear process (potential barrier)

V_T temperature voltage

Circuit simulator provides a time step Δt
The model has to calculate the corresponding ΔQ at the applied V_{CL}
The new signal charge change I_d which is returned to the simulator.

$$\frac{\Delta Q}{\Delta t} = I_{C0}\left(e^{y} - 1\right)$$

$$f = I_{C0}\left(e^{y} - 1\right) - \frac{\Delta Q}{\Delta t}$$

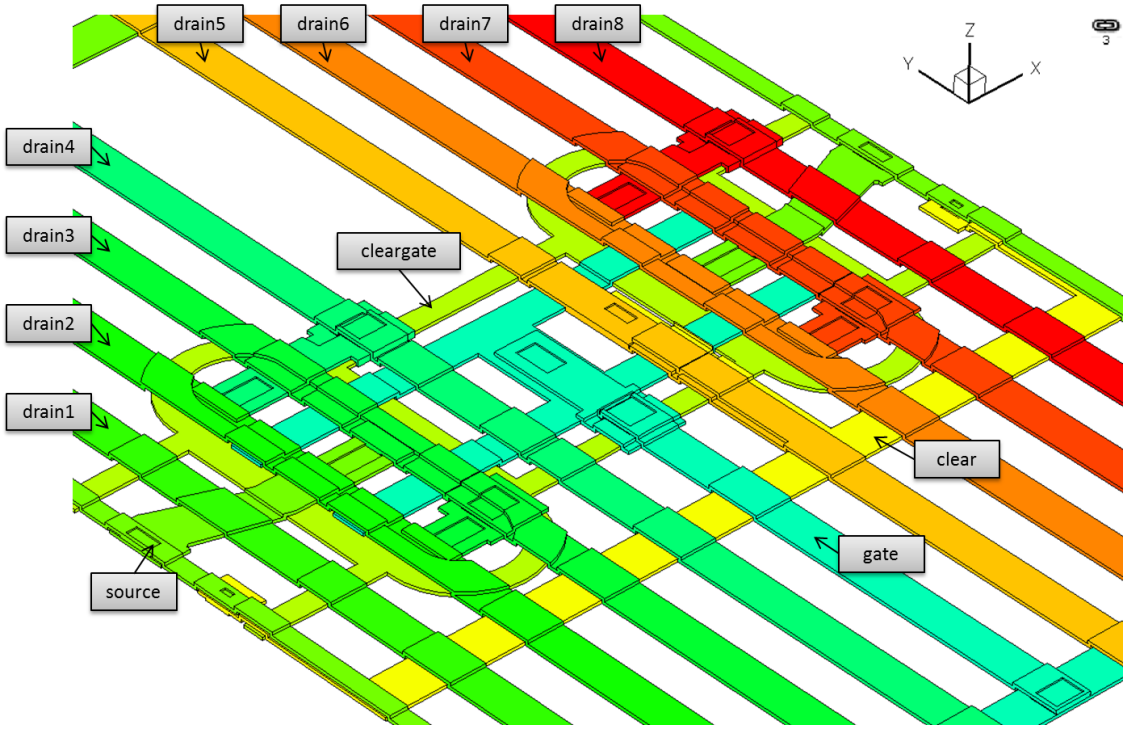
Search for the root (null) gives ΔQ

Really quick and dirty - works but physical meaning ??

Needs revision:

Better subthreshold modell for n channel trans. (source follower mode)

Belle line capacitances – 3d



Belle Layout gds data imported to Sentaurus Structure editor

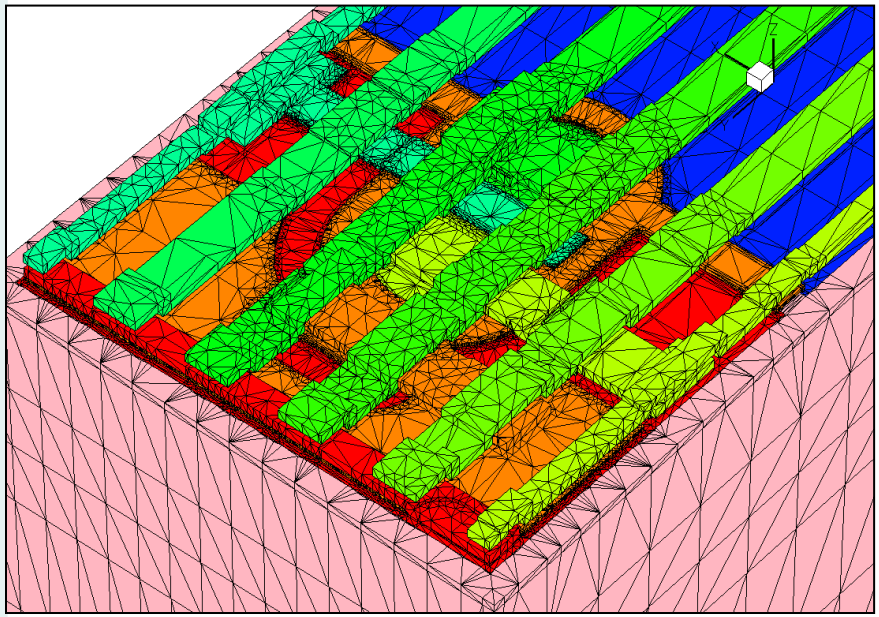
3d simulation with Raphael field server

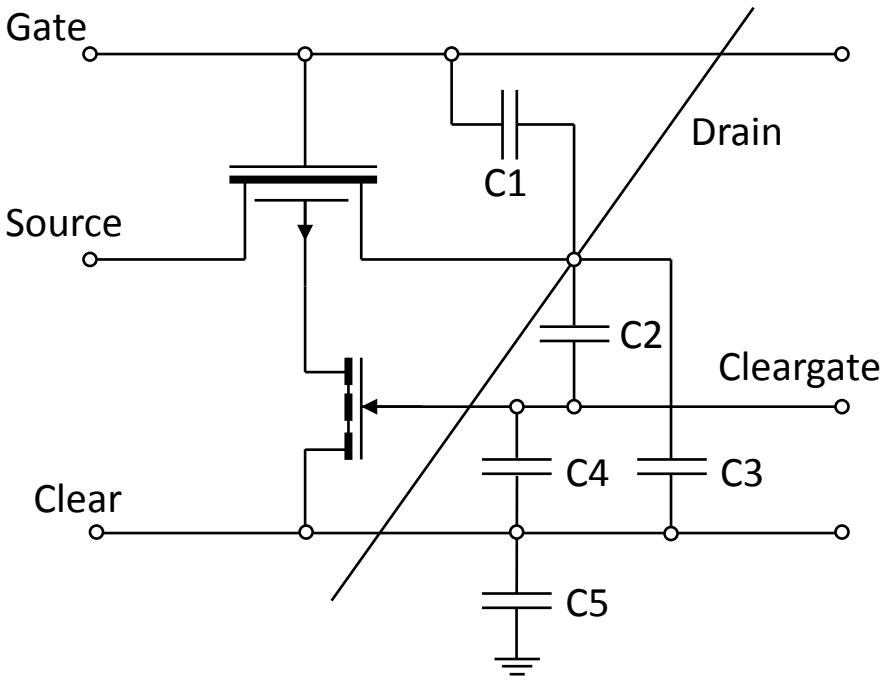
-> capacitance matrix

(Christian K.)

Expected efford for a new design: ca. 0.5 days

Results for a Capacitive Coupled Clear Gate Pixel





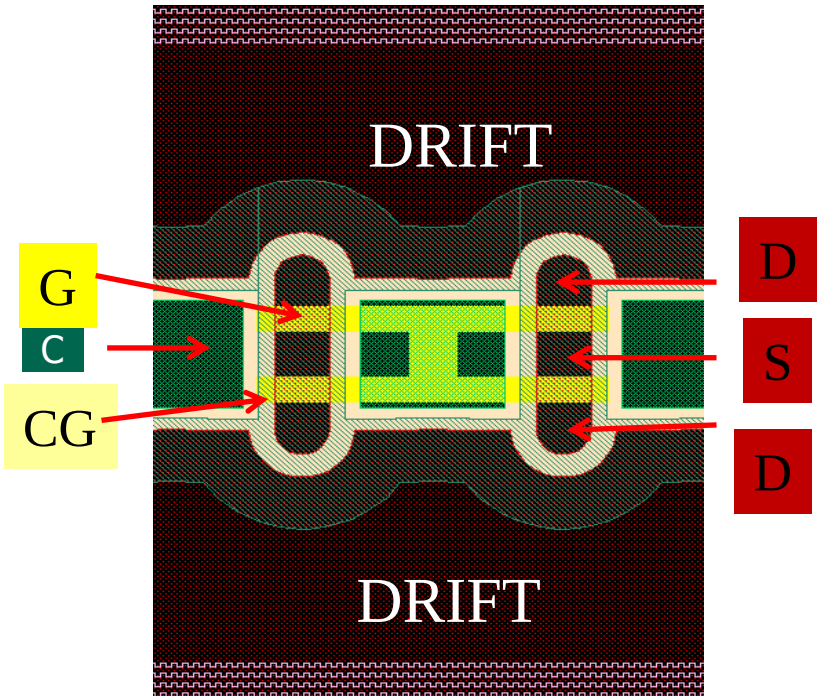
cap label	net1	net2	cap [fF]
C1	Gate	Drain	8.7
C2	Cleargate	Drain	17
C3	Clear	Drain	4.5
C4	Clear	Cleargate	167
C5	Clear	All except cleargate	56

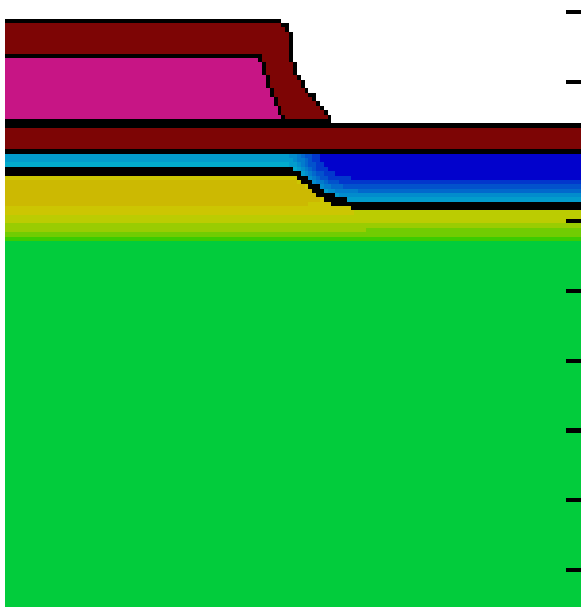
For a pixel array 768x160:

Cclear_line = 100 * 223fF = 22pF

Number of layout cells per row.

How to deal with junction caps (in silicon)





Old method: extraction by 3d device simulation

very cumbersome and time consuming ☹

Better methods? extraction like line caps. with a simple field server (only Laplace equ.)
works for all reversed biassed junction

If MOS current is flowing … standard situation look at Spice models

Simulation - Single Sampling

Simulation of I_{DS} DCD input current

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Summary

We want make circuit simulation running for HLL sensors

improve detector performance and better understanding of limiting mechanisms

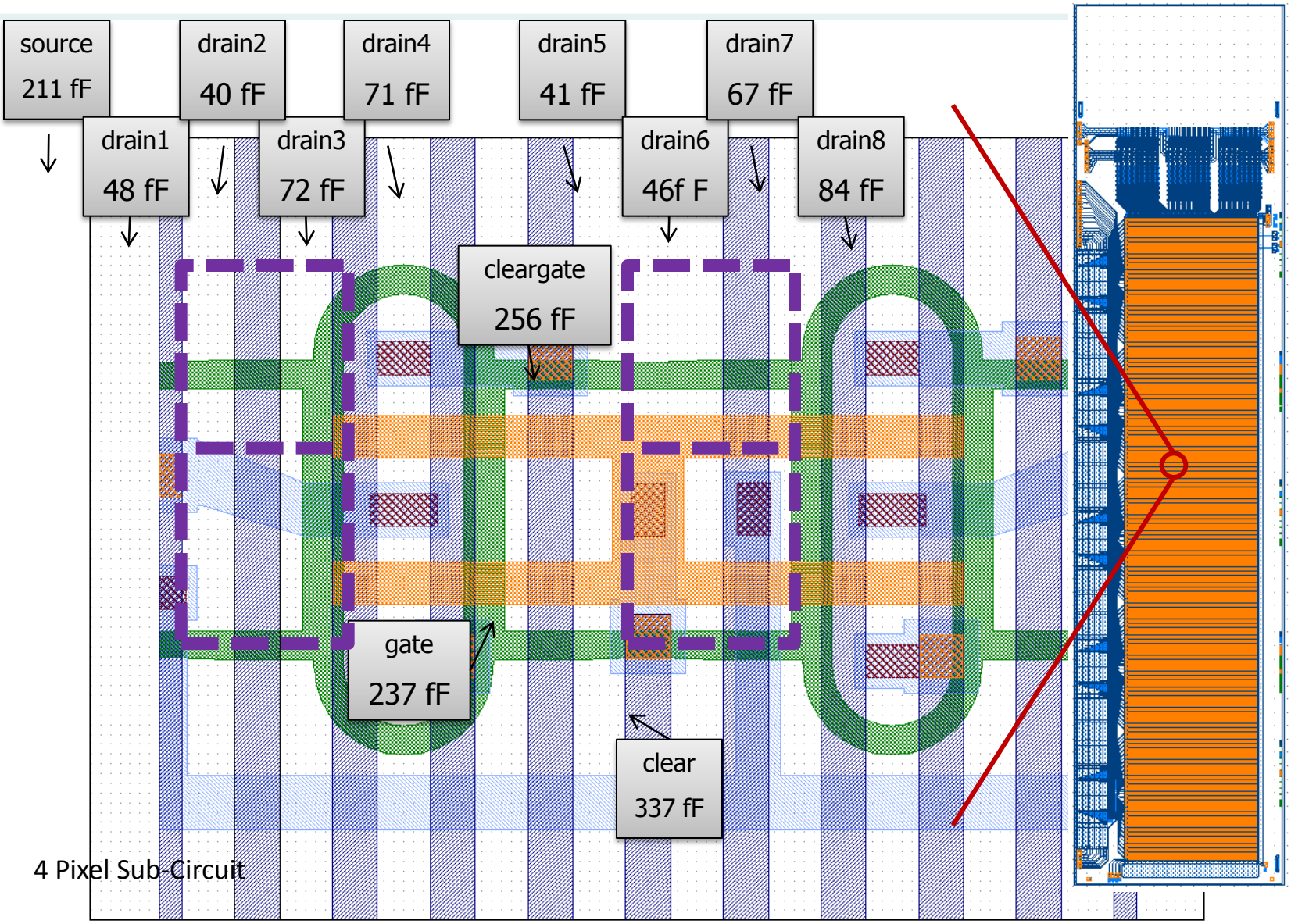
Most challenging: DEPFET modelling and capacitance extraction

work in progress

ambitious and interesting task

Backup slides

Capacitance of a DEPFET



4 Pixel Sub-Circuit