MAX PLANCK
HALBLEITERLABOR

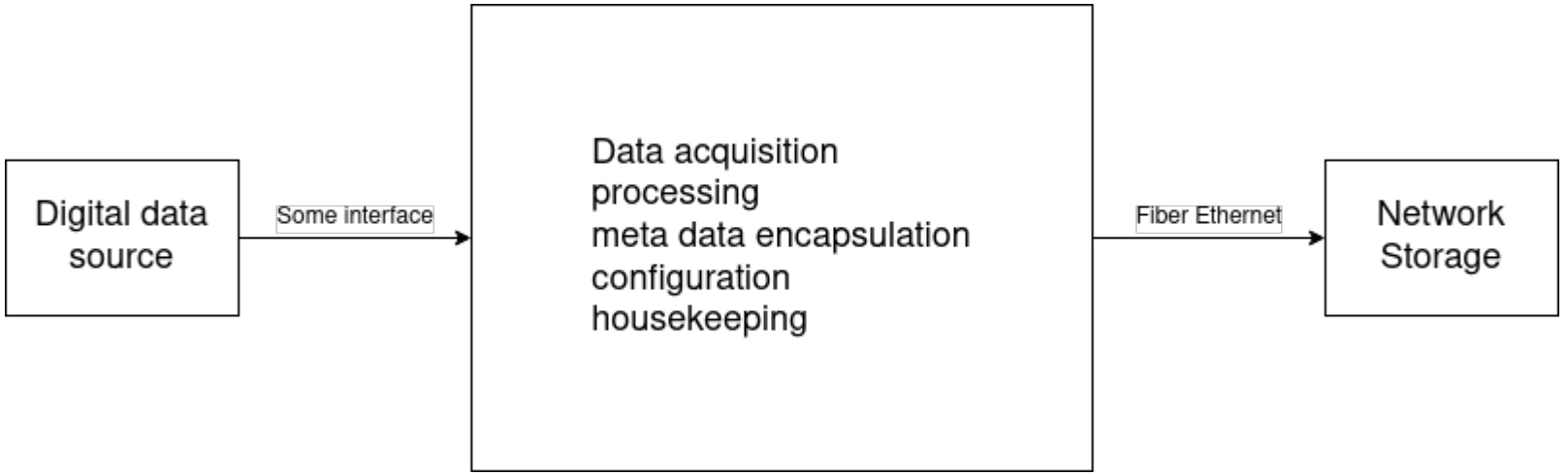
FPGA FIRMWARE DEVELOPMENT OVERVIEW

SYNERGIES BETWEEN PROJECTS

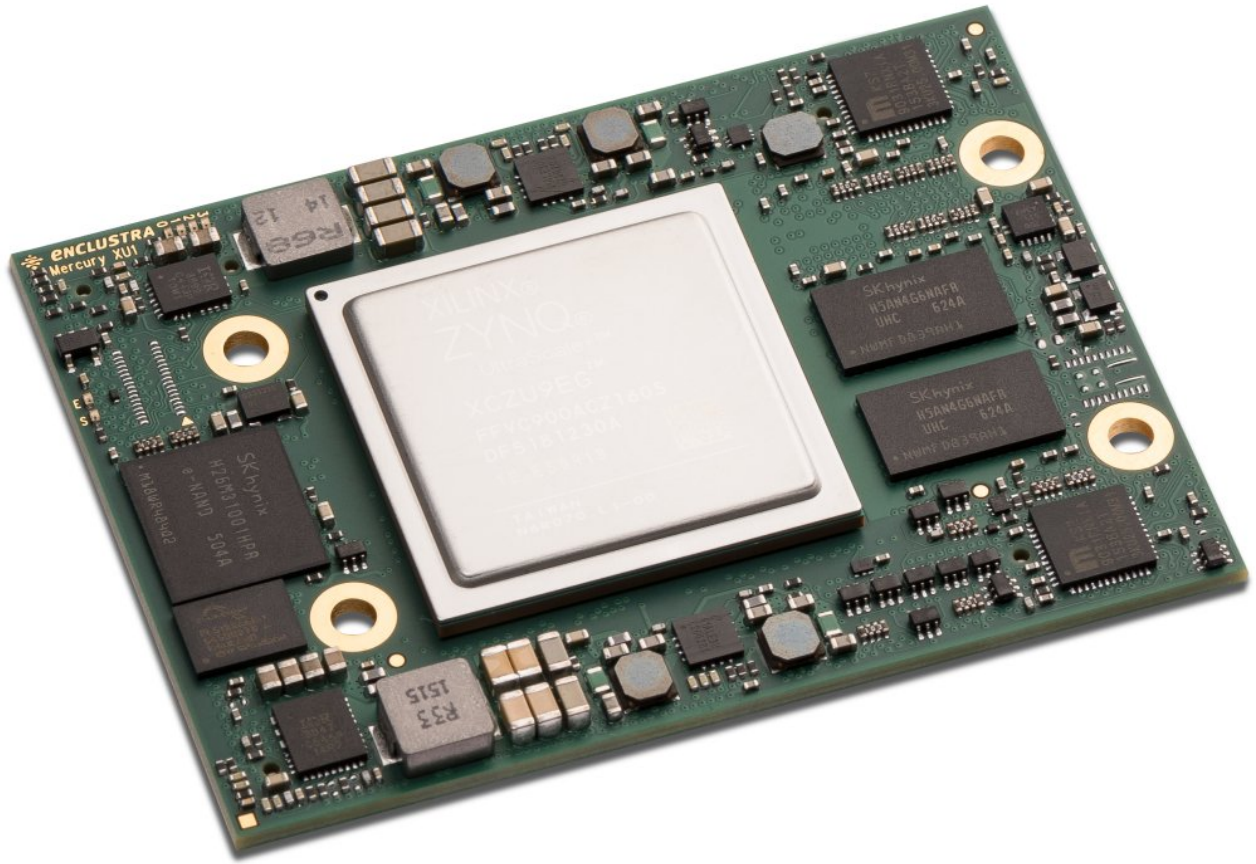
VISION OF THE FUTURE

Ringberg, December 2022

GENERALIZATION OF TASKS (DAQ SYSTEM)



HARDWARE CANDIDATE



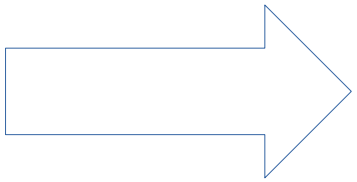
Highlights

- Built around Xilinx's Zynq Ultrascale+™ MPSoC
- DDR4 SDRAM with Error Correction Code (ECC)
- 19.2 GByte/sec memory bandwidth
- Offers PCIe® Gen2 x4, 2x USB 3.0 and 2x Gigabit Ethernet interfaces
- Available in industrial temperature range
- Three 168-pin Hirose FX10 connectors with 294 user I/Os
- Linux BSP and tool chain available
- Powerful and compact FPGA board

FPGA: TOOL CHAIN & WORKFLOW

PL requirements

- Reproducibility
- Fast simulation
- VCS



Chosen set

- SystemVerilog
- Vivado HLS
- Cadence Xcelium
- Vivado NPM (tcl flow)
- Git

IP CORES

Interconnect

- AXI(S,L) switch
- AXI-SRAM interface converters
- SRAM-register array (Xilinx primitive ports and PL settings)
- SRAM-DRP(Xilinx primitives DRP)
- PL to PS' DDR

High speed links

- Aurora
- UDP/IP XG Ethernet
- JESD204B (upto 12.5Gbps)

Peripherals

- SPI
- GPIO
- Version footprint
- S7 sequencer
- DHPT/DMC TRG sequencer

Data processing

- Dark/Offset correction
- Common mode correction
- CTI correction
- Linearity correction
- Stacking of up to N frames
- Data reduction for spectroscopic application

Data handling

- CDC
- AXIS data remap
- Slicing
- Meta data encapsulation
- Header handling

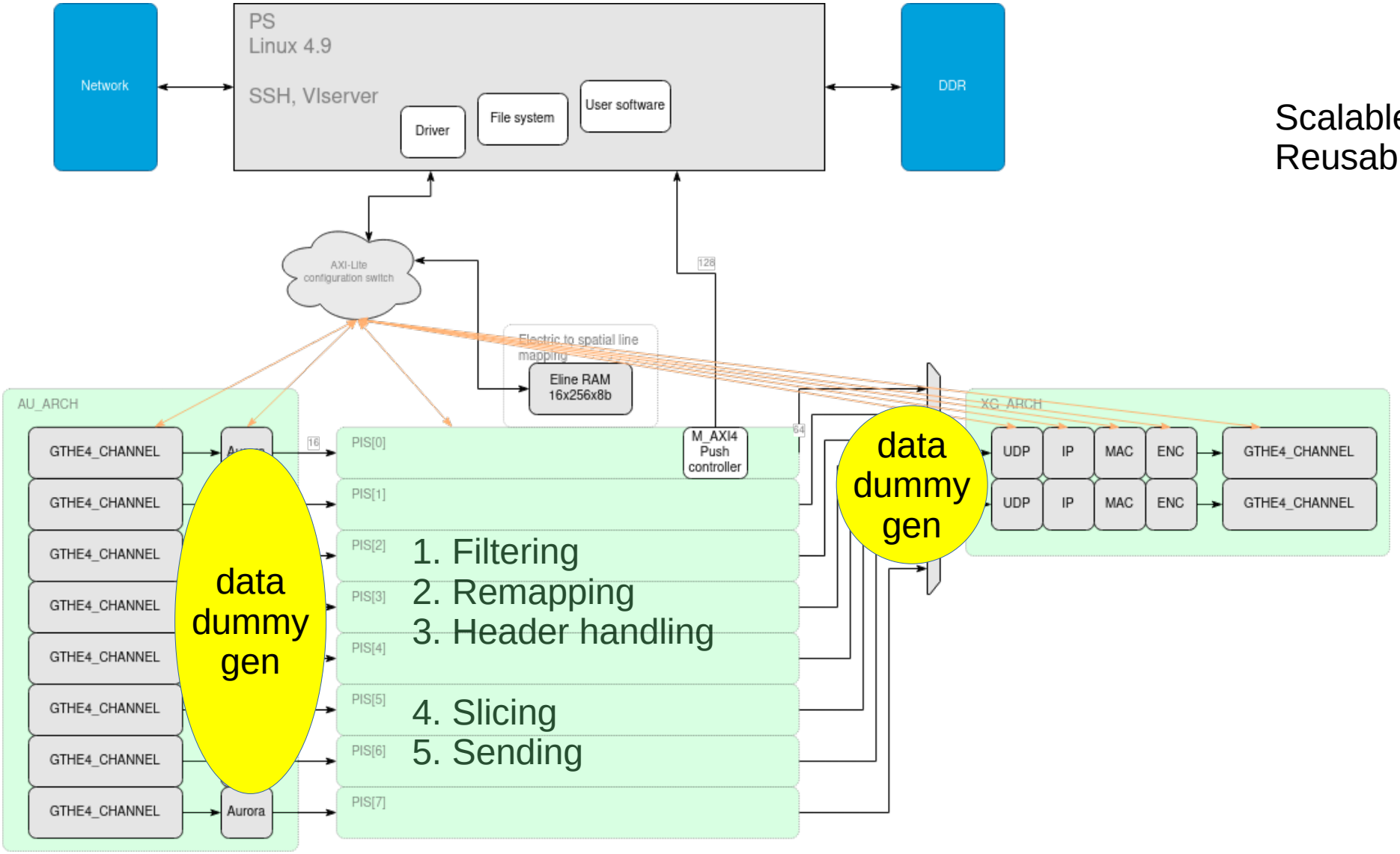
Debug

- JTAG over TCP/PS
- Registers and DP memory

*No proprietary solution used, no license fee paid

EDET80K FIRMWARE BRIEF

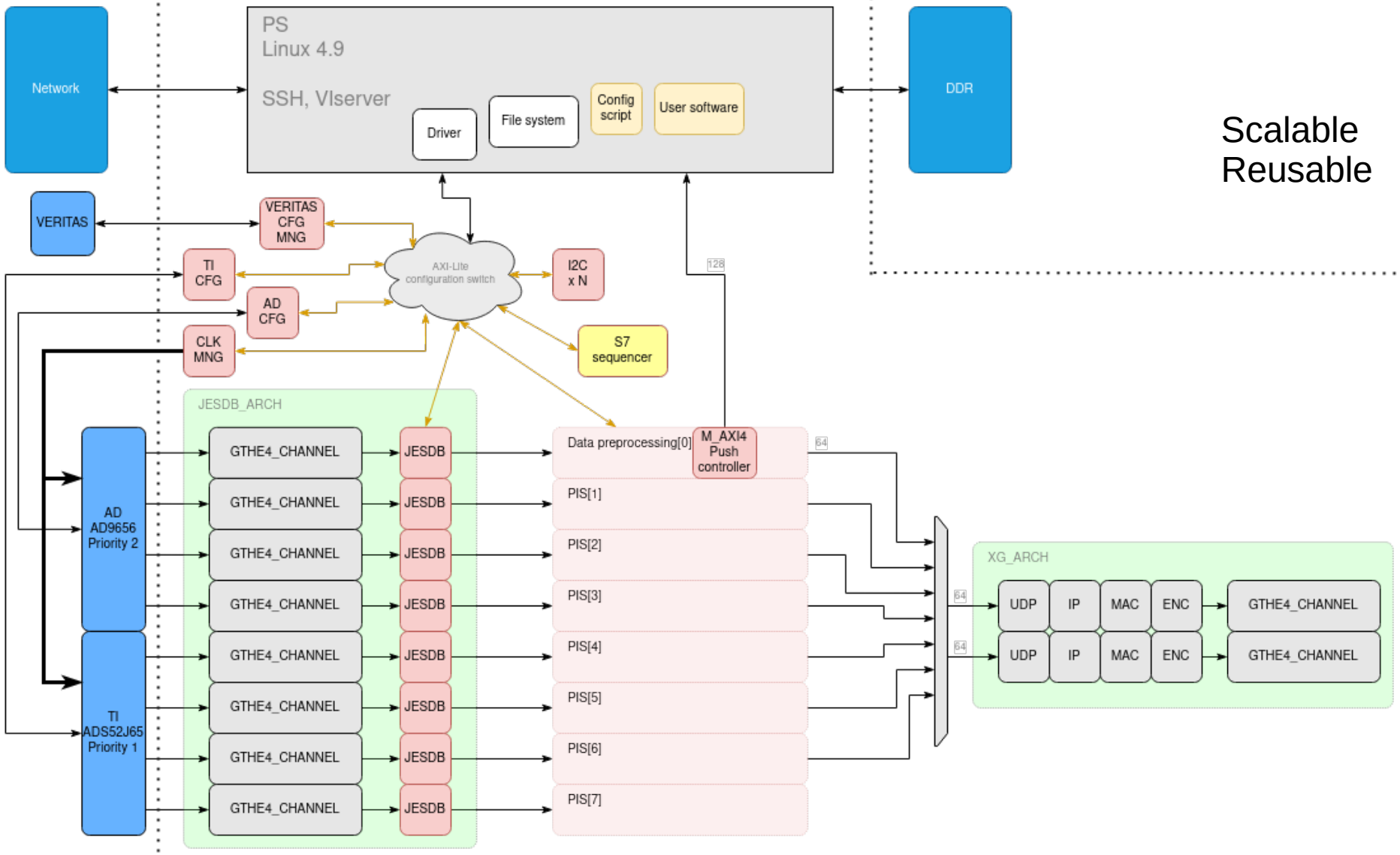
Data path



Scalable
Reusable

FSP+TNG FIRMWARE BRIEF

Data path

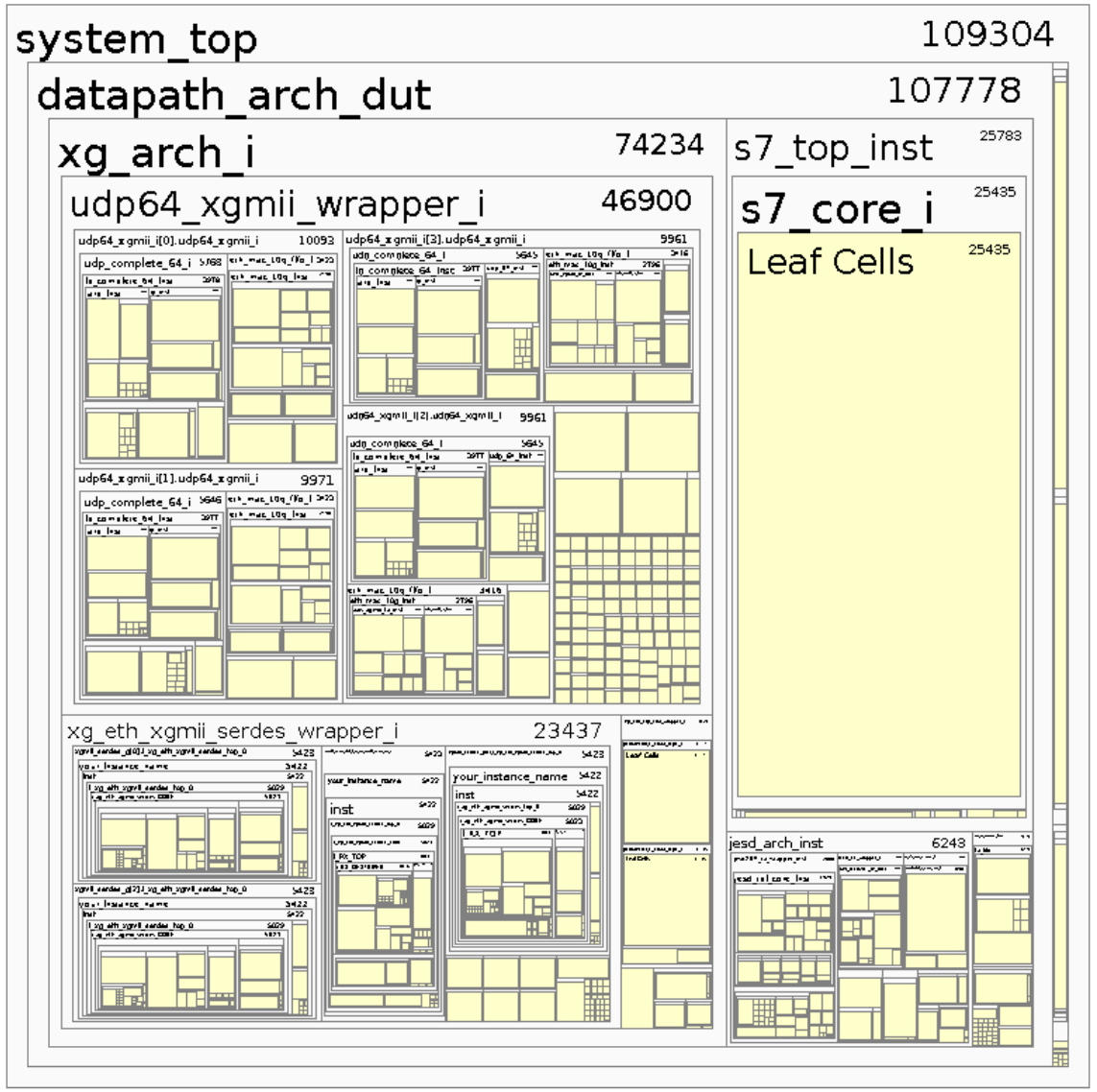


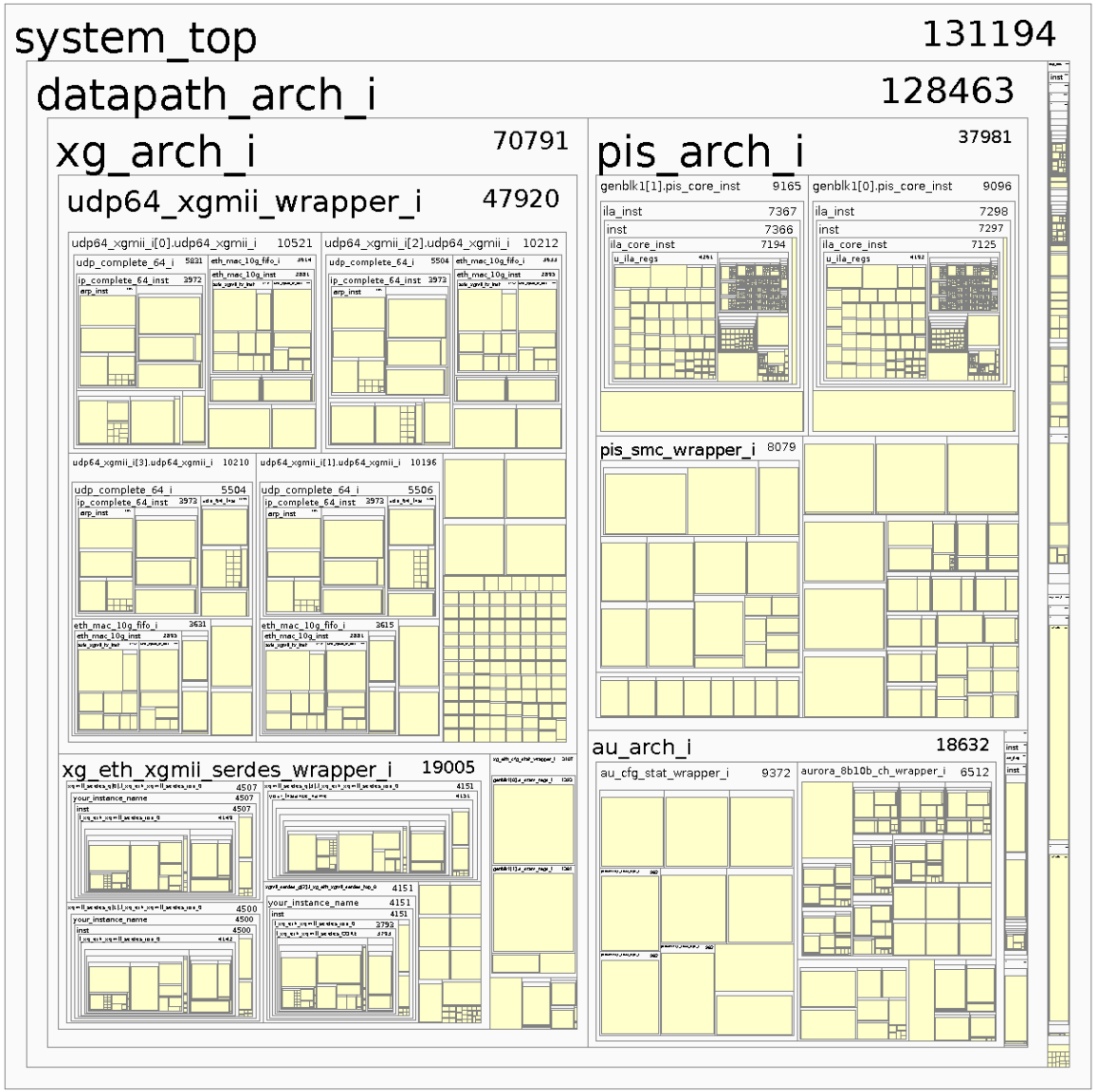
Scalable
Reusable

EDET AND FSP+TNG IP CORES UTILIZATION

EDET only	Common	FSP+TNG only
Peripherals: DHPT/TRG sequencer	Interconnect	Peripherals:SPI
HSL: Aurora	Peripherals	Peripherals:S7 sequencer
	HSL: UDP/IP XG Ethernet	Data processing
	Debug	HSL: JESD204B
	Data handling	

PROJECT HIERARCHY: FSP & EDET





PROCESSING SYSTEM

- Unified for projects
- Centralized network boot
- SDRAM based filesystem
- Rich package set

FUTURE STEPS

Workflow related:

- Update Vivado tool version (used 19.2, latest 22.2)
- Increase verification coverage
- Automate verification/build process
  (day: HDL, night: verification and build if success)

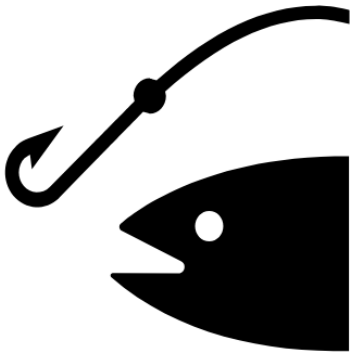
Project oriented:

- EDET:
  - Improve TRG sequencer to meet DMC capabilities
  - Enable second 10G link
- FSP+TNG
  - Improve JESD204B to rev. C
  - Implement data processing block (HLS)
- Common
  - Update Linux filesystem (add requested packages)
  - Switch to a newer kernel(?)

PS PL FIRMWARE

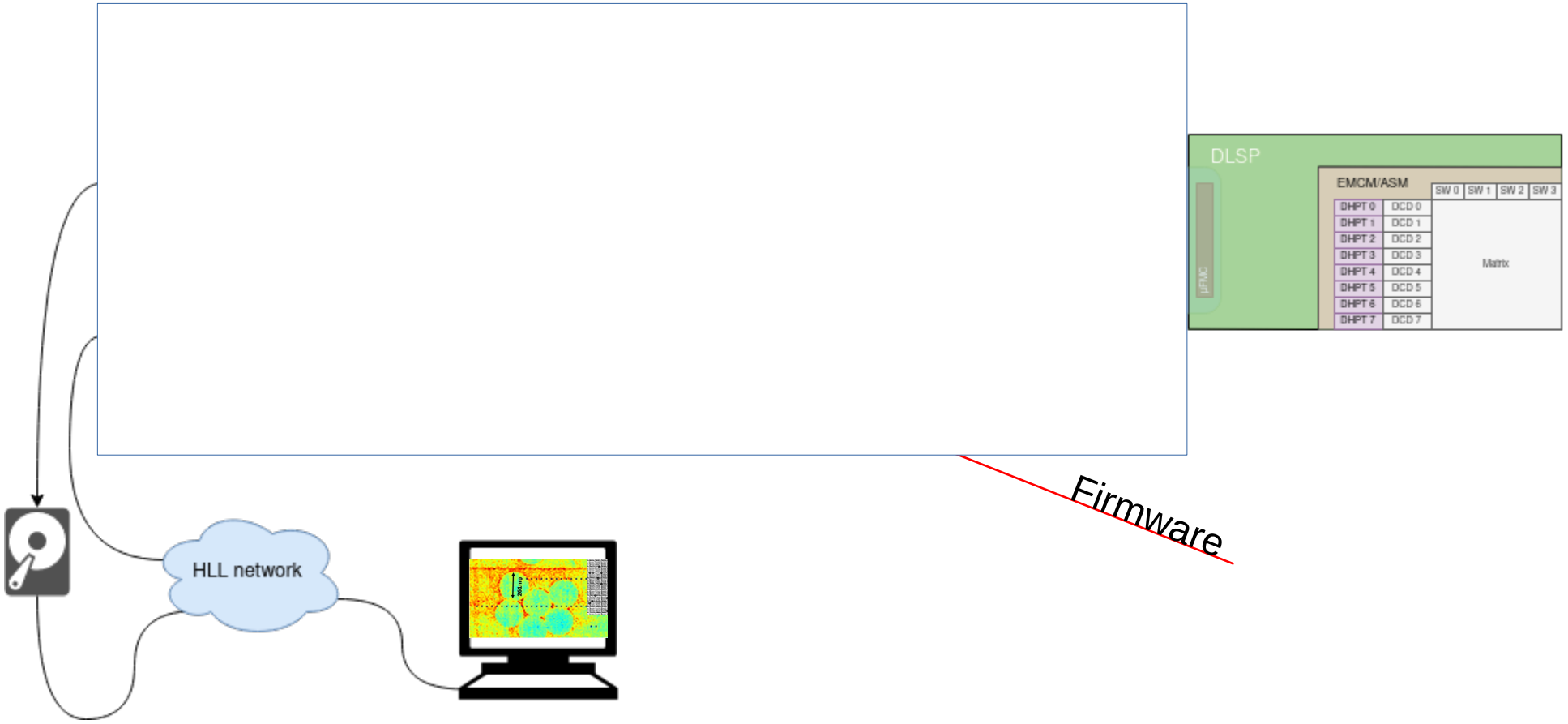
Thank you for your attention

Questions, suggestions, remarks are welcomed.



EDET80K BLOCK SCHEME

Data path

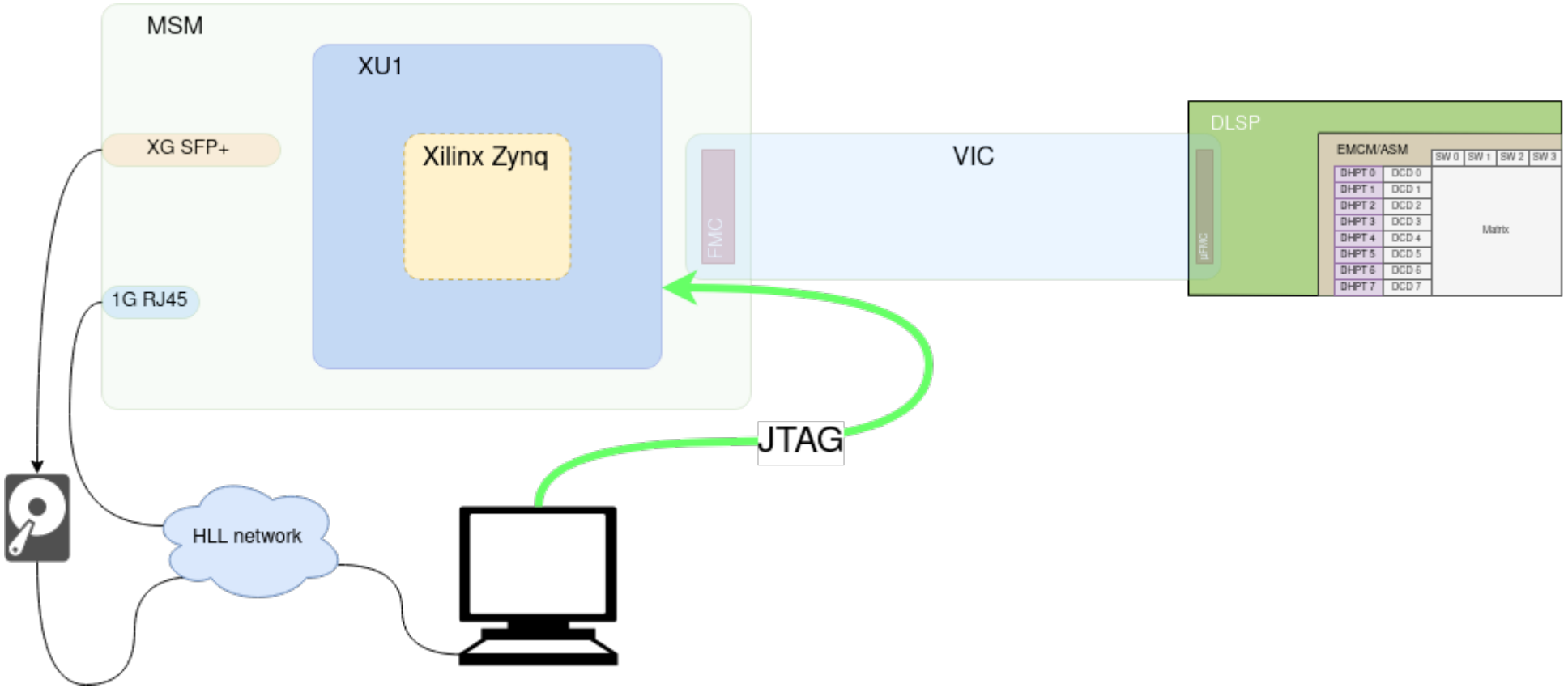


TASKS AND CHALLENGES

- Boot up (QSPI, DHCP, FSBL, UBOOT, Linux, filesystem, device tree, drivers, etc.)
- Configure the firmware, know the status
- Simulation
- Get, process and transmit the data
- Debug
- Transfer knowledge (how to use)

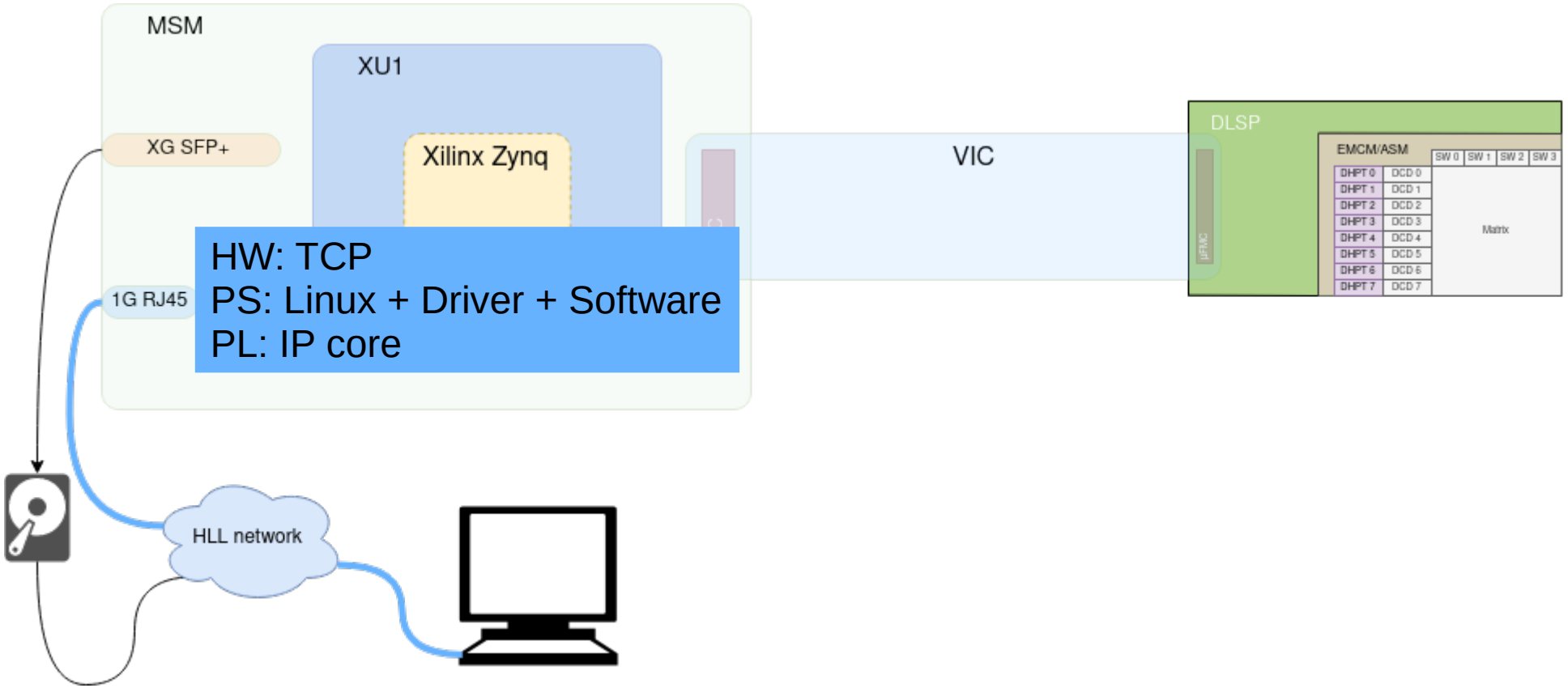
FIRMWARE DEBUG

Old

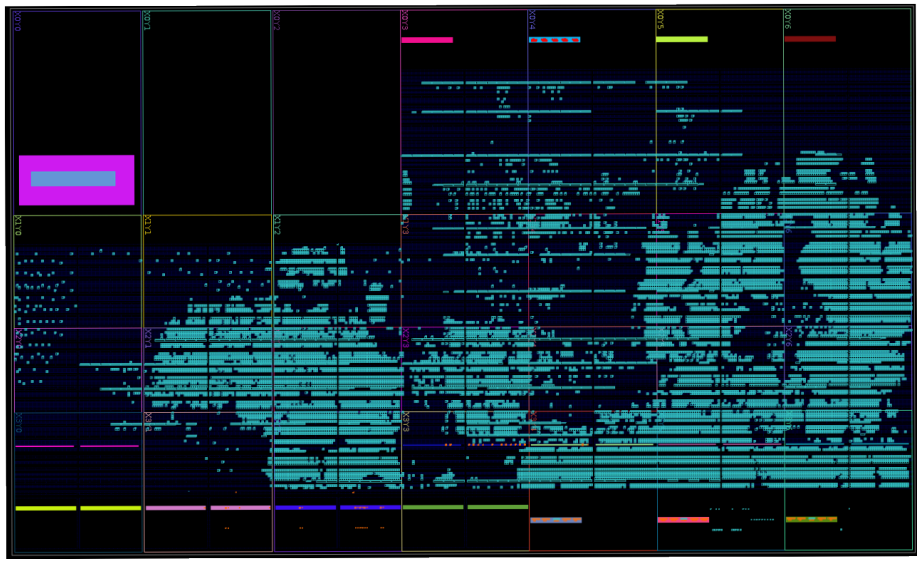


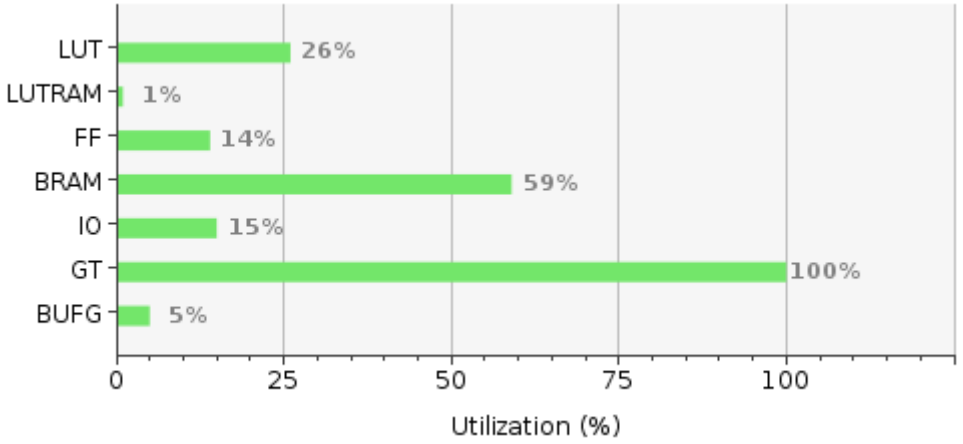
FIRMWARE DEBUG

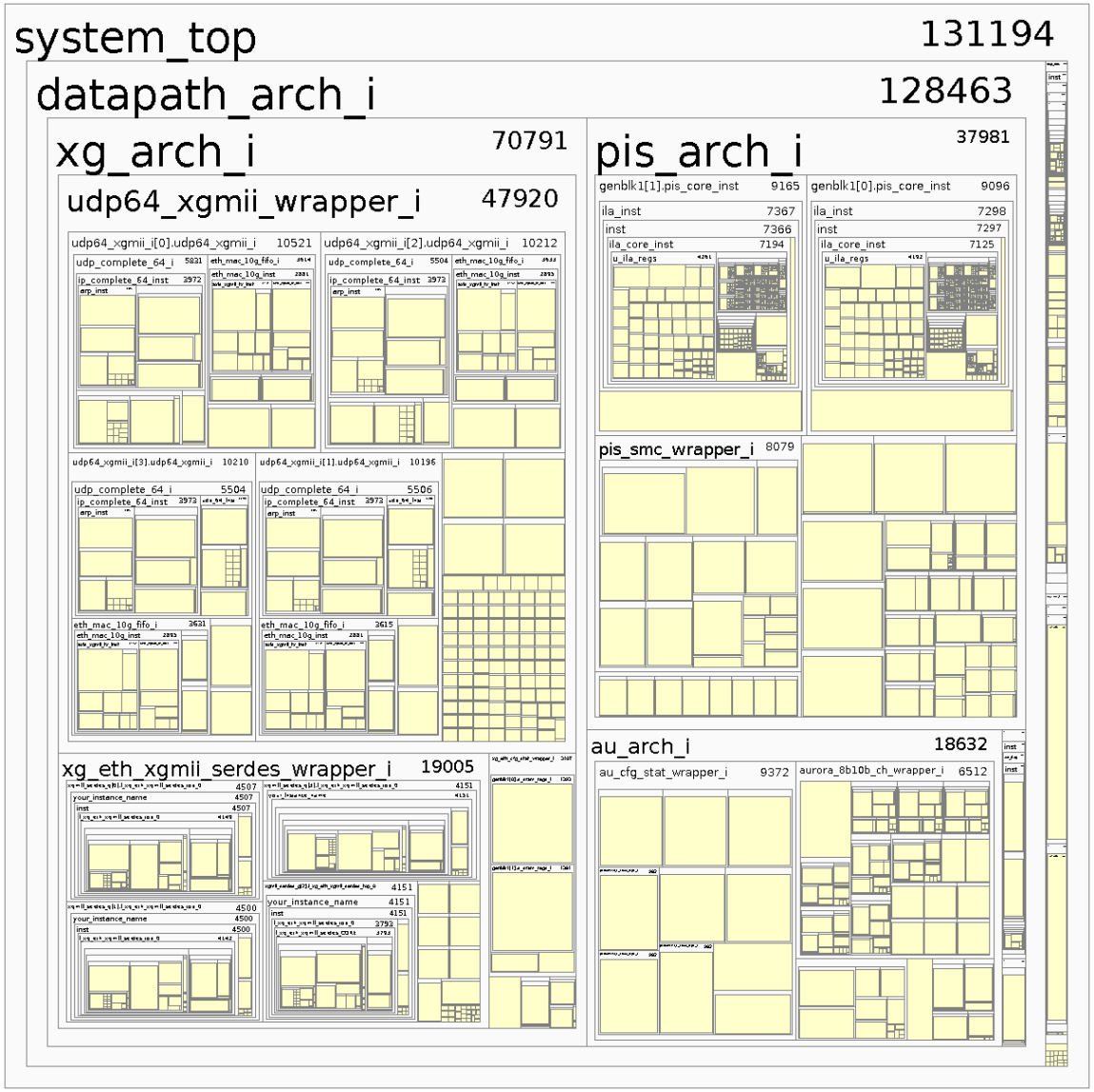
Less cables – less problems



FPGA UTILIZATION

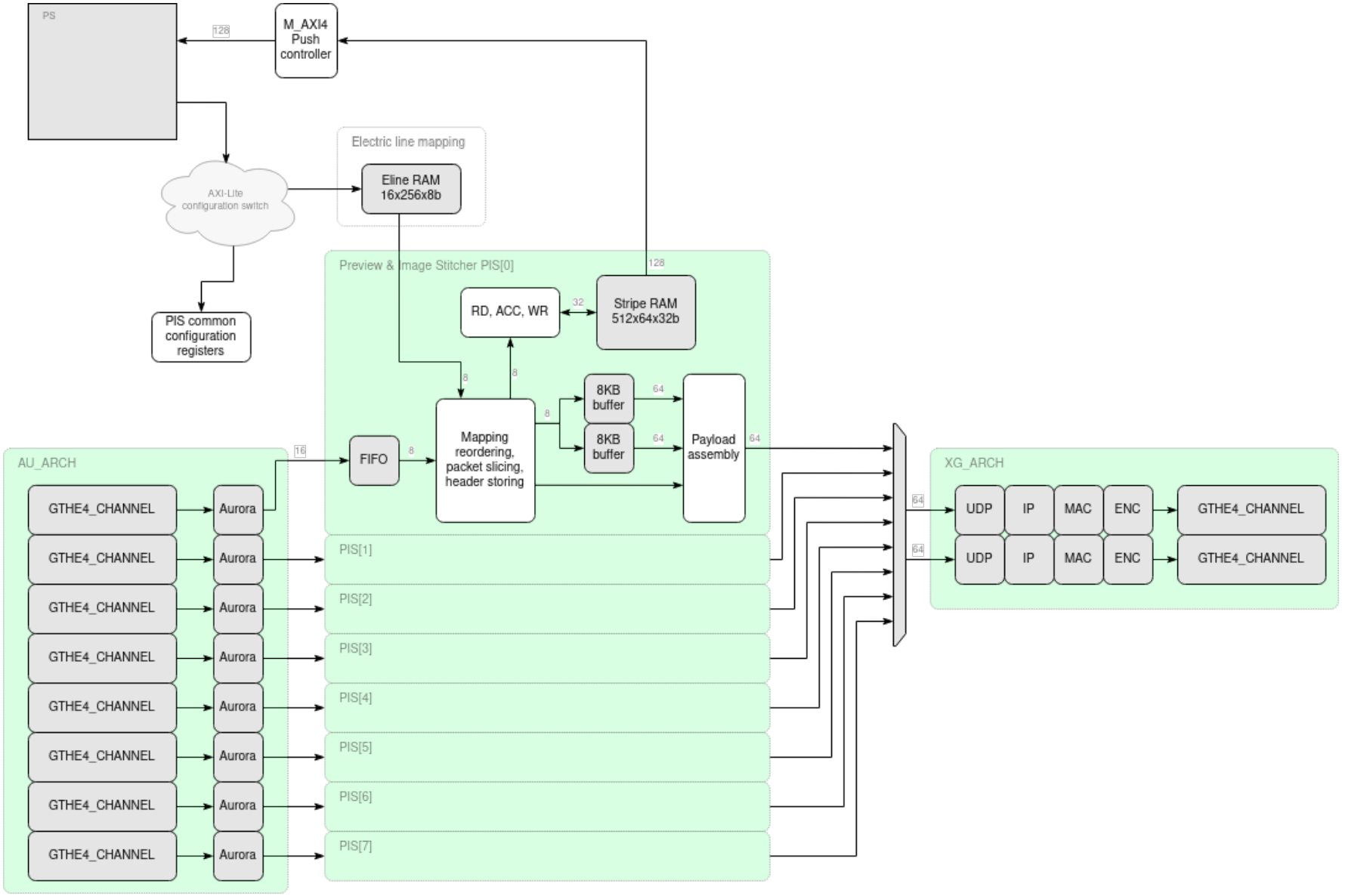


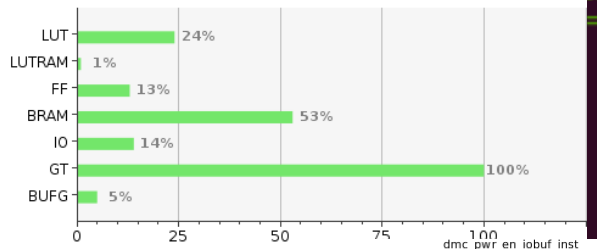


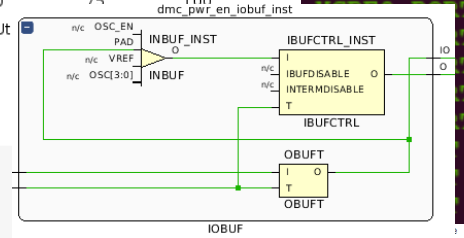


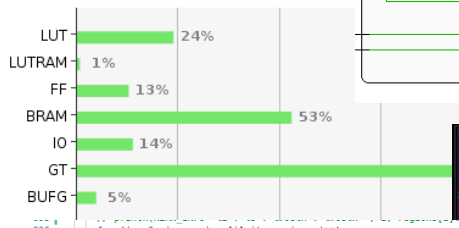
TOOLS USED

- **HDL: (System)Verilog, VHDL**
- **Scripting: Shell, TCL**
- **Software: Xilinx Vivado, Cadence Xcelium**
- **Packages: Linux, Buildroot, Uboot, etc.**
- **Paradigm: command line interface, scripting**

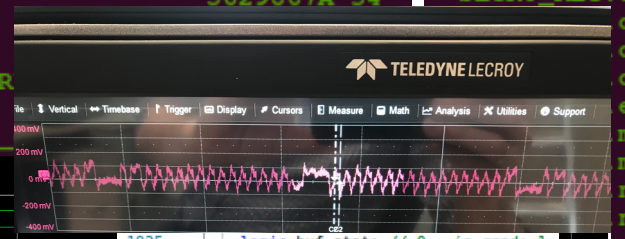

PS
128
M_AXI4 Push controller
Electric line mapping
AXI-Lite configuration switch
Eline RAM 16x256x8b
PIS common configuration registers
Preview & Image Stitcher PIS[0]
128
RD, ACC, WR
32
Stripe RAM 512x64x32b
8
8
8KB buffer
8KB buffer
64
64
8
Payload assembly
64
FIFO
8
Mapping reordering, packet slicing, header storing
16
AU_ARCH
GTHE4_CHANNEL
Aurora
PIS[1]
PIS[2]
PIS[3]
PIS[4]
PIS[5]
PIS[6]
PIS[7]
64
64
XG_ARCH
UDP
IP
MAC
ENC
GTHE4_CHANNEL

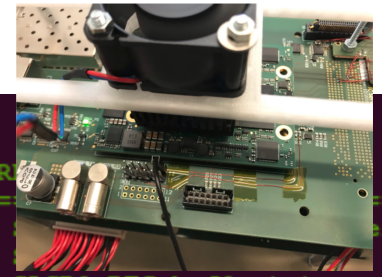






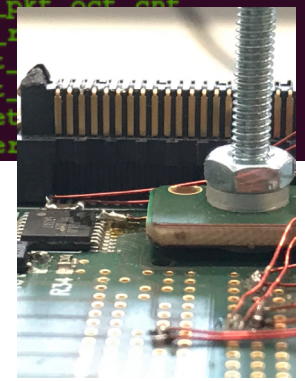

```
# ./cfg.sh xgstat 0

REGISTER NAME                                    VALUE 44
================================================== 44
XGBE0_PORT.QPLL0LOCK                             00000001 43
XGBE0_PORT.GTPOWERGOOD                           00000001 42
XGBE0_PORT.TXRESETDONE                           00000001 41
XGBE0_PORT.TXPMARESETDONE                        00000001 40
XGBE0_PORT.TXBUFSTATUS                           00000000 39
XGBE0_PORT.TXDATA_L                              17043BFA 38
XGBE0_PORT.TXHEADER                              00000002 37
XGBE0_PORT.RXRESETDONE                           00000001 36
XGBE0_PORT.RXPMARESETDONE                        00000001 35
XGBE0_PORT.RXDATA_L                              5629867A 34
XGBE0_PORT.RXBUFSTATUS
XGBE0_PORT.test
UDP0_PORT.CFG_ARP_CACHE_R
UDP0_PORT.CFG_GATEWAY
UDP0_PORT.CFG_INTERFRAME_
UDP0_PORT.ETH_AXIS_RX_BUSY_CNT
UDP0_PORT.ETH_AXIS_RX_ERR_HET_CNT
UDP0_PORT.ETH_AXIS_TX_BUSY_CNT
UDP0_PORT.IP_RX_BUSY_CNT
UDP0_PORT.IP_RX_ERR_HET_CNT
UDP0_PORT.IP_RX_ERR_INVCS_CNT
UDP0_PORT.IP_RX_ERR_INVHDR_CNT
UDP0_PORT.IP_RX_ERR_PET_CNT
UDP0_PORT.IP_TX_BUSY_CNT
UDP0_PORT.IP_TX_ERR_ARP_FAIL_CNT
UDP0_PORT.IP_TX_ERR_PET_CNT
UDP0_PORT.MAC_RX_ERR_BADFR_CNT
UDP0_PORT.MAC_RX_ERR_FCS_CNT
UDP0_PORT.MAC_RX_FIFO_BADFR_CNT
UDP0_PORT.MAC_RX_FIFO_GOODFR_CNT
UDP0_PORT.UDP_RX_ERR_PET_CNT
UDP0_PORT.UDP_TX_ERR_HET_CNT
```





```
                                                 VALUE 27
================================================== 27
                                                 00002710 26
                                                 00000000 25
SLCR0_REG.buf0_stat                              00000000 24
SLCR0_REG.buf1_stat                              00000000 23
SLCR0_REG.ch_rdy                                 00000000 22
                                                 00000001 21
                                                 00000000 20
                                                 00000001 19
                                                 00000001 18
                                                 00000000 17
                                                 00000000 16
                                                 00000000 15
                                                 00000000 14
                                                 00000835 13
                                                 0000001D 12
                                                 00000000 11
                                                 00000000 10
                                                 00000001 9
                                                 00000002 8
                                                 00000004 7
                                                 00000000 6
                                                 00000000 5
                                                 00000000 4
                                                 00000000 3
                                                 00000000 2
                                                 00000010 0
```

```
1925    logic buf_stat; // 0 - is read; 1
1926    logic [12:0] bytes_written;
1927    logic [31:0] dhpt_hdr;
1928  } nbuf_status_t;
1929
1930  typedef struct packed{
1931    logic [8:0] y_offset;
1932    logic [2:0] stripe_num;
1933    logic [3:0] x_offset;
1934  } quarter_addr_t;
1935
```

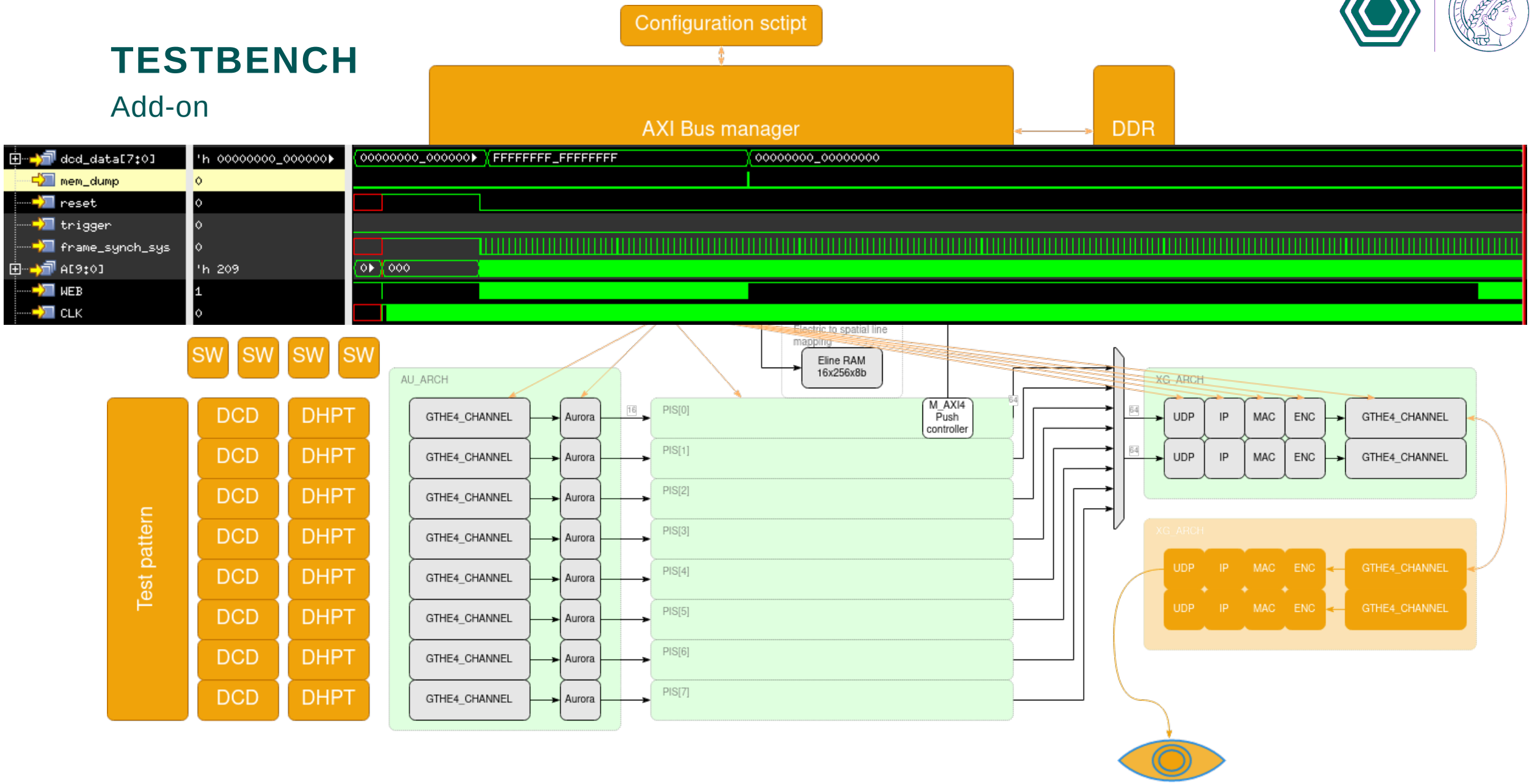


```
# sh cfg.sh austat
AU_0_CDR:. X
AU_1_CDR:.............................. Ok
AU_2_CDR:. X
AU_3_CDR:. X
AU_4_CDR:.............................. Ok
AU_5_CDR:.............................. Ok
AU_6_CDR:. X
AU_7_CDR:. X
```

```
##    TODO:
##  + Include Vivado_HLS design flow in order to remove out of git repository
##    dependencies;
##  + Provide different run modes. (e.g. regenerate IPs, simulate, etc.)
##  - Include $BUILD_DATE, $BUILD_TIME into BRAM init file and connect the RAM
##    block to AXIL bus.
##  + Get rid of BD file. Transfer all the IPs to HDL. ?
```

TESTBENCH

Add-on



DOCUMENTATION

Wiki pages / git repositories

https://fsteam.hll.mpg.de

Welcome to FSTEAM Wiki

Contents [hide]

1 What is it for?
2 Common
3 Projects
3.1 EDet80k
3.1.1 Brief
3.2 TNG (FSP)
3.2.1 Brief
3.3 SPIX
3.4 GREST
3.5 DANAE
4 Design Software

MSM

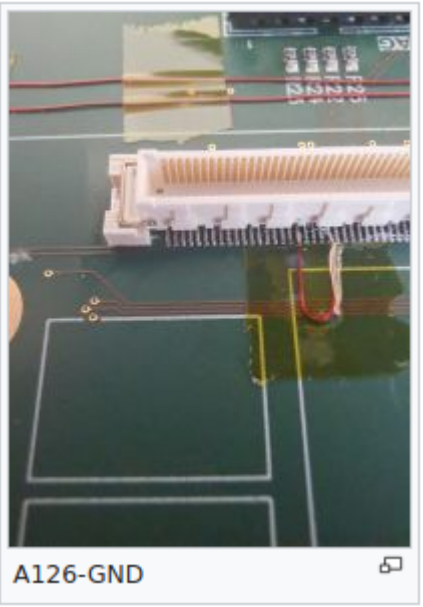
Contents [hide]

1 Description
2 Schematics
3 Errata list
4 History
4.1 May 2019
4.2 Jan 2020
5 Status

#	GPIO	Dir*	Name	Notes**
	06	OUT	JTAG_TDI	
	07	OUT	JTAG_TCK	
	08	OUT	JTAG_TMS	
	09	IN	JTAG_TDO	
	00	OUT	JTAG_CLK_TRG_OE_N	1 - puts JTAG in Z-state
	01	OUT	ADAPTER_DLSP_SWITCH	0 - adapter, 1 - DLSP
				PULLUP
				PULLUP
				PULLUP
15	51			

Contents [hide]

1 Zynq UltraScale+
1.1 Processing system(PS)
1.1.1 Quad Cortex A53
1.1.2 Dual Cortex-R5
1.1.3 GPU Mali-400
1.2 Programmable logic(PL)
1.2.1 Design structure
1.2.2 Accessing registers
1.2.3 Driver installation and removal
1.2.4 Driver repository



A126-GND

EDet80k

Brief [edit]

- Project owner: Johannes Treis
- Hardware components used in EDet project:

  MSM -- XU1 -- PSP -- PPM -- DLSP -- VIC -- E1Hybrid -- ASM
- Software tools:

  SVF player -- Virtual instrument
- Test setups:

http://persei.hll.mpg.de:3000/ #2 (Calibration

TNG (FSP) [edit]

Brief [edit]

- Project owner: Alexander Bähr
- Hardware components used in TNG project:

  MSM -- XU1 -- MCM --