universitätbonn

SI LAB
Silizium Labor Bonn

Data Handling Processor v0.1
Preliminary Test Results - August 2010

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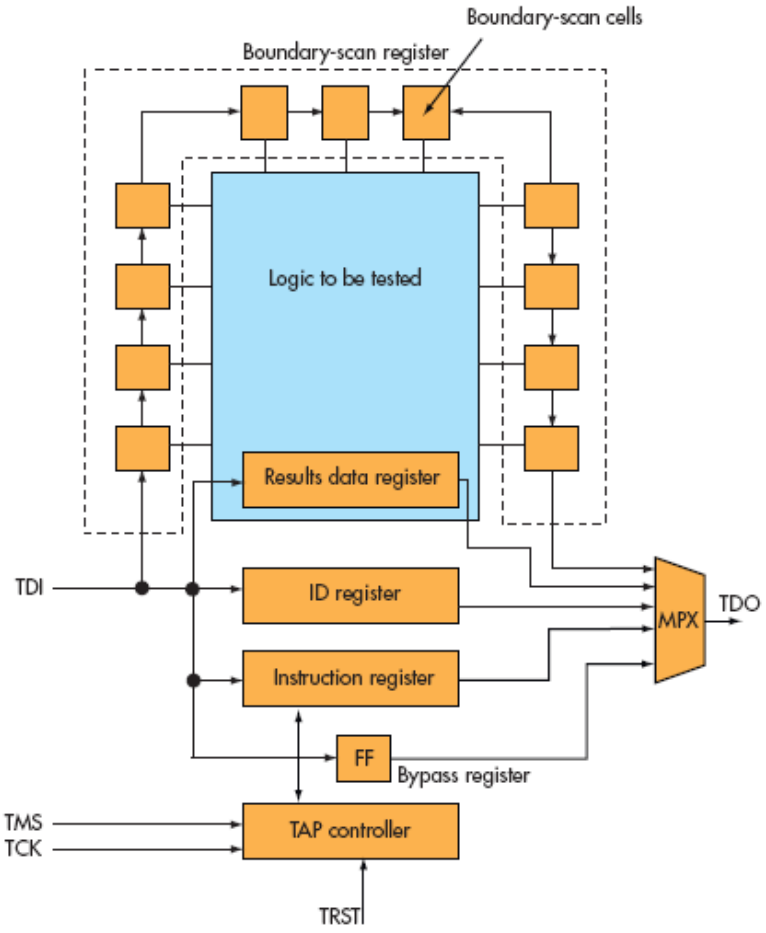
DHP01 Overview

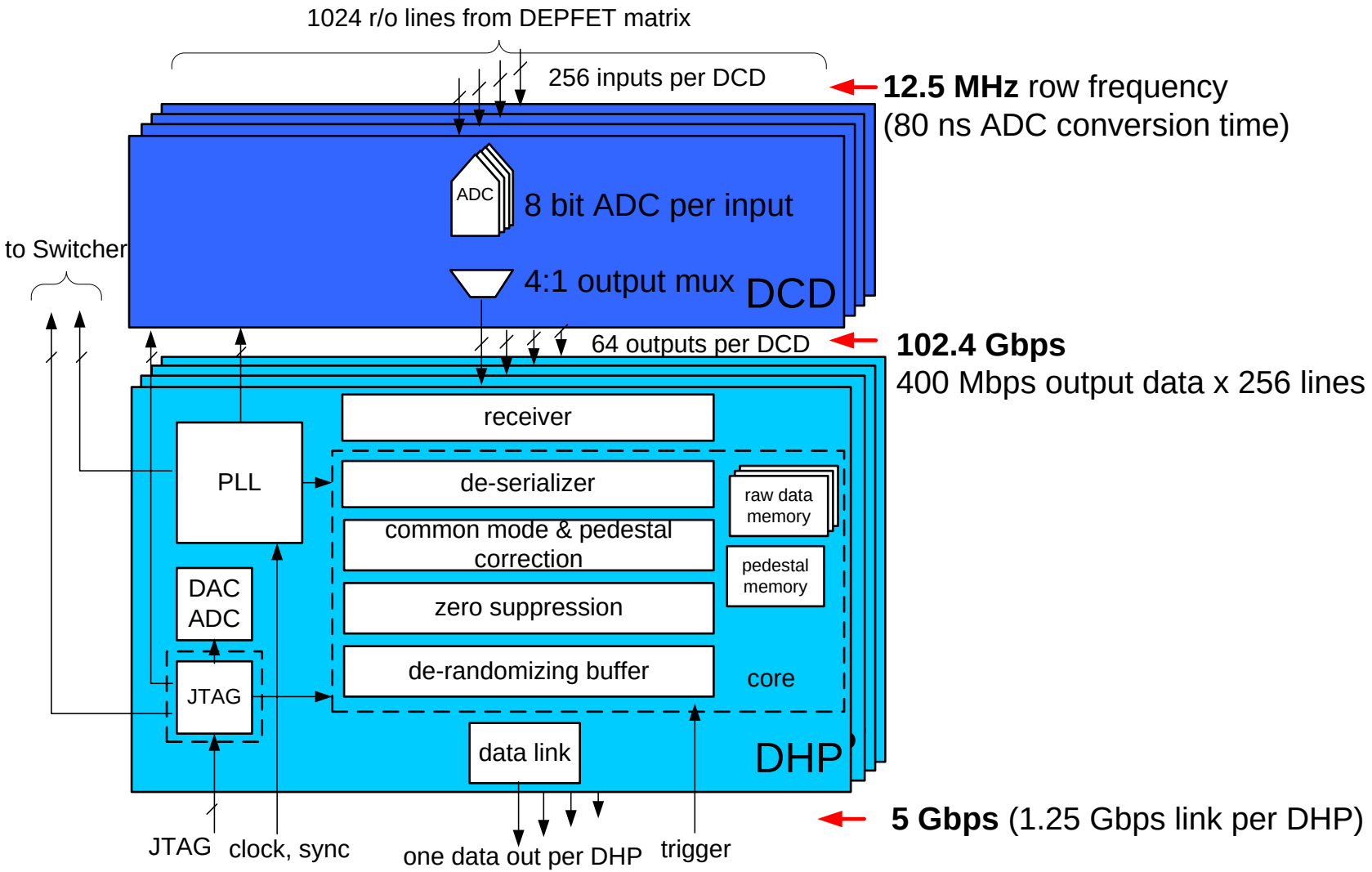
- Technology
  - IBM 90nm – 9 metal layer
  - 1.2 core / 1.8 IO voltage
- Interface
  - 32 (4x8) 400 MHz inputs from DCD (HSTL18)
  - LVDS control signals (clock, trigger, sync)
  - CMOS JTAG
  - Hi-speed CML output
- Internal Blocks
  - Common mode correction
  - Pedestal subtraction (static and dynamic*)
  - Zero suppression (threshold)
  - Channel framing and serialization
  - DCD offset correction
  - Raw data storage up to (2048 rows)
  - Sequencer for switcher
  - Configurable delays
  - Clock generation (PLL)
  - Configurable trigger latency (up to 1024 rows)
  - Slow control (JTAG)
  - ADC & DAC

Slow control - JTAG

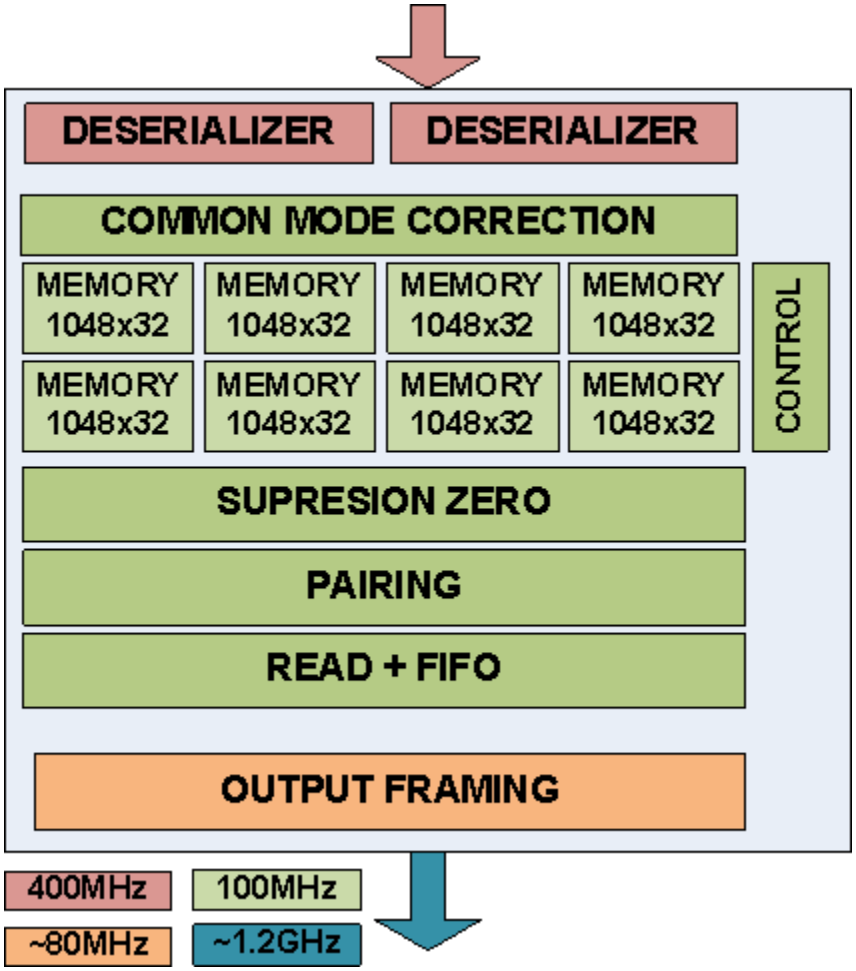


- Boundary scan
  - EXTEST
  - SAMPLE
  - PRELOAD
  - INTEST
- Configuration
  - BYPASS
  - IDCODE
  - USERCODE
  - ADC
  - BG
  - CORE_READBACK
  - CORE_REG
  - DAC
  - DACENC
  - GLOBAL_REG
  - MEM_ADDRESS
  - MEM_DATA
  - OFFSET_MEM_ADDR
  - OFFSET_MEM_DATA

DHP – Signal Rates & Data Flow



Processing



- Deserializer (1 to 4)
- Common mode correction
- Buffering for latency
- Pedestal correction
- Hit Pairing
- Readout
- Output framing

Operating modes

- MEMORY ACCESS

  Allows to access memory block through JTAG interface for pedestal and offset correction.

- RAW DATA RECORD

  Storing raw data to memory (support for trigger).

- RAW DATA SEND

  Sending through fast output link all memory contents.

- AQUSITION

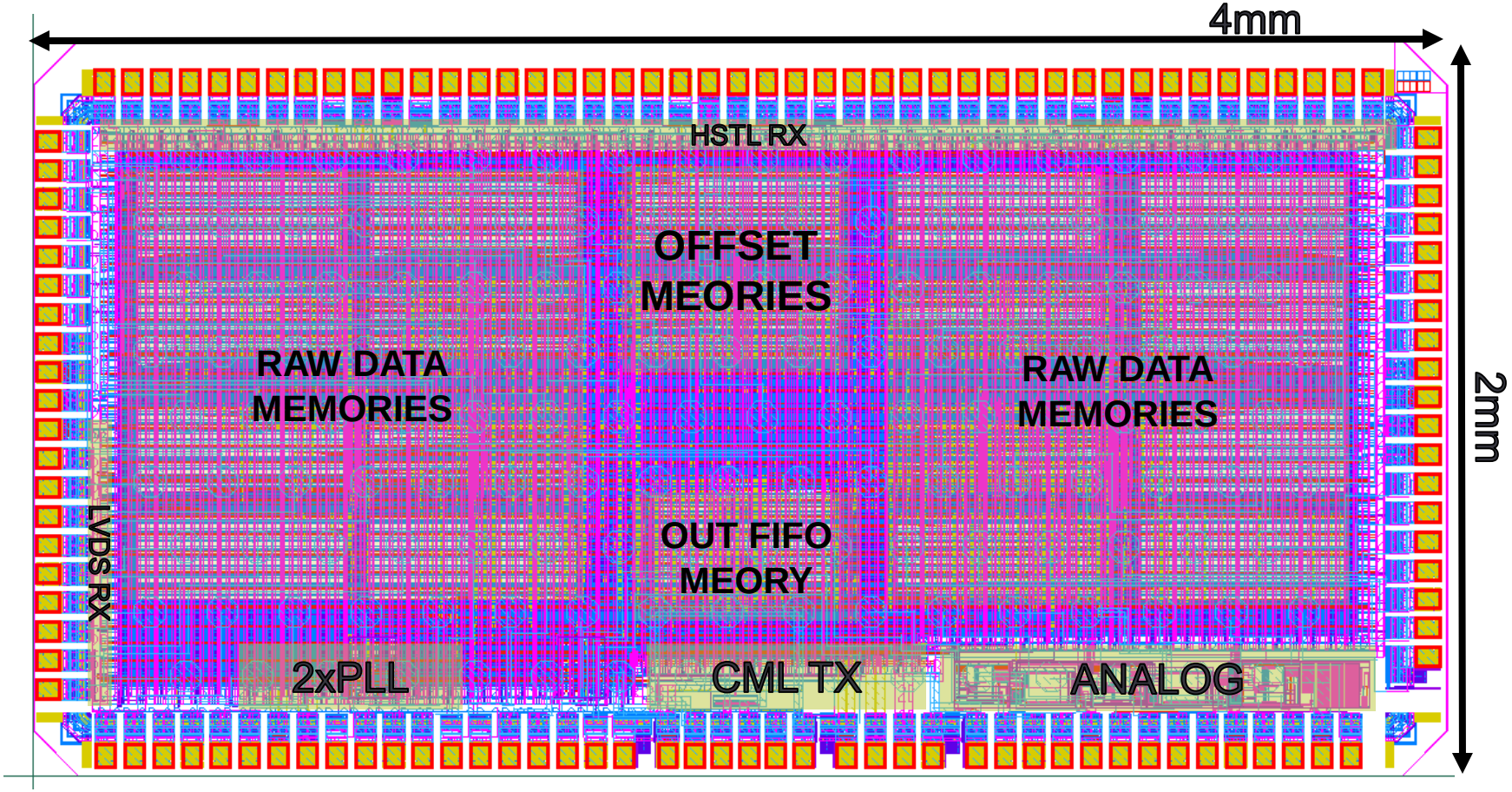
  Normal operation mode where data are going through all processing stages. Support for trigger and latency buffering.

- TEST

  Like AQUSITION but new data are not being recorded.

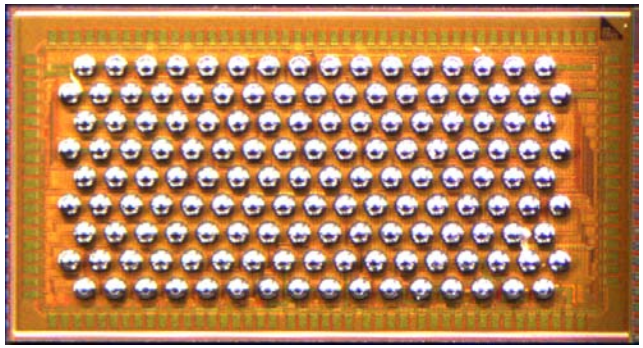
DHP01 - Layout

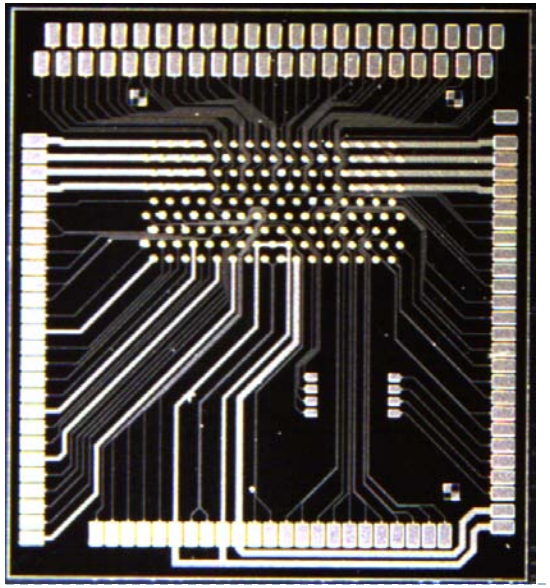
- Prototype with 32 input chip

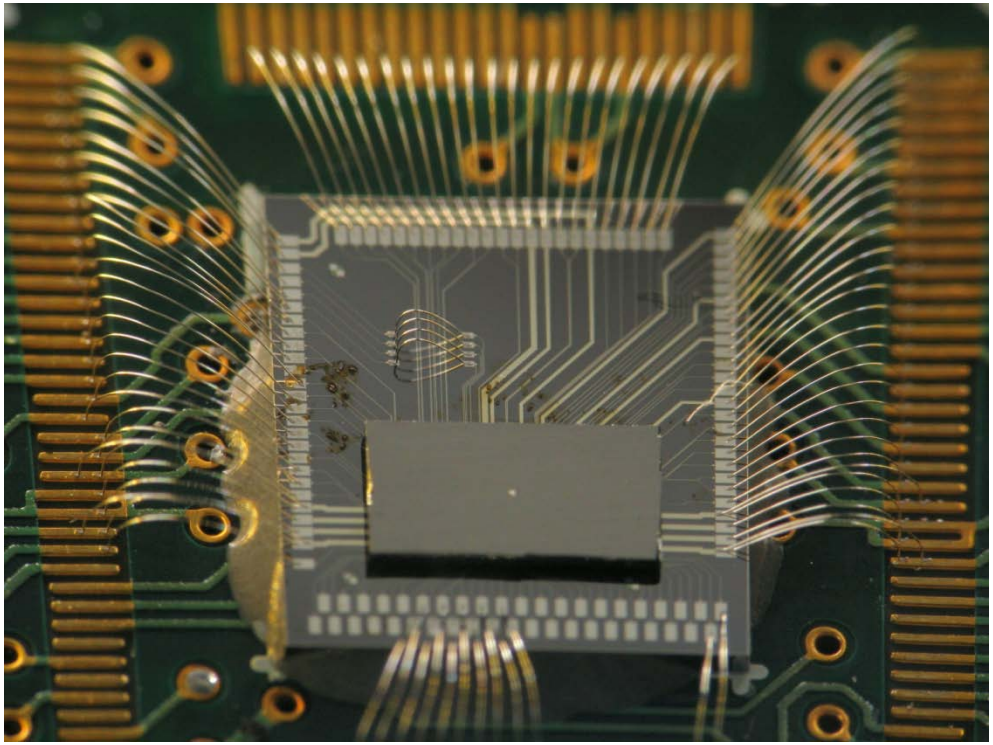


~5.5mln transistors

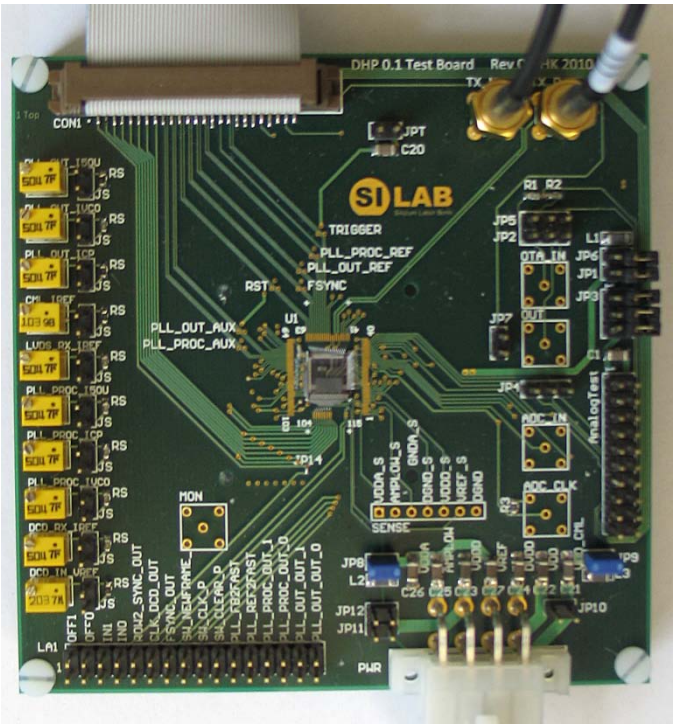
DHP01 – Bump bonding





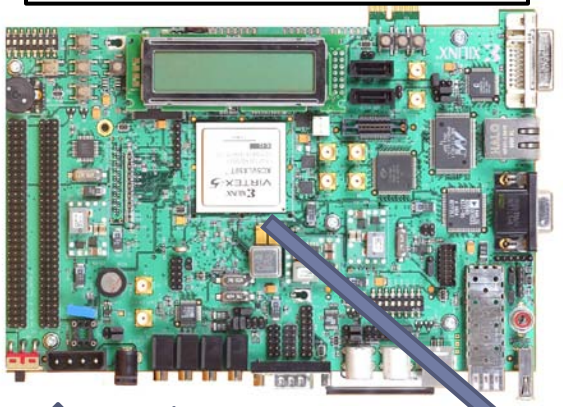


Test Setup



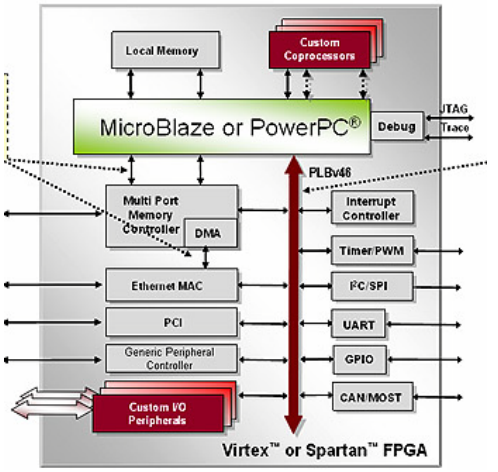
GPIO
SMA/Coax

Xilinx XUPV5-LX110T



ETHERNET/
UDP/TCP/IP

UART



Testing till now

Looks to be working:

- LVDS Input
- HSTL like Input (from DCD)
- Slow control (JTAG)
- Memories read/write
- CML Hi-speed link (tested up to 1.555 GHz) data transition
- Input readout
- Patter generator

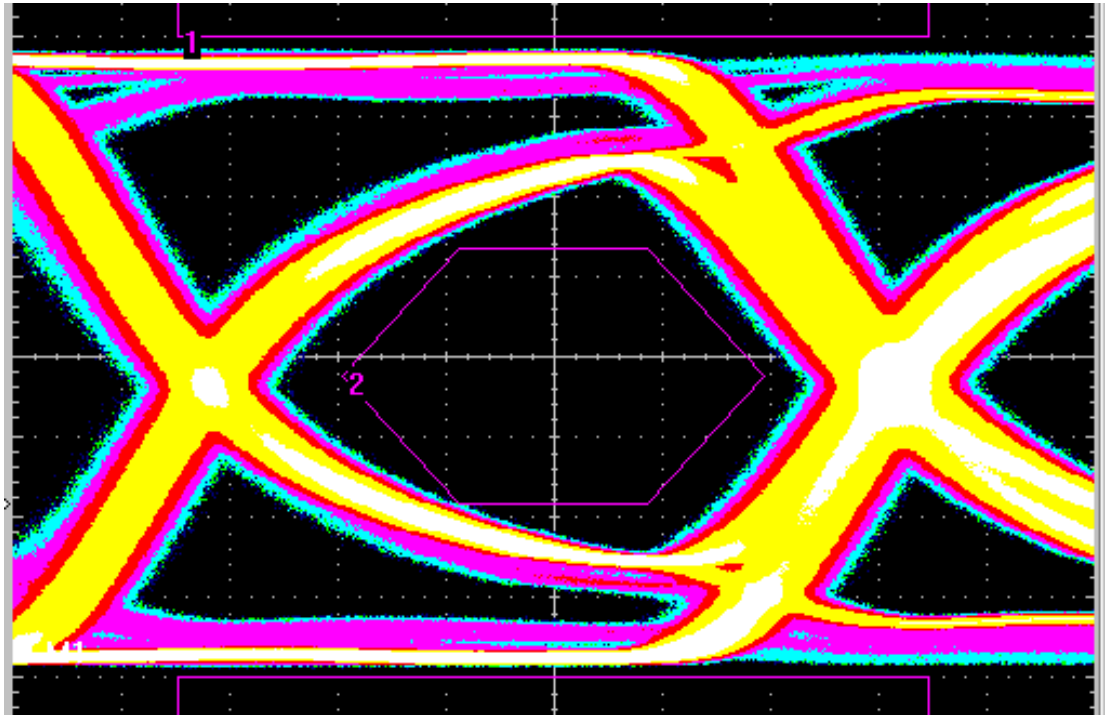
To Do:

- Analog parts
- Processing (different configurations)
- DCD communication and synchronization

Power

- Measurement conditions:
  - 1.2 V, 400MHz (100MHz Core)
- Current consumption:
  - CML TX - ~25 mA
  - 2xPLL - ~5mA
  - digital core - ~60mA

PLL and CML



- 1.5552 GHz – data transmission (random 8b10b)
- WB + ~5 cm PCB + SMA +~40cm coaxial cable + SMA
- 100 ps/div
- 100 mV/div

Problems till now

- Looks like CMOS output pads can work till ~100MHz so unable to test with DCD at 400 MHz
- Configuration of one PLL output (slow one) not fully accusable (simple bug known from submission) there is a workaround

-> More results in Valencia

Timeline

- Finish test setup to be ready for hi-speed data accusation
- Prepare setup with DCDB
- Radiation tests

- DHP 1.0:
  - scale design to full size chip → (beginning/middle of 2011)

- ***Need to know exact processing algorithm (needed corrections and data sizes) !***
- ***Need to know final number for occupancy***

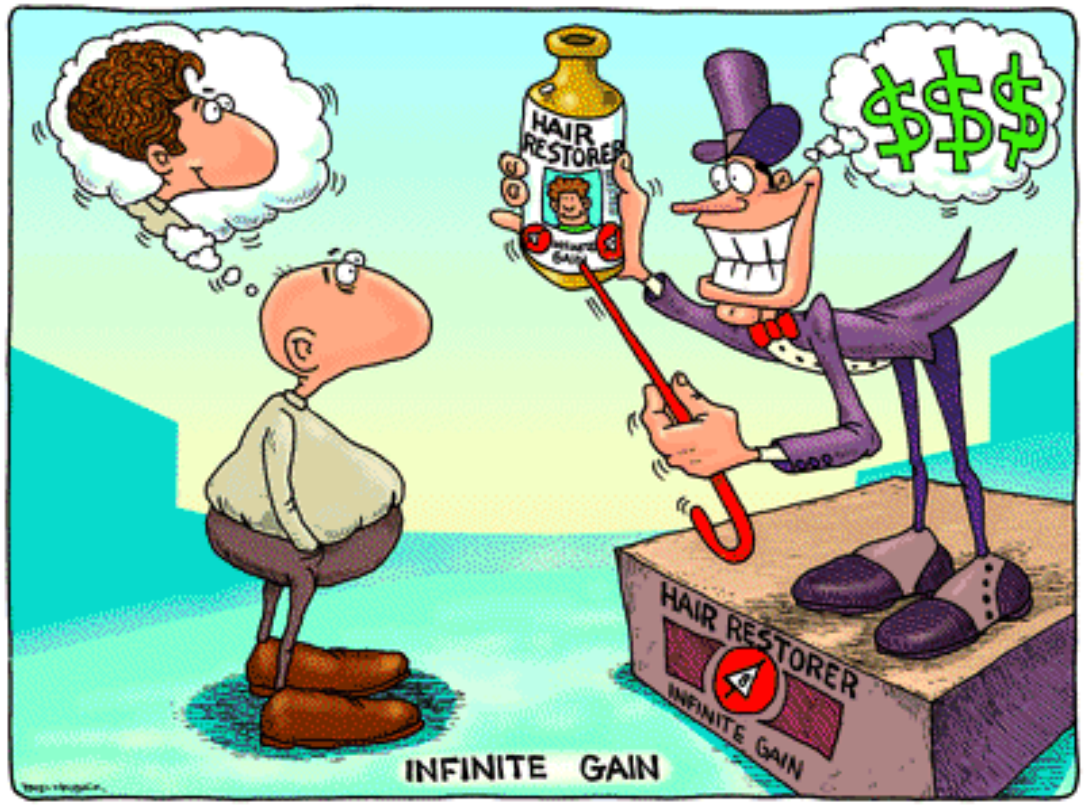
Thank to

Bonn:

- Hans Krüger
- Andre Kruth
- Mikhail Lemarenko
  - and others

Barcelona:

- Albert Comerma
- Angel Dieguez
- Lluıs Freixes
- Eva Vilella
  - and others



Thank You.