DHH Status

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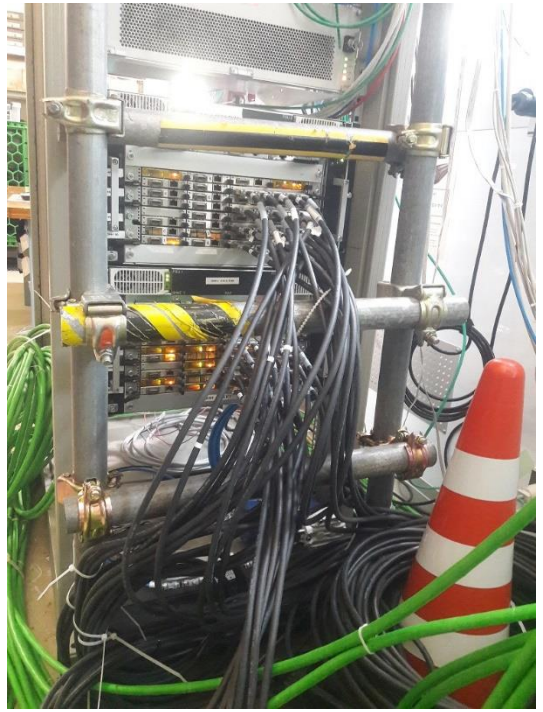
PXD and DEPFET Workshop 22-24.05.2023

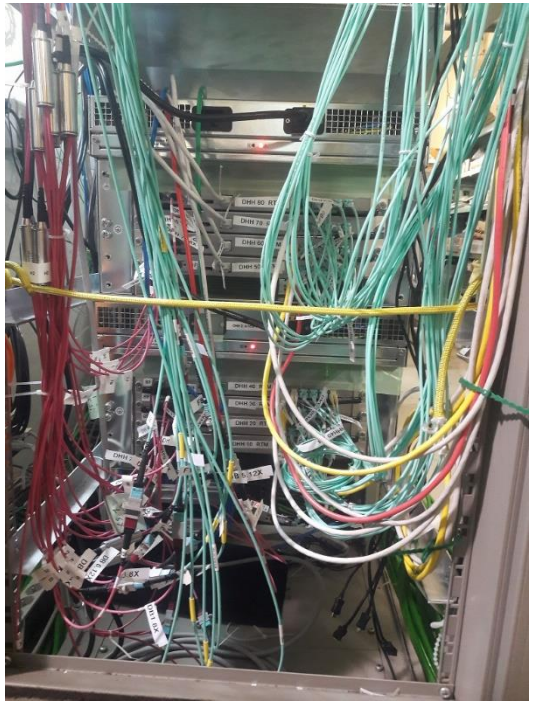
Outline of Talk

- DHH Status
- DHH Carrier Card Upgrade

DHH Status at KEK

- DHH for PXD2
  - DESY DHH
  - PXD1 DHH
- Quite smooth commissioning
- Provision of special X-switch configuration for DHH tests with single DHP link
- No big issues
  - ripped of USB connector together with usb cable => repaired by exchanging JTAG-USB controller at KEK
  - Loose FTSW connector on one of DHHRTM, no handshake with FTSW
  - Careful work around rack is required
  - Arranging cables in safe way for final installation using cable channels
  - Exchange of 2 DHE modules due to unstable power switch behavior





Remaining DHH Issues

FTSW Links

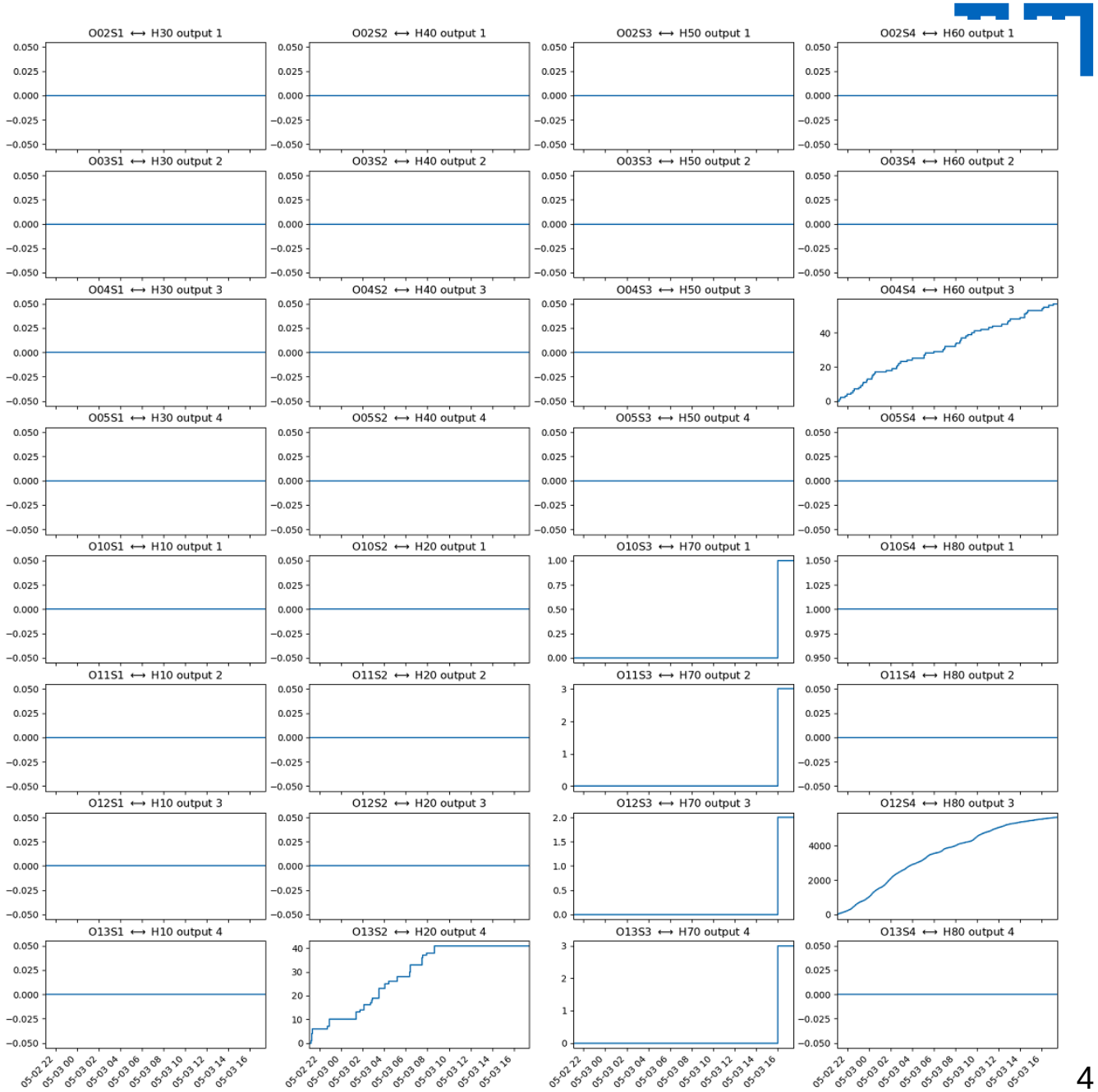
- DHH70 handshake with FTSW not established

Instable ONSEN links

- DHH20.4
- DHH60.3
- **DHH80.3**

Origin of the problem and solution

- Not fully plugged connector between CC <=> RTM
- Small displacement of connector in the design



DHH UPGRADES

DHH Carrier Card Upgrade

DHE1	DHC	DHE4	DHE5
DHE2	DHE3	DHI	

Change of DHH Carrier Card layout

- PCB layer stack optimized for matched impedance transmission lines
- Rearranged DHC position to minimize HS link traces' length
- Improved layout for high speed links
- All external transceivers mounted on DHHCC no RTM

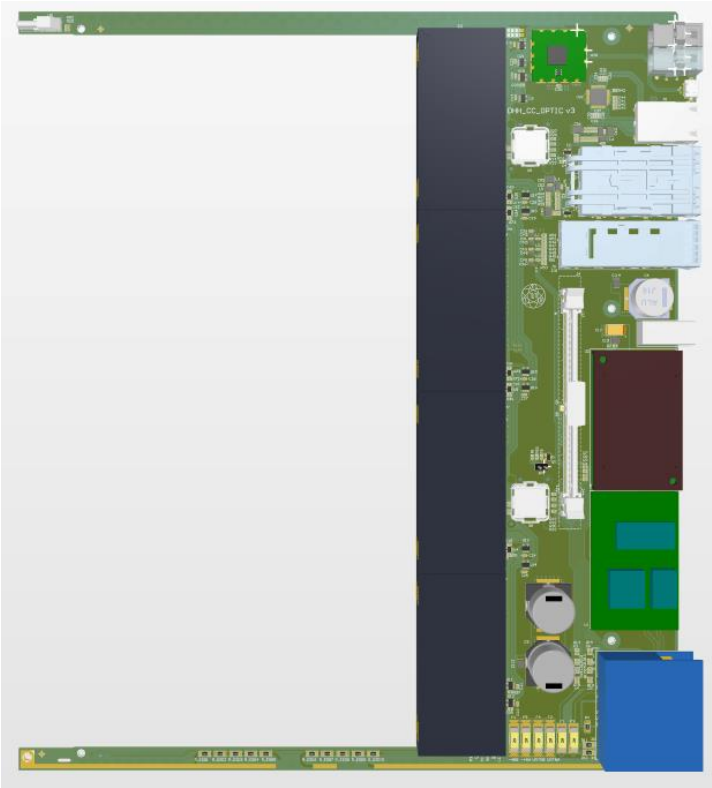
Test of the prototype

- JTAG - OK
- ONSEN links, FTSW, IPBUS - OK
- FTSW - OK
- Test of DHC-DHE/DHI link tests
- DHE5 and DHI suffer from signal deteriorate after longer traces
- Still room for optimization of driver and receiver parameters

Preparation for production

- Change layout LConnect DHE5 and
- Submit final production

Module	Error rate	Trace length
DHE1	10^-11	Tx : 119 mm Rx : 112 mm
DHE2	10^-11	Tx : 89 mm Rx : 99 mm
DHE3	10^-11	Tx : 39 mm Rx : 33 mm
DHE4	10^-11	Tx : 123 mm Rx : 121 mm
DHE5	10^-8	Tx : 188 mm Rx : 180 mm
DHI	10^-8	Tx : 180 mm Rx : 174 mm



DHH Carrier Card Upgrade

Preparation for production :

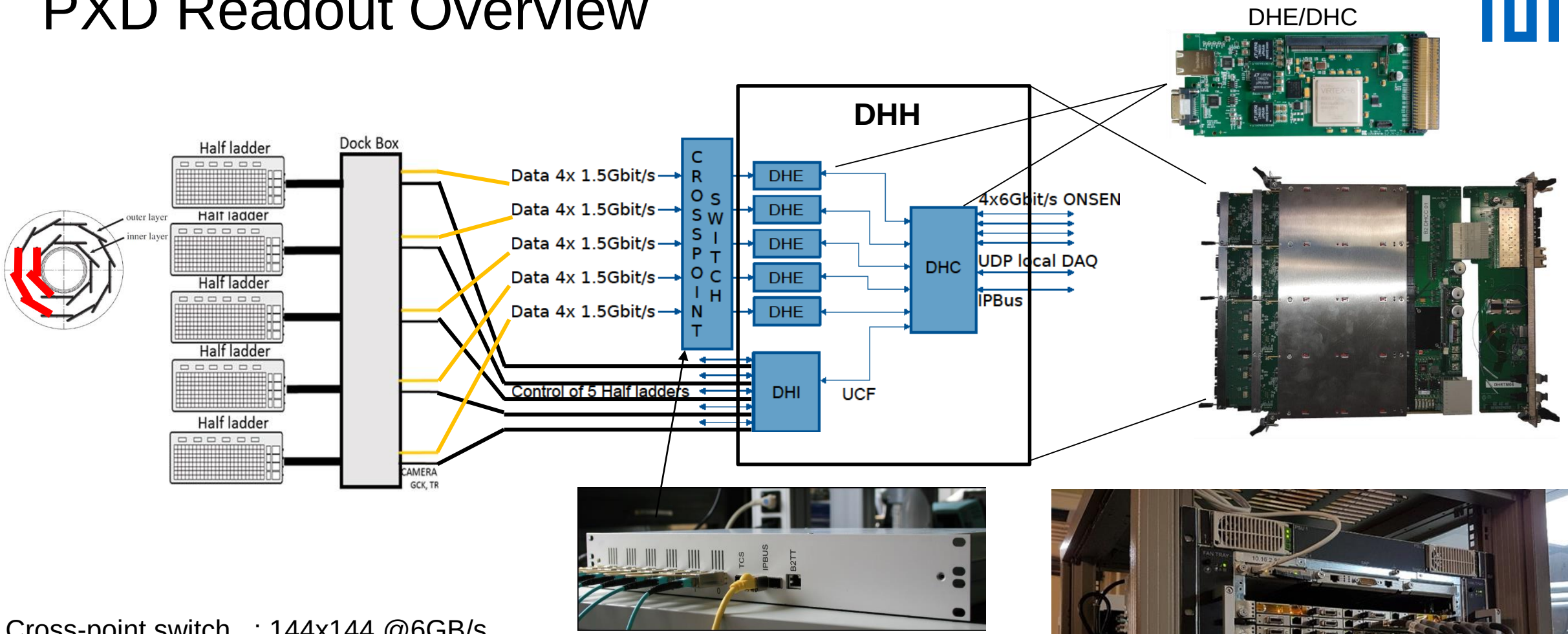
- Change of layout : use external high speed cables for DHE5 and DHI
- Submit full Carrier Card production in June
- Installation : after full commissioning of PXD2 winter break ?

Summary

- DHH and X-switch were successfully commissioned at KEK
- Issue with FTSW link of DHH70 to be investigated
- ONSEN links require extra attention and to be tested and debugged right after DHH moved to final location. Time for that to be allocated.
- Carrier Card was tested and small layout changes were done
- Submit for full production in June

THANK YOU

PXD Readout Overview



Cross-point switch : 144x144 @6GB/s
DHHCC : ATCA
DHI : A7XC100T, Configuration and Trigger
DHE/DHC : V6XC130 FPGA, 4GB memory, Data processing
DHH : DHI + 5xDHE + DHC

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PXD Data Throttling II

1. New data throttling algorithm

- Idea is to prevent overflow of DHP buffers to handle any occupancy
- Extrapolation and prevention of expected full detector occupancy from first one or few first gates
- Provision of active throttling to DAQ with data

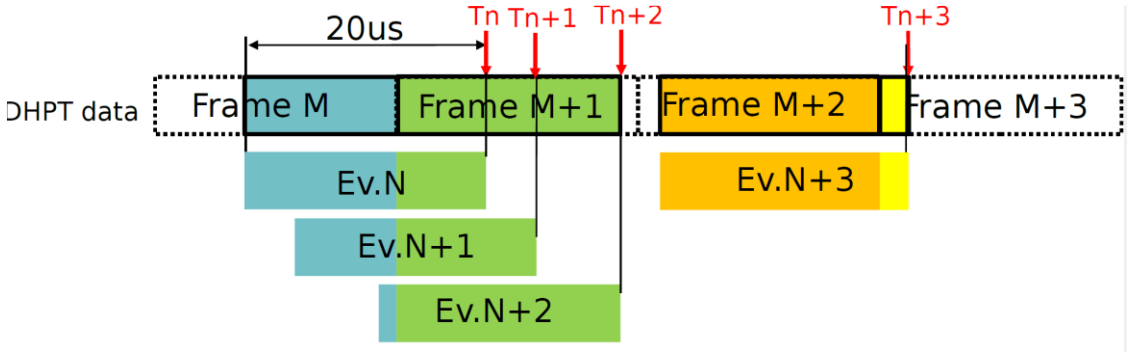
DHC End of Sub Event Frame

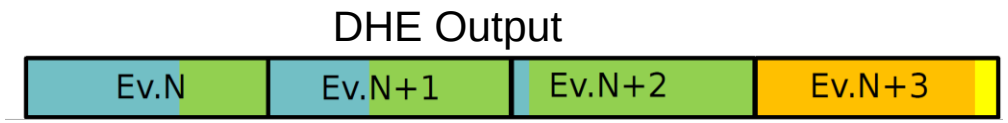
3		2										1										0									
1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0
E	1100				nu		DHC ID, 4b					Reserved										Trigger Nr. 15:0											
32 bit word counter																															
Error word																															
CRC32																															

- Normal operation
  - DHPs run continuously
  - DHE monitors detector occupancy
  - DHE extracts data in time with trigger
- Throttling
  - DHE detects high occupancy and issues VETO
  - DHE VETO => DHC => DHI => DHP
  - VETO valid for one or more FRAMEs
  - VETO conditions
    - Exceeding maximum occupancy of one frame
    - Exceeding maximum occupancy of part of frame
    - Exceeding DHP buffer maximum fill level by monitoring data latency

PXD Data Throttling I

- Fundamental difference of PXD vs other detectors is an integration time of 20 us or 2 KEKB revolution cycles.
- PXD readout based on running shutter. It takes 20 us for one round and each round organizes hits in single FRAME
- B2TT Triger initiates PXD Trigger which is effectively DATA ENABLE signal





- DHPT links' bandwidth allow to read maximum 2.3% occupancy in continuous mode when DATA ENABLE is always active
- Exceeding maximum PXD occupancy causes loss of data and
- at some cases it may cause loss of synchronization of data between DHP and DHE

Single Server Configuration

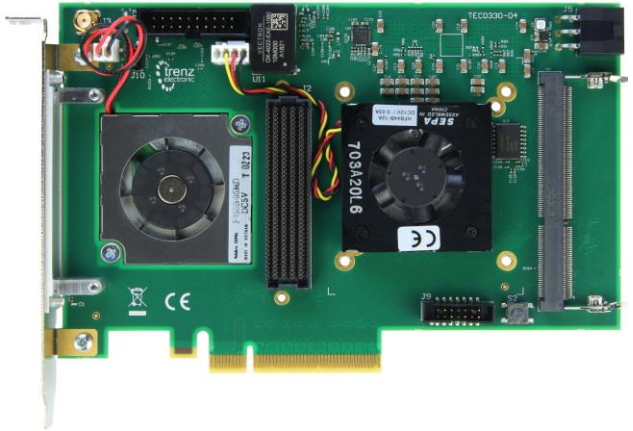
Hardware

PCIE Card from Trenz Electronics GmbH TEC0330

- FPGA Xilinx Virtex-7 XC7VX330T-2FFG1157C
- PCIE 8 lane Gen2, 3 GB/s
- 8 GByte DDR3 memory
- FMC connector with 12 High speed interfaces
- Delivery in January 2024

Server Dell PowerEdge R7515

- 1x7302 AMD CPU, 16 cores
- 128 GB DRAM, extendable to 512 GB
- 2x M.2 SSD 1TB



Main PCIe FPGA functionality

- buffer
- Clustering
- Event building

Main server functionality

- DMA data transfer from PCIe to local memory
- Data buffering till HLT
- Data retrieving and ROI selection
- Interface to EB2

- Missing manpower for software development for this project
- We are looking for a possible solution and we hope to find one