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SI LAB
Silizium Labor Bonn

P. Ahlburg, F. Bernlochner, J. Dingfelder, H. Krüger, B. Paschen, P. Wolf

PXD Power Supply - Over Voltage Protection (OVP) Studies

PXD Workshop and 25th International Workshop on DEPFET Detectors and Applications

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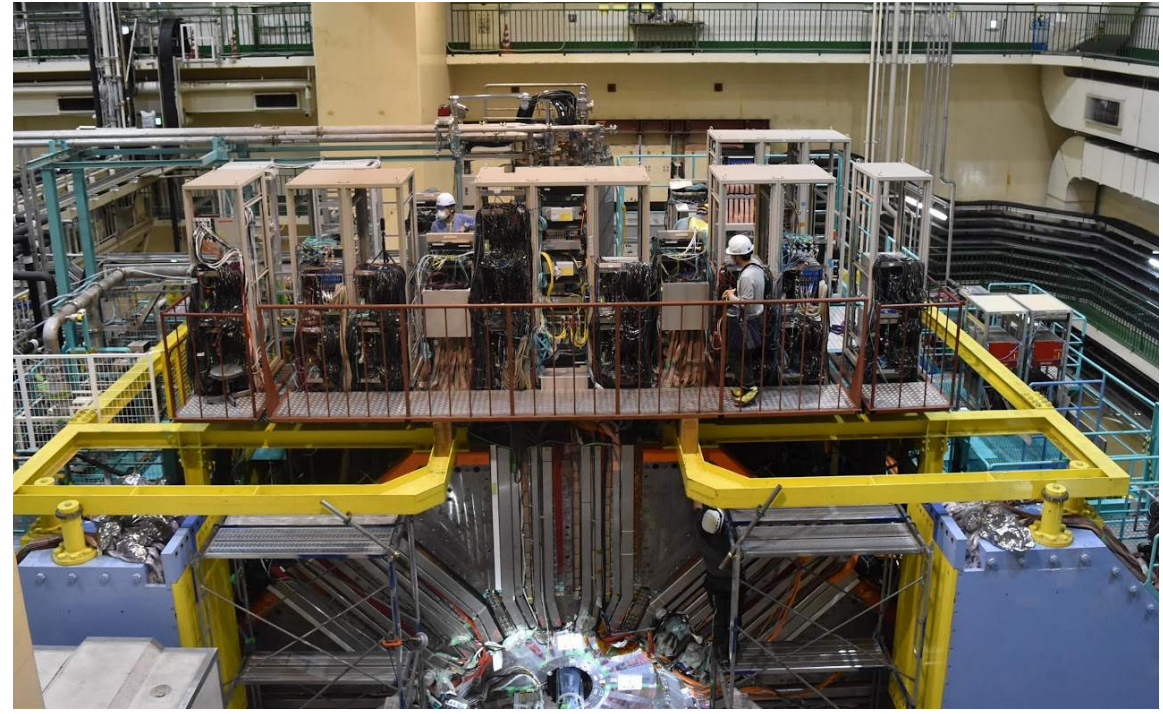
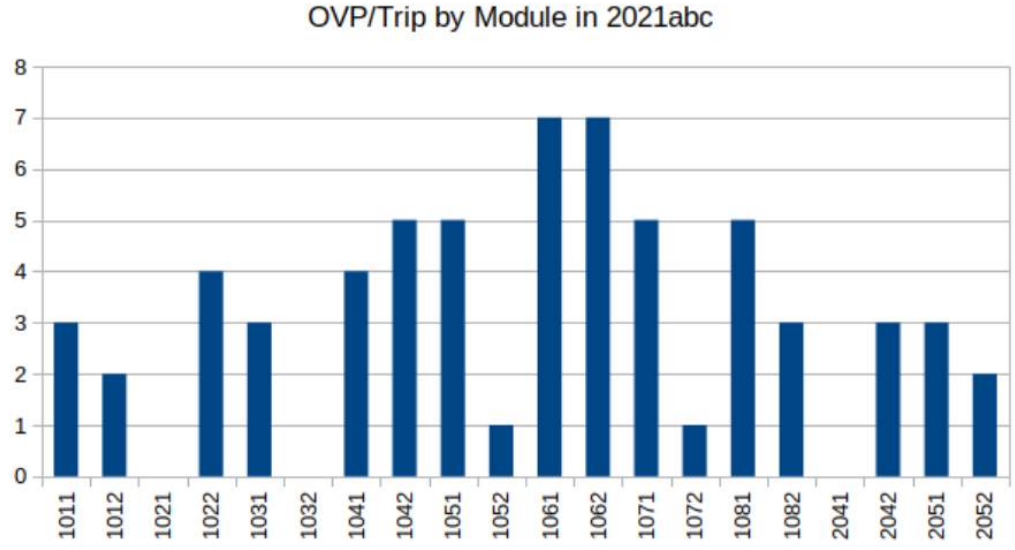
OVER VOLTAGE PROTECTION BOARD

- Part of the PXD-Power Supply (PXD-PS)
- **Protects** the detector and associated electronics (ASICs) against over-voltage/under-voltage conditions
- OVP board protects **24 conditions (23 voltage channels)**
- Approx. 15 m outside of the Belle II experiment (on top of Belle II)



OVP ISSUES AT BELLE II

- OVP events ("***HV Trip***") rate increased in spring 2021 (beam currents were increased)
- Rate approx. 0.5-1 per day
- Talks by Björn Spruck:
  - PXD HV "Trips" Issues By Over-Voltage-Protection (link)
  - Update on PXD HV "Trips" Issues By Over-Voltage-Protection (link)



[B.Spruck]

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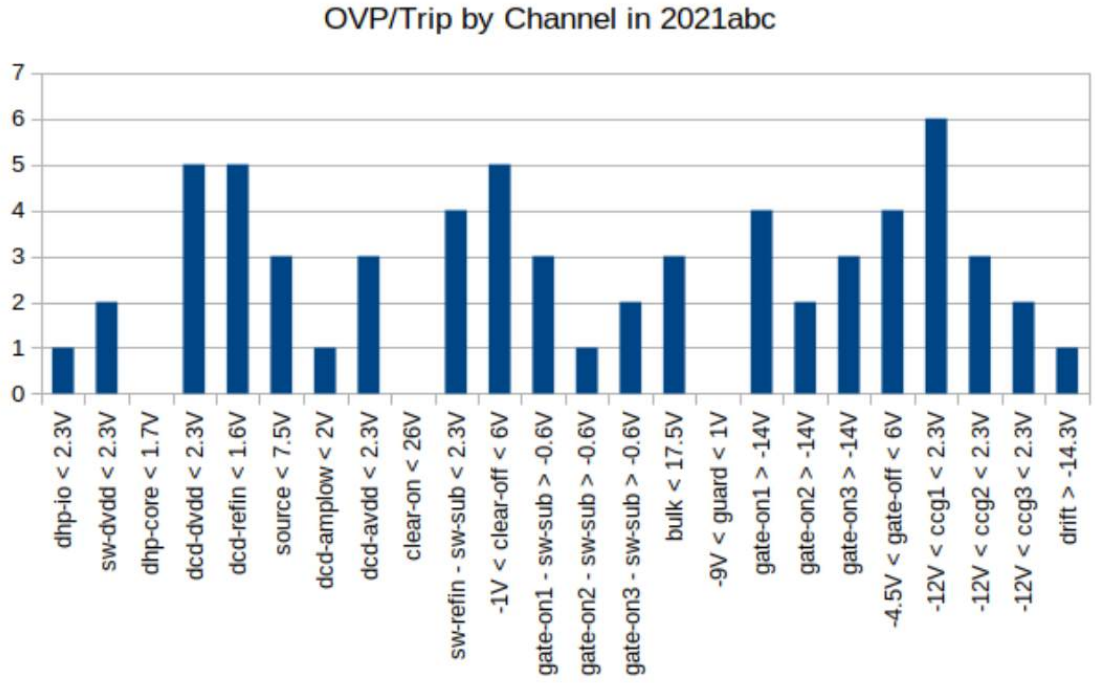

[B.Spruck]

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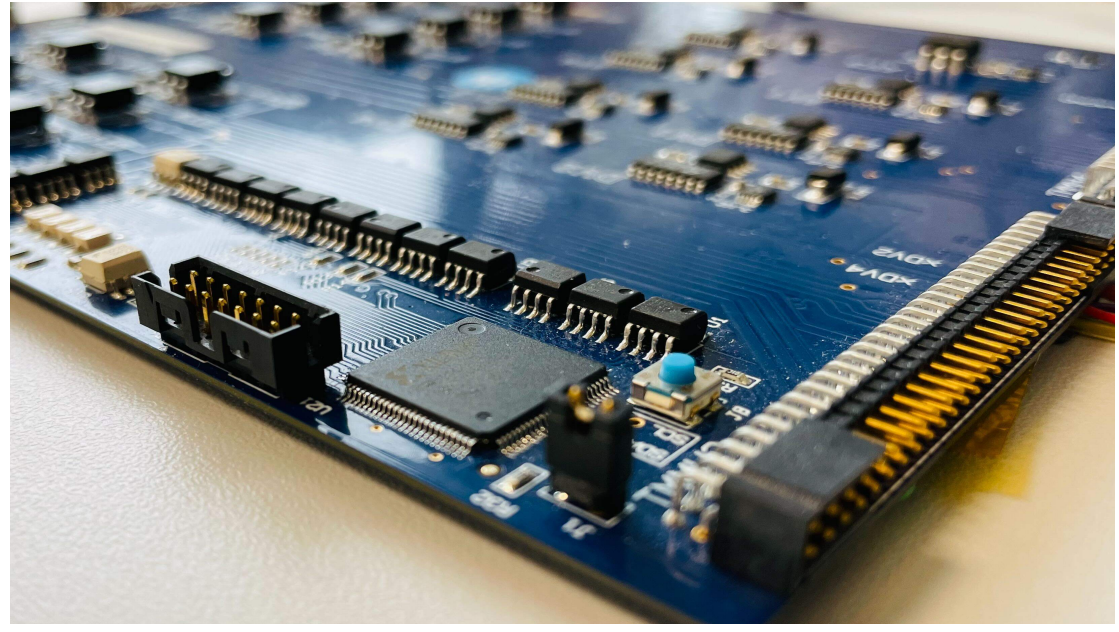
POSSIBLE REASONS FOR OVP EVENTS

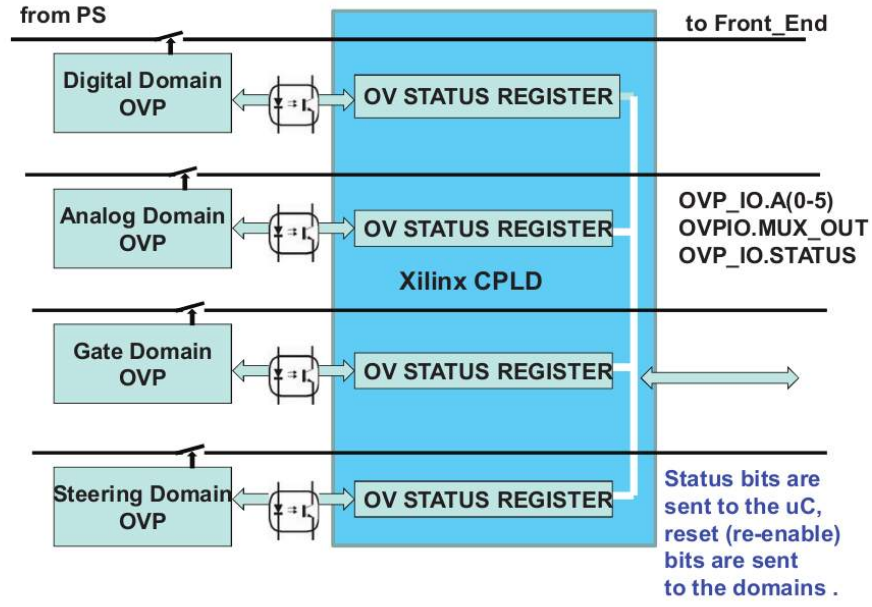
- **Observation**: OVP events occur even when voltage regulators are switched off
- Effect of radiation on the logic can cause triggering of OVP events
- **Single Event Upsets (SEUs)** can trigger an OVP event
- Vulnerable to these events: Control logic implemented in the **Complex Programmable Logic Device (CPLD)**



CPLD on the OVP board

OVER VOLTAGE PROTECTION (OVP)

- Voltages are grouped in 4 domains: **Analog, Digital, Steering** and **Gate**
- Four independent grounds
- Each supply channel is equipped with the protecting circuitry
- Central logic unit (***Xilinx CPLD***) is connected to all protecting circuits (optocouplers)
- Collects status bits from every channel



[P.Kapusta]

CPLD CONTROL LOGIC

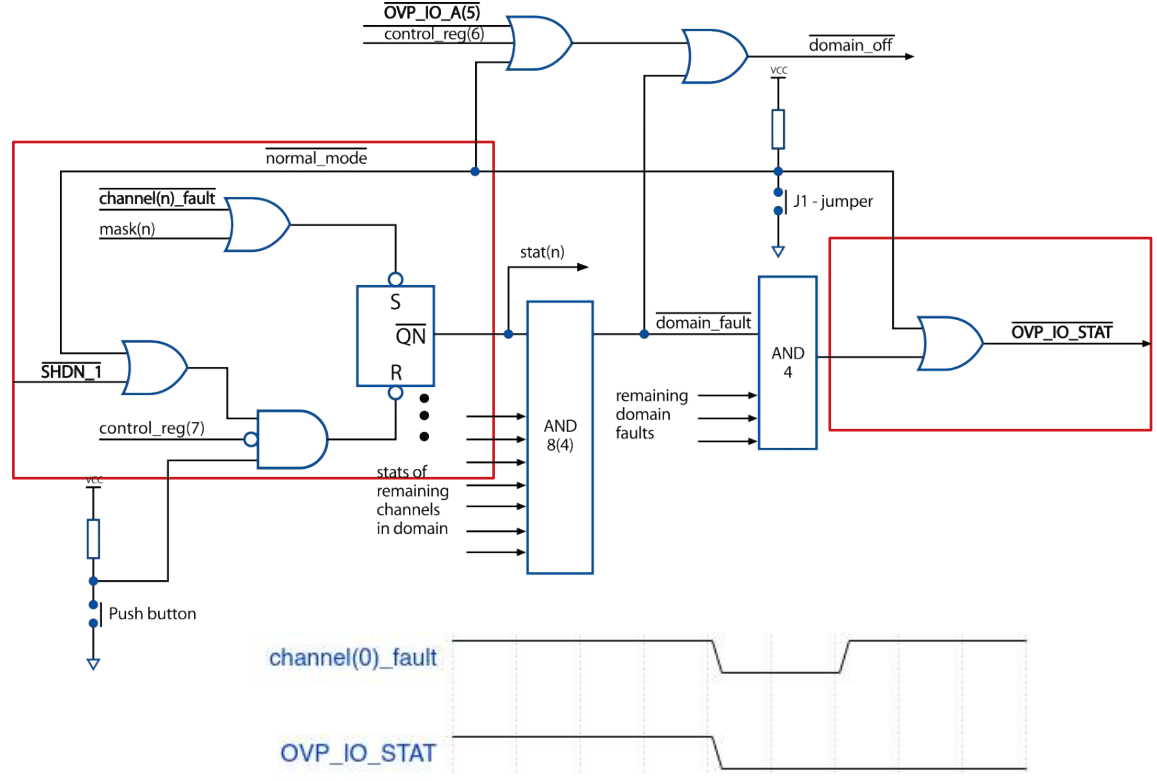
- Control logic in the CPLD:

  1. After detecting an error condition in a channel, ***channel(n)_fault*** is received

  2. The signal is fed into an asynchronous latch (set *S*)

  3. A general fault signal is sent: ***OVP_IO_STAT***

  4. An “emergency off” is issued



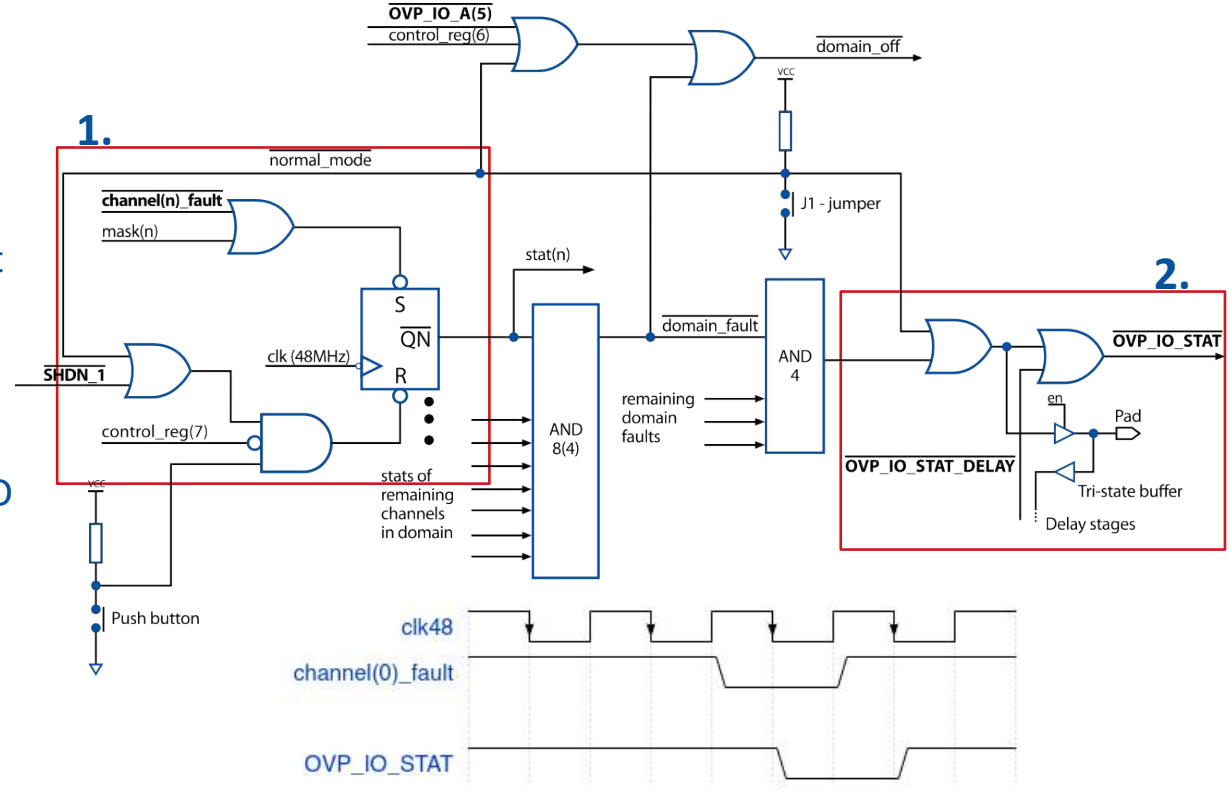
CPLD CONTROL LOGIC

- Countermeasures against SEUs:

  1. Use of a **flip-flop (clocked)** instead of latch: reduces the probability of triggering on a short fault signal / resets state after SEU

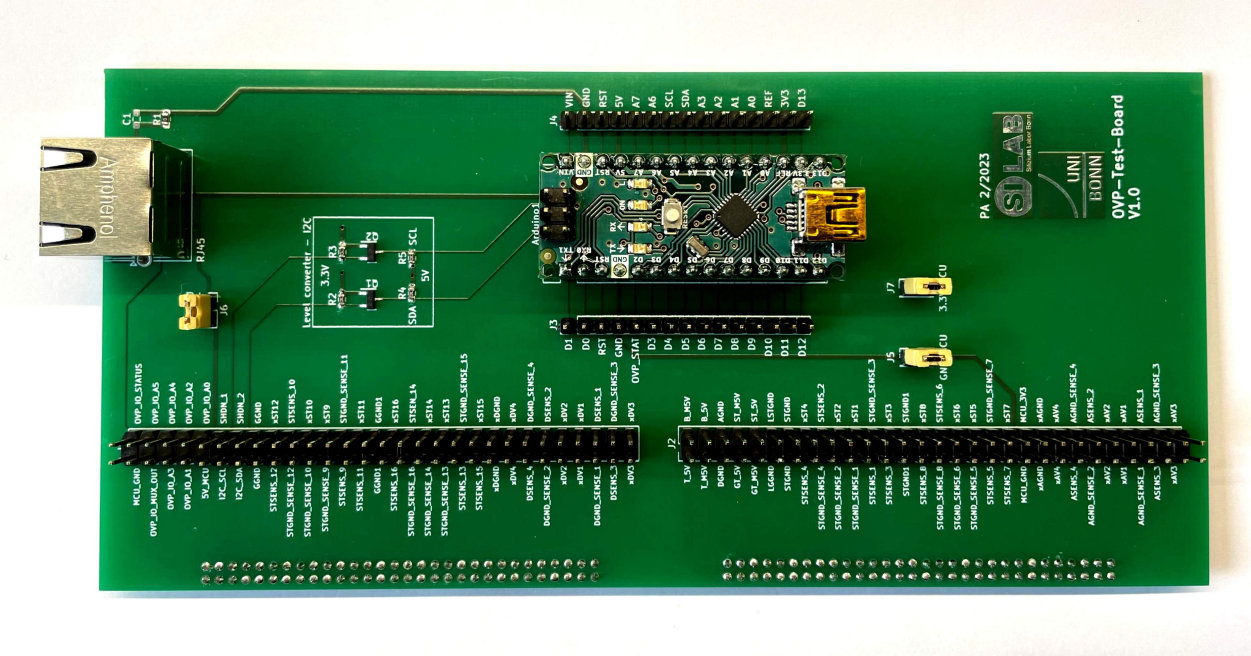
  2. **Pulse length filter** for ***OVP_IO_STAT*** signal to prevent short pulse signals within the CPLD

- Clock frequency is transmitted from second CPLD via an existing line



OVP-TEST-BOARD

- Logic behavior tested in simulations
- **OVP-Test-Board** designed for stand-alone OVP tests
  - Houses an *Arduino Nano*
  - Communicate with auxiliary CPLD (via ***I2C***) -> status of individual channels, write masks or reset the control logic
- Signals on the OVP board can be measured



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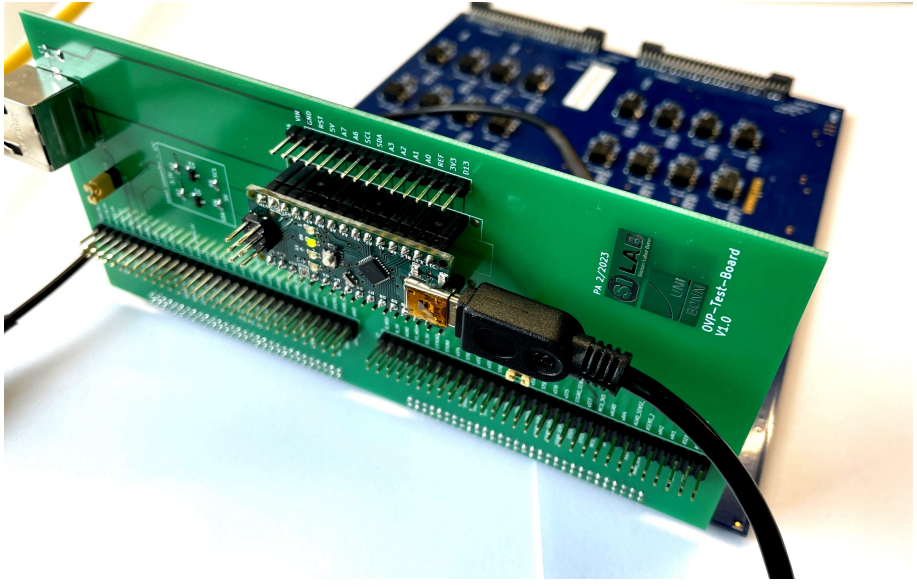
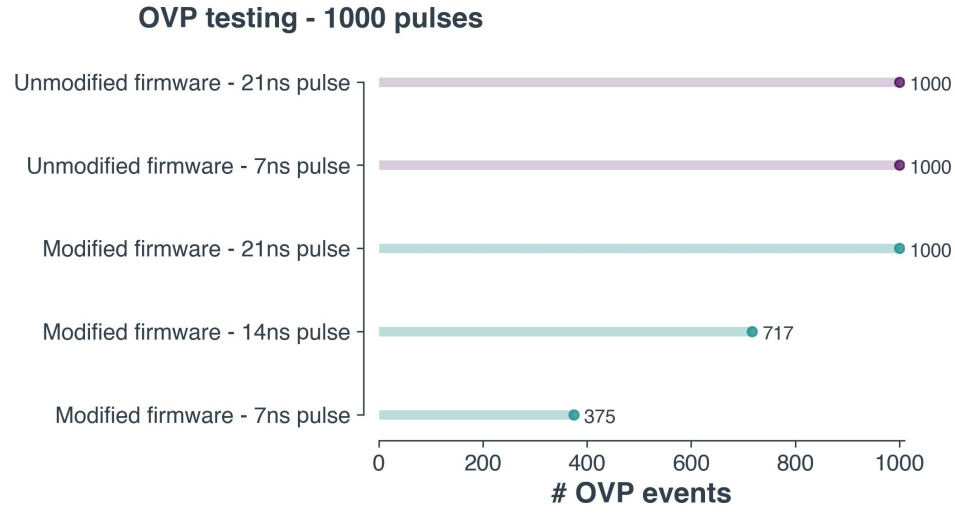
OVP-TEST-BOARD MEASUREMENTS

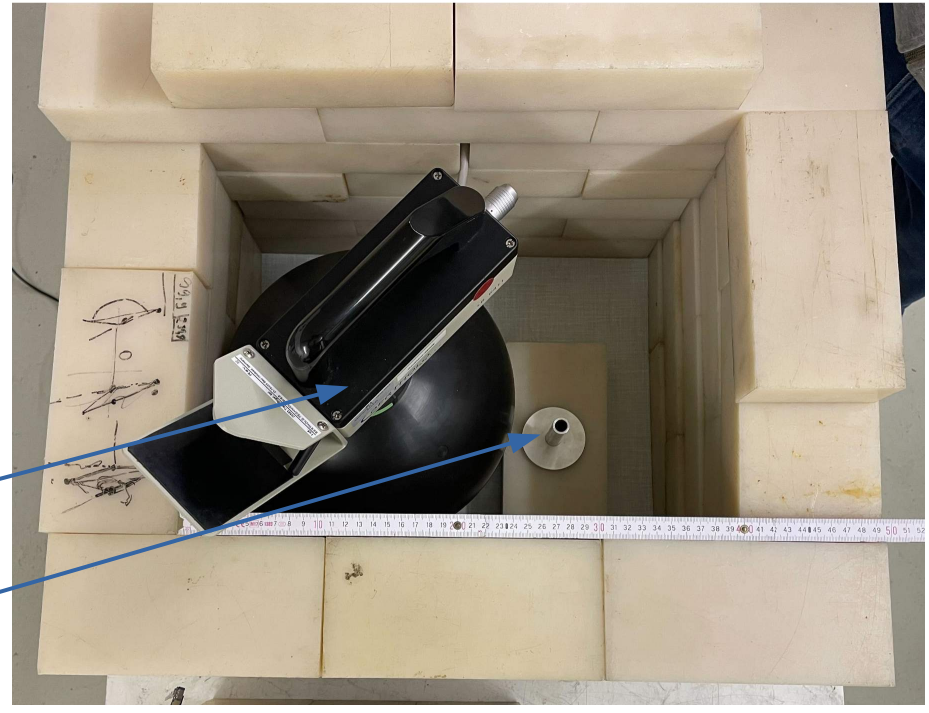
- Injecting short pulses to ***channel_fault***





VERIFICATION – NEUTRON SOURCE

- **Goal:** Verify that changes in logic lead to a reduction in OVP events by SEU
- Neutron source measurement at Helmholtz-Institut für Strahlen- und Kernphysik (HISKP) in Bonn
- Measured 303 muSv/h (distance 17.5cm)
- Duration of the measurement: 18 h



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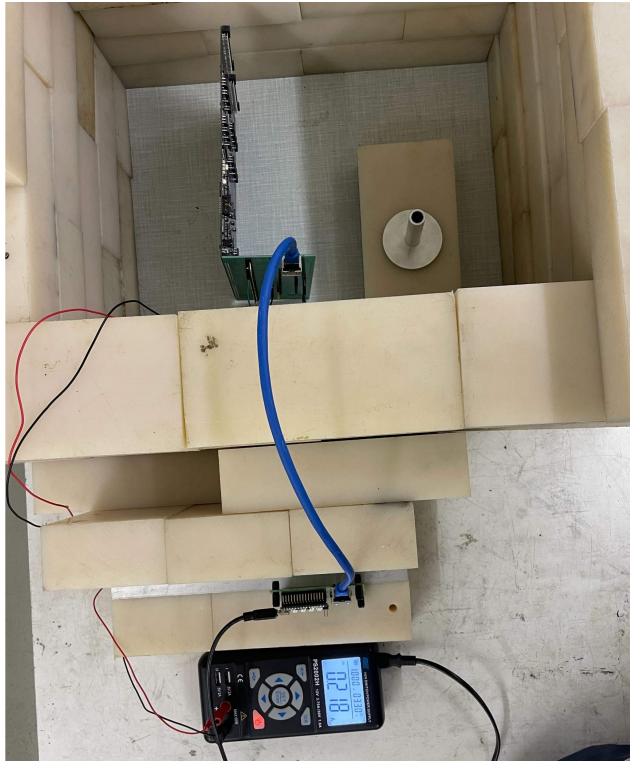

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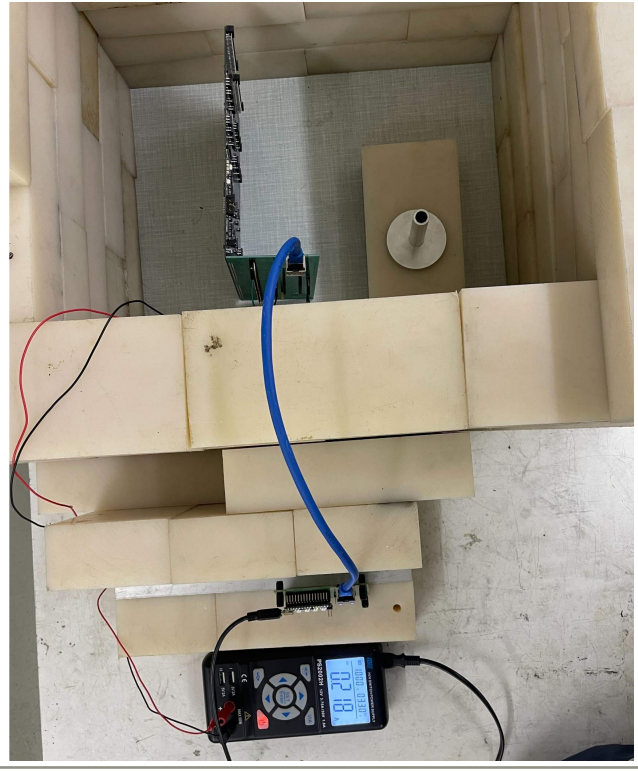

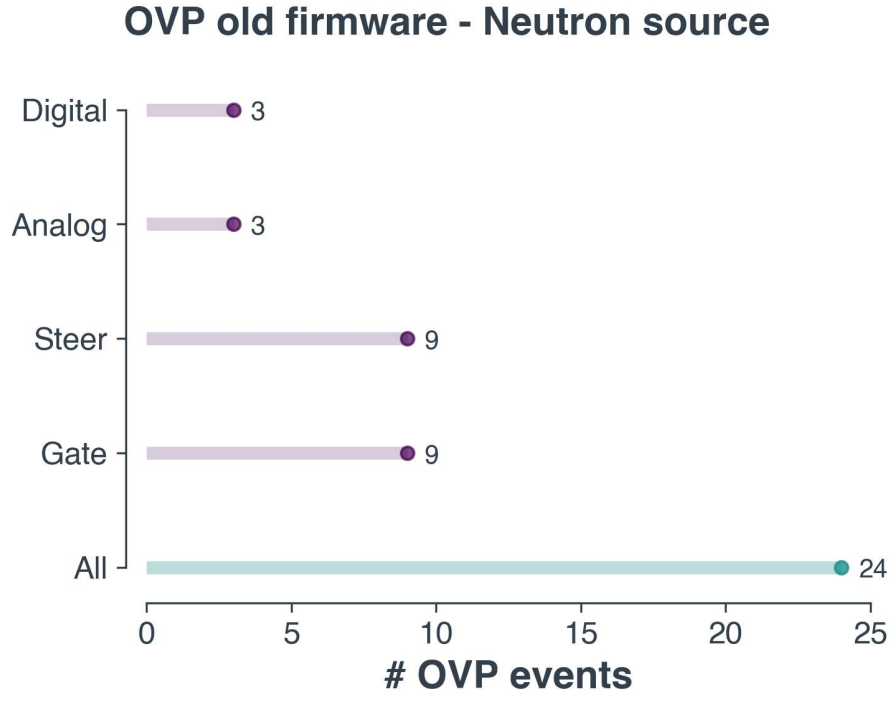

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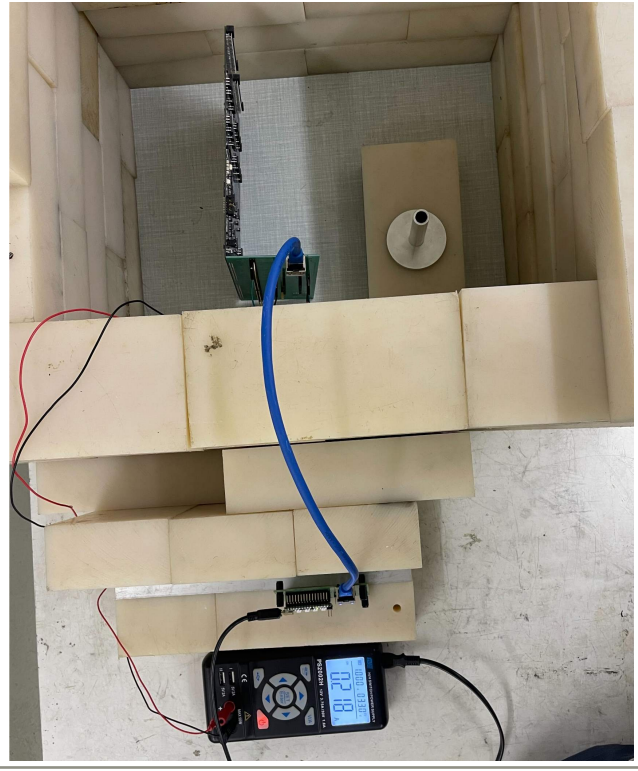
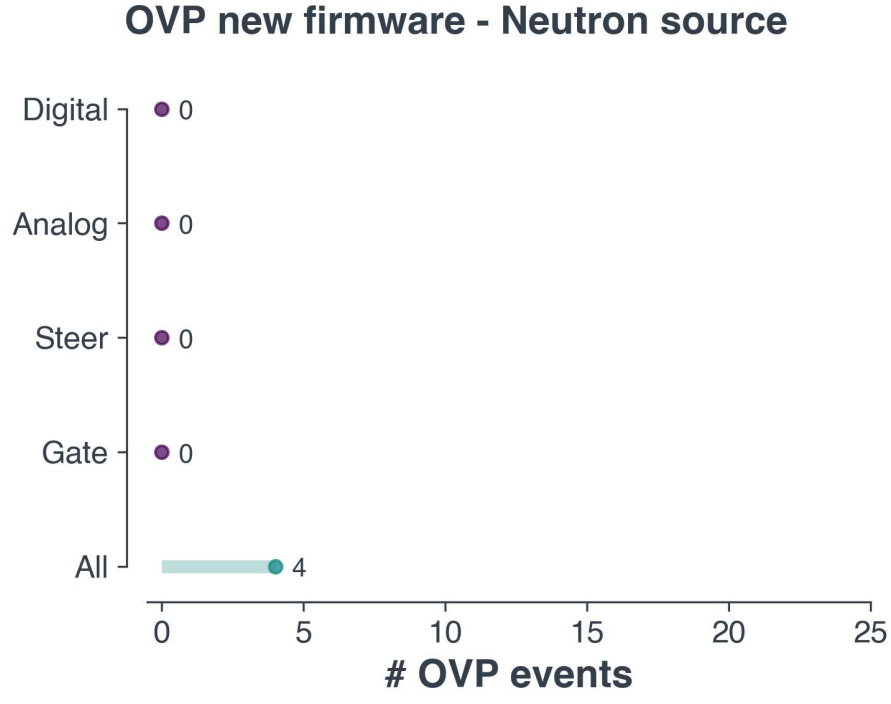
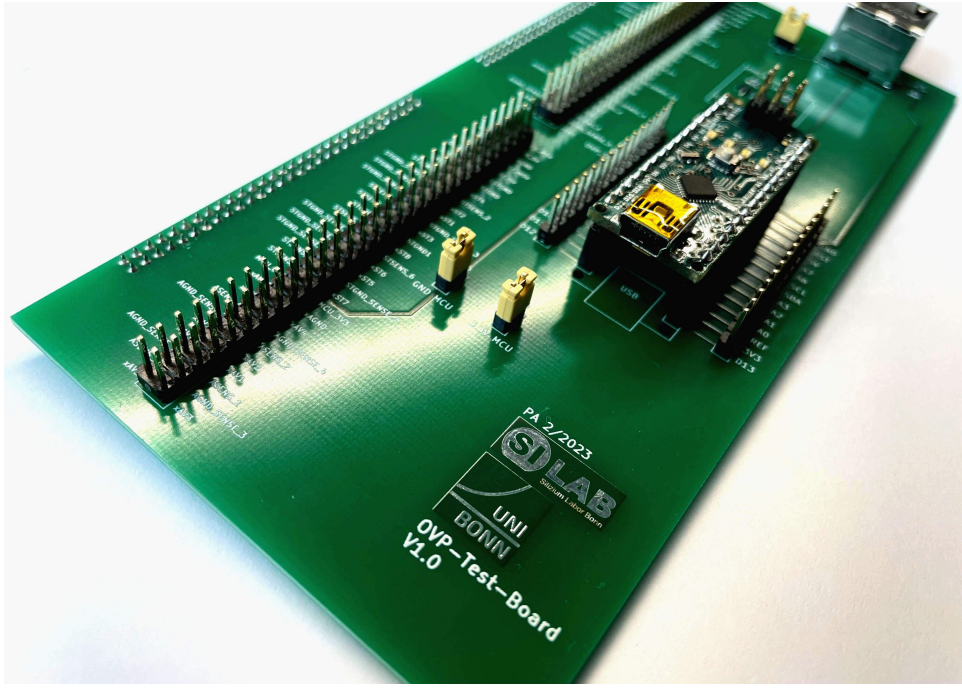




CONCLUSION



- Simulation and measurements show desired reduction of SEU triggered OVP events
- Tests of the OVP board installed in the PXD-PS show the functionality of the new firmware
  - But: Information about which channel triggers is missing
- Possible solution already under test

DOCUMENTATION

- Documentation and files on: https://github.com/SiLab-Bonn/PXD-OVP

Introduction

The LMU-PS OVP board protects the PXD sensor and ASICs from overvoltages and conditions that could potentially damage the PXD detector. In total, 24 conditions are checked. In the presence of an OVP event, the voltages are shut down and the detector is no longer in operation. The rate of triggered OVP events has increased since spring 2021 (0.5-1 per day) after beam currents were increased. Since OVP events occur even when regulators are off, the cause are ***Single Event Upsets (SEUs)*** in the CPLD logic which sends the OVP trigger signal.

The modified firmware is intended to prevent these occurrences.

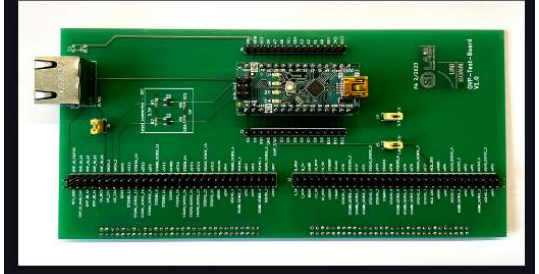
Instructions

ISE Design Suite 14.7 (on Ubuntu) is used to generate the CPLD programming file. The settings for generating the file, the necessary steps for uploading the file as well as the simulation settings are described in the following sections:

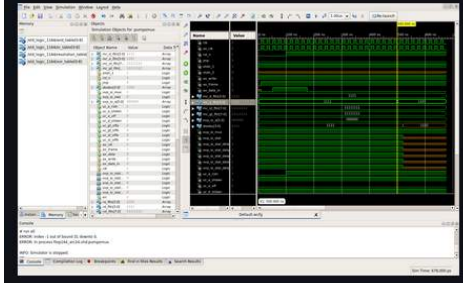
- Generate programming filed
- Upload programming file
- Simulation (behavioral/post-fit)

OVP Test Board

For the investigation, the OVP-Test-Board was designed which houses an Arduino Nano. The Arduino is used to communicate with the CPLD (via **I2C**), read out the status of the individual channels, write masks or reset the control logic.

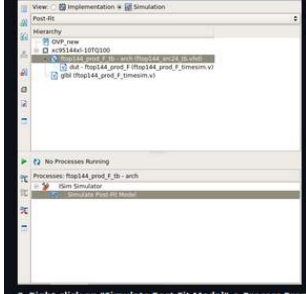


3. Run "Simulate Behavioral Model" and ISim Gui should open



Post-Fit Simulation

1. Select Simulation and "Post-Fit" in the drop-down menu



2. Right-click on "Simulate Post-Fit Model" -> Process Properties

Important: The "Waveform Database Filename" has to be set (`ftop144_prod_F_tb_isim_fit.wdb`)

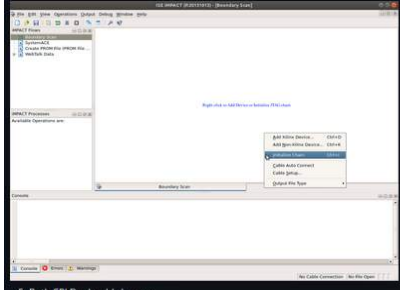
Upload firmware

The CPLDs on the OVP-board can be configured by using ***ISE iMPACT*** and a JTAG adapter.

1. To install the ***Xilinx Platform Cable USB-JTAG drivers*** follow the instructions in section 3.3.
2. Export file `libusb-driver.so`

```
export LD_PRELOAD=/path/to/your/file/usb-driver/libusb-driver.so
```

3. Start ***iMPACT***
4. Double-click on "Boundary Scan" and then right click and "Initialize Chain"



5. Both CPLDs should show up