Monolytic **A**rray of **R**each **Th**rough **A**PDs (MARTHA)

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Outline

- Concept

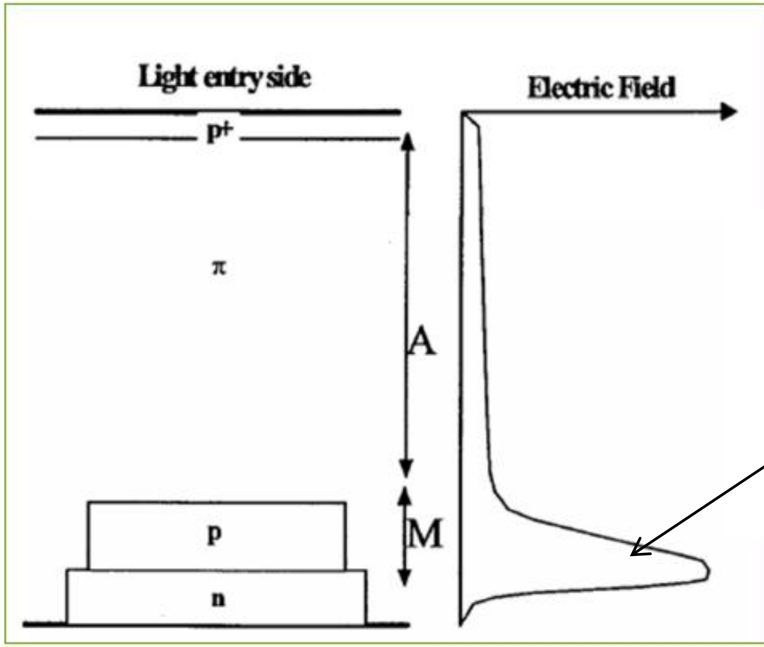
  operation in proportional mode

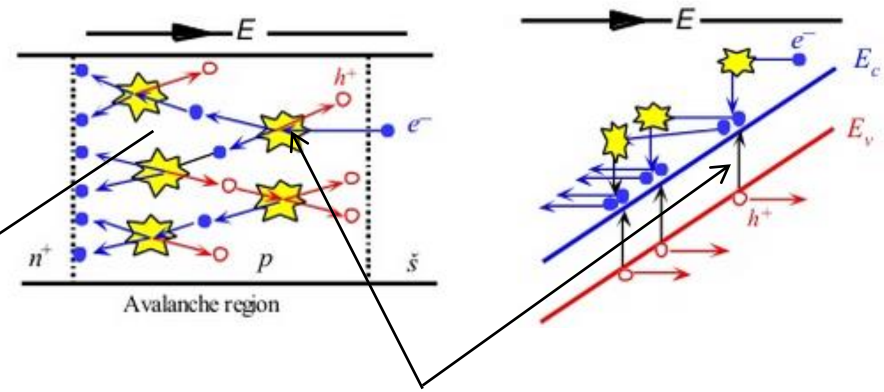
  no inter pixel dead space

  suitable for large pixel arrays

- Status

Reach Through APD (schematic view)

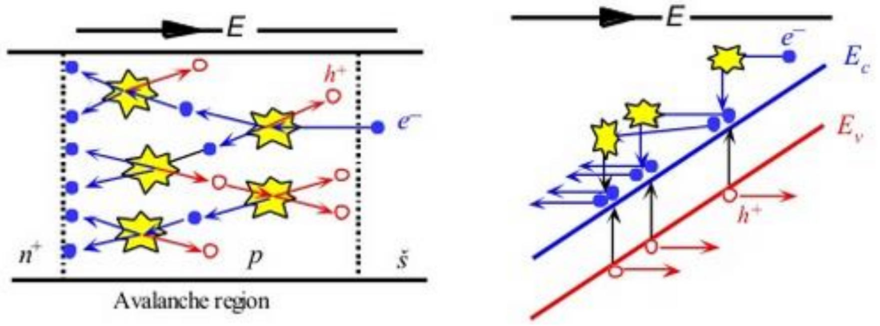




(signal) electron gets mutliplied by impact ionization

An e/h generation can be initiated by a high energetic electron or hole
in **Silicon** electron initiation is more likely and starts at lower electric fields

Two general operation modes (not only for RT APD):



A) at moderate E-Field electrons and a f**ew** holes cause multiplication $e_{mult} \approx M\ e_{sig}$
-> we can conclude from e_{mult} back to e_{sig} -> **APD in proportional mode**
B) at high E-Field electrons and **many** holes cause multiplication -> chain reaction M $\rightarrow \infty$
-> huge output signal but **cannot** conclude from e_{mult} back to e_{sig} **APD in Geiger mode** (Simpl)

APD vs SiPM

no dark rate trigger
no optical cross talk
no after pulsing
no dead space (100% fill factor)

Applications of single RT APDs (proportional)

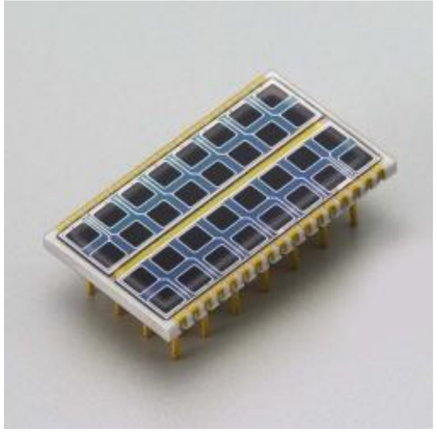
From Excelitas web page:

Laser range finder
Scanning video imager
Confocal microscope
Spectrophotometers
Flourescence detection
Luminometer
DNA sequencer
Particle sizing

probably many would benefit from 1d or 2d position resolution

What about APD arrays ?

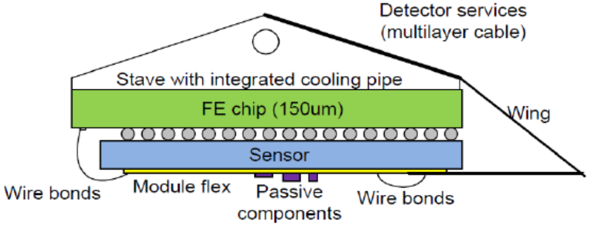
Hamamatsu APD array S8550-02,
4x8 pixel, sensitive area 1.6mm²

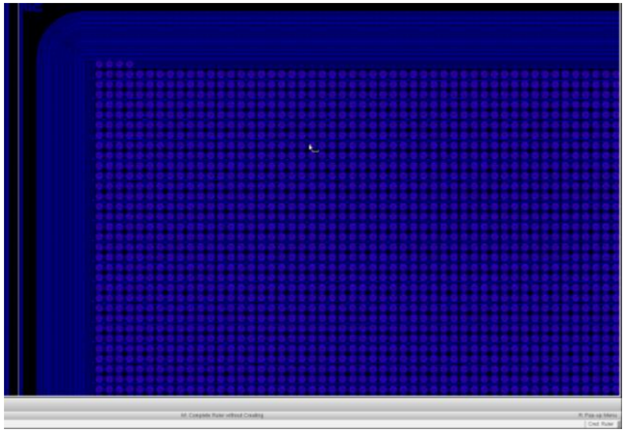


Laser Components
8 or 16 elements (40μm gap only)

Similar products from **First Sensor**, **Excelitas** **max. elements 64, min. dead space 40μm**

ATLAS **pin diode array**
500k pixel a 50μm

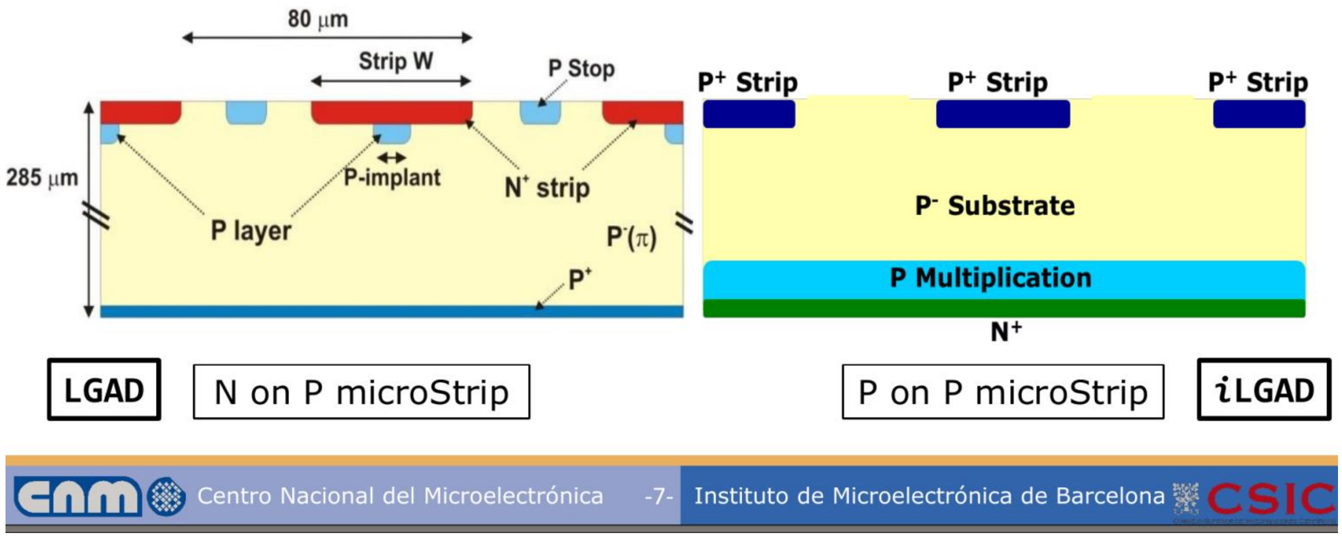




LGAD – for Tracking (FBK, CNM et others)

strip detector approach

2 basic concepts

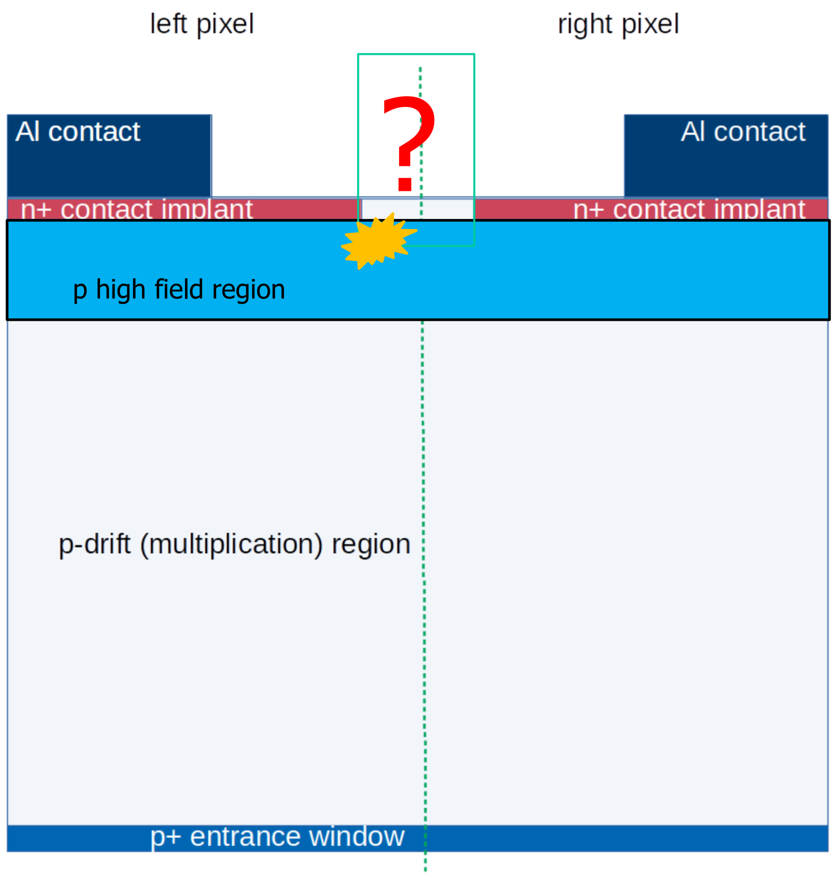


basically a RT device
poor fill factor

hom. amplification but only for charge deposited in the center of the wafer
suitable for MIPS but **not for soft xrays**

There is a new approach – presented at the end of the talk

Interpixel isolation



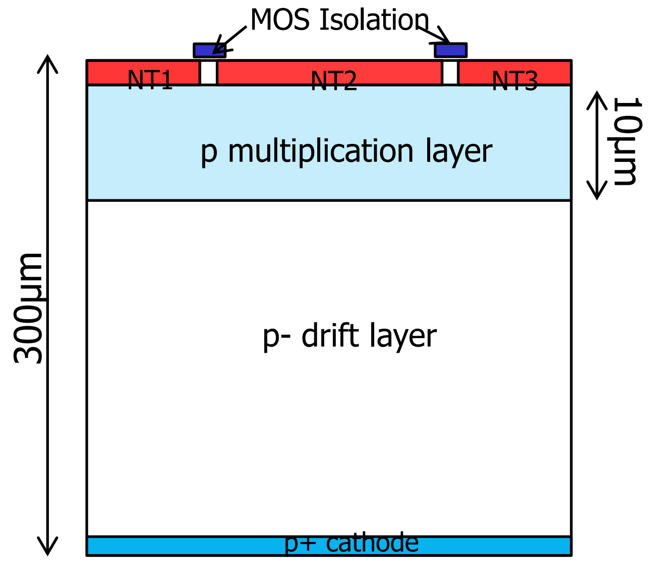
Requirements

- Isolation (drastic reduction of electron density)
- Edge break down suppression (inhomogeous response)

Very nice to have

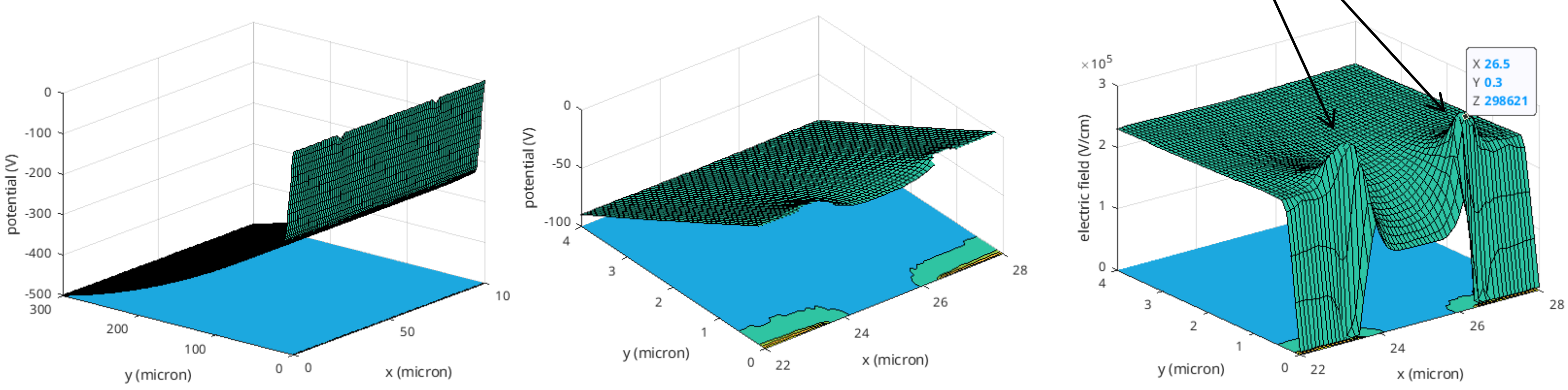
- 100% fill factor
- (no gain loss -> homogeneous gain)

Strip array 50µm pitch (2D simulation) without edge breakdown suppression



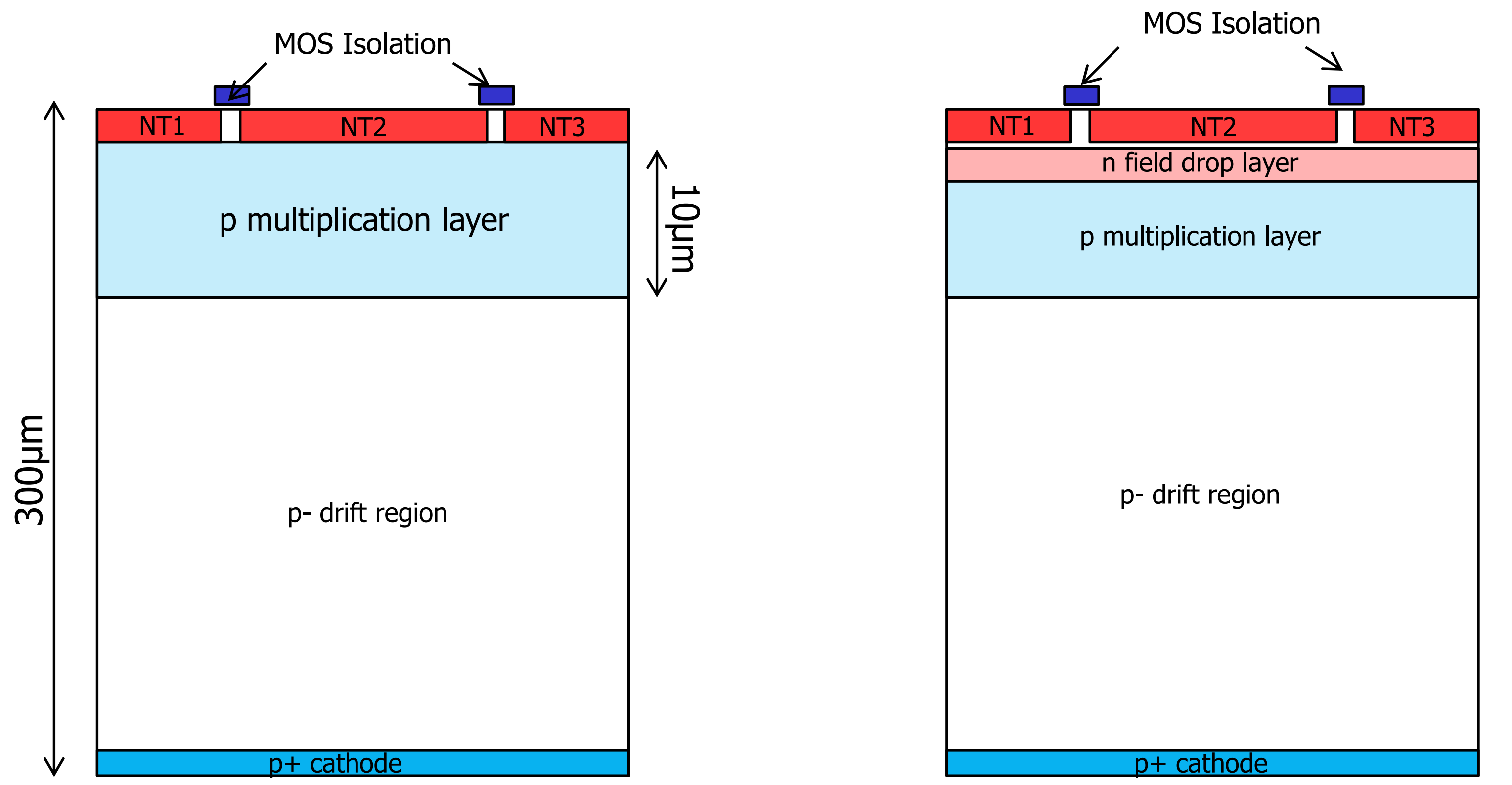
Avalanche (beakdown) occurs at first at pixel edges

HF region extends over pixel gaps



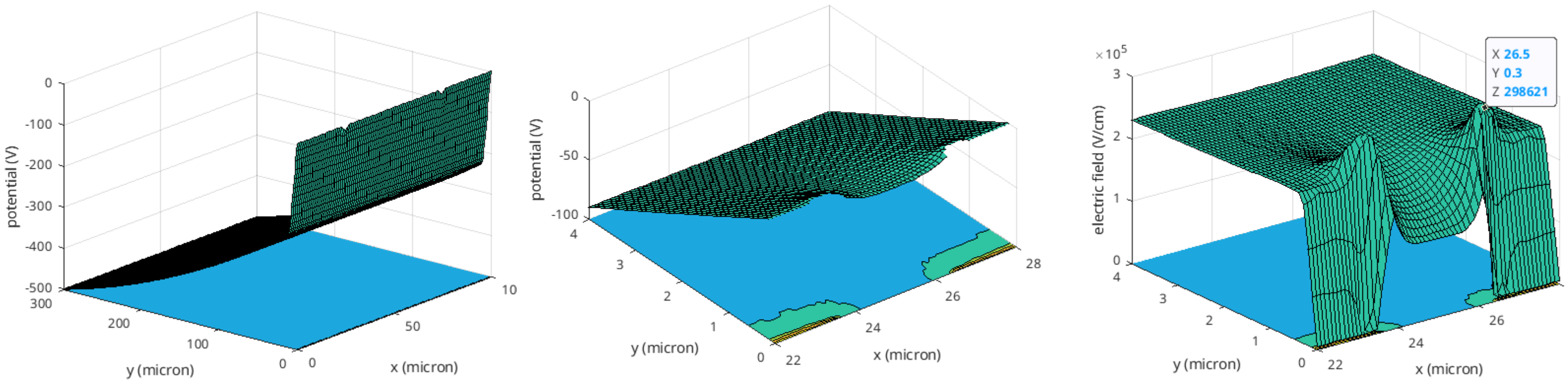
approach not usable ☹

APD array without and with edge breakdown precaution

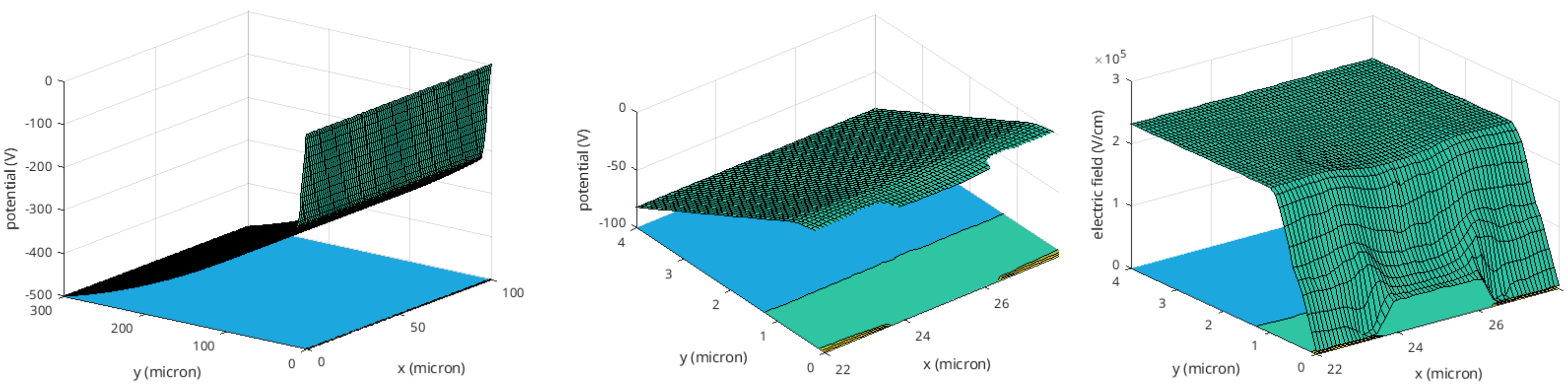


2D simulation – Strip array 50µm pitch, 3µm gap

HF region extends over pixel gaps



HF region and field drop layer extend over pixel gaps



V_{MOS}=3V

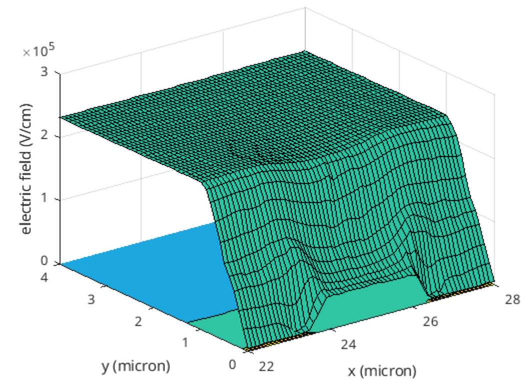
Why does it work?

From Poisson eq. $\frac{d^2u}{dx^2} = \frac{dE}{dx} = \frac{1}{\varepsilon}(qN(x) + n + p)$

$$E(x) = \frac{q}{\varepsilon}\int_{x1}^{x2} N(x)\ dx$$

$$D(x) = \int_{x1}^{x2} N(x)\ dx$$

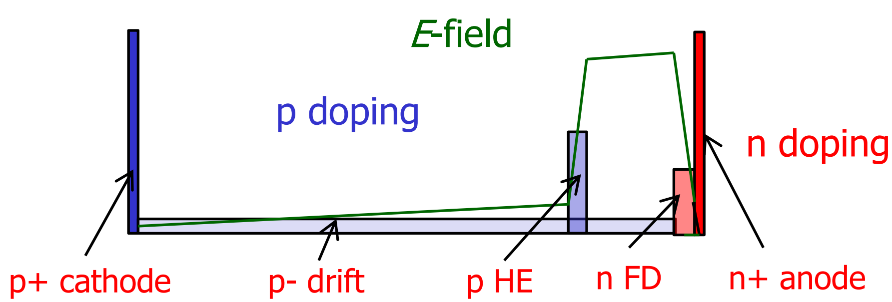
u – potential, n,p electron, hole density
E – electric field
N – depleted! doping concentration (cm^{-3})
ε – permittivity of silicon
q –electronic charge
D - (implanted) dose (cm^{-2})



⟶ Equivalence of electric field and depleted dose !

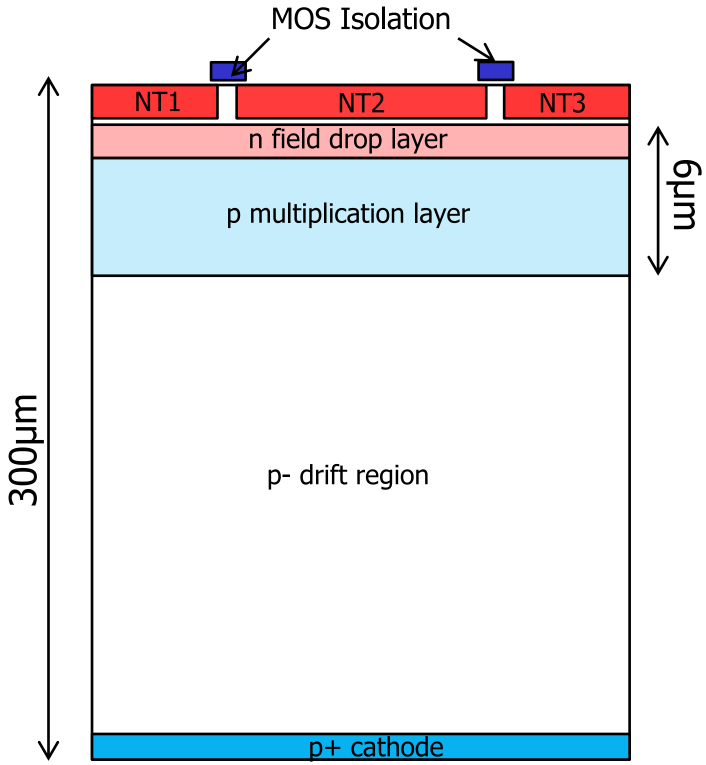
$\varepsilon E_{max} = q \sum D_p = q \sum D_n$ (depleted doses)

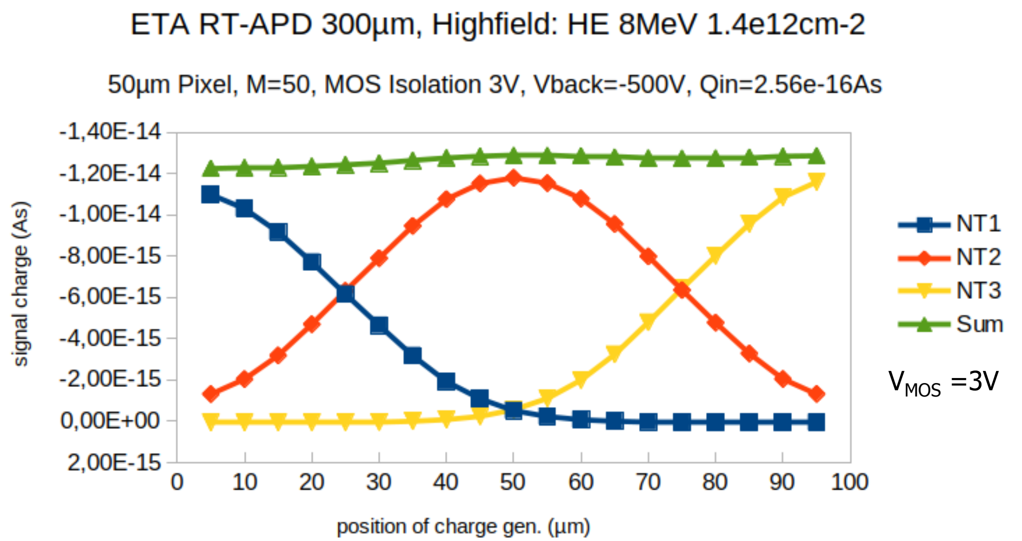
$$D_{FD} \approx \frac{2}{3} D_{HE}$$



-> 2/3 field drop
FD gets depleted by HF
(no pixel shortage)

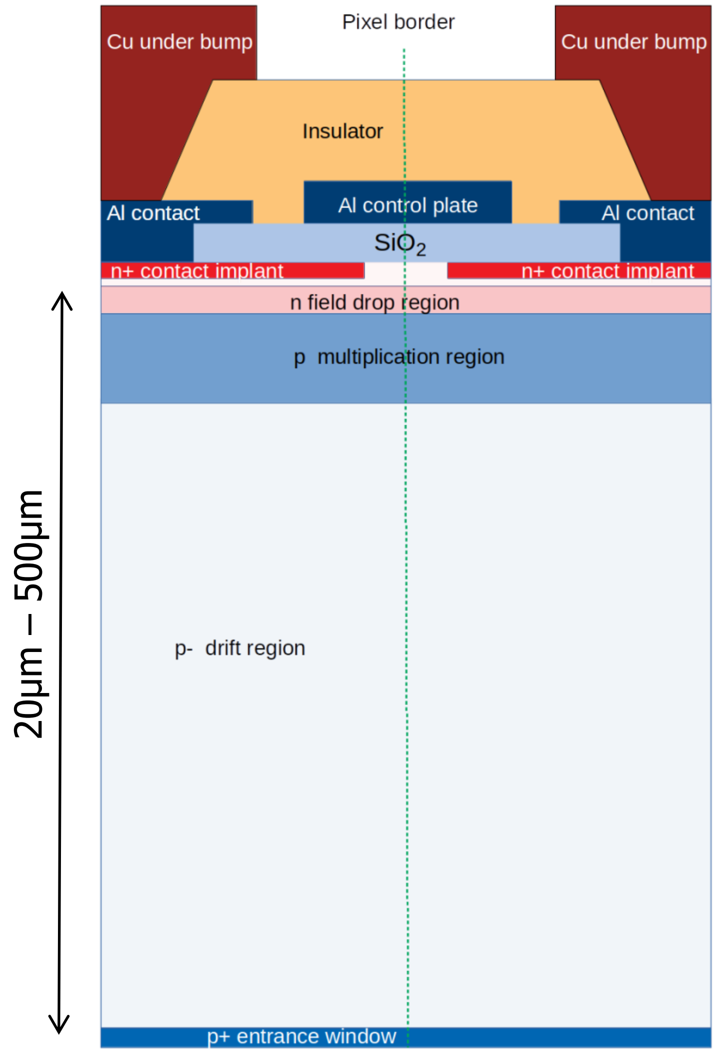
Reach-through APD with 50µm pixel and MOS Isolation (position scanning (ToSCA))





Gain ≈ 50

Our goal: final array



Expected features

Gain up to 20

Collection efficiencies: > 99%

Pixel pitch: given by bumpbond technology and ro electronics space consumption (ATLAS 50µm)

Position resolution: $<< \frac{pitch}{\sqrt{12}}$

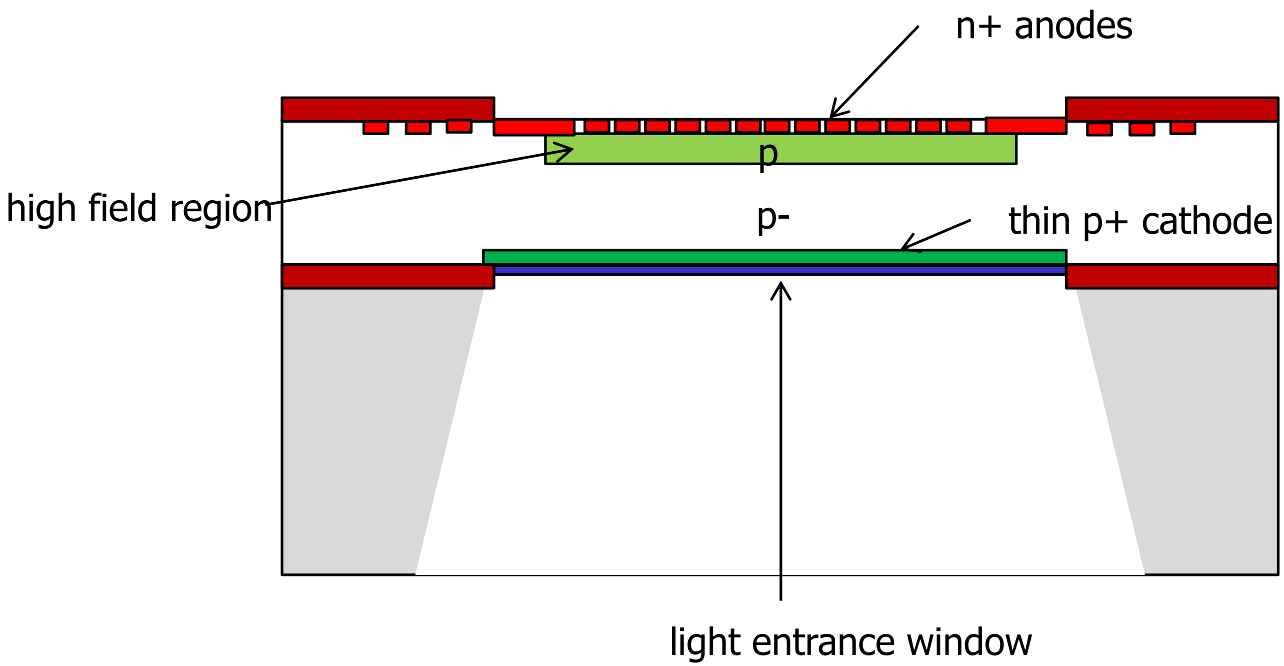
Time resolution:

Application dependend

Leading edge trigger: <50ps

Full signal formation 50ns (500µm)

Thinned Reach Through APD based on HLL SOI Technology



$t_{APD} \gtrsim 20\mu m$

t_handle_wafer ≈ 400μm

$t_{APD} = 20\mu m$: drift times (triggering electrons + amplified holes) ≈ 0.5ns

Why don‘t we use just avalanche detectors? Signal to Noise of an APD

$$\frac{S^2}{N^2} = \frac{I^2 * M^2}{B(2q(I + Idv) * M^2 * F + 2qIds + \frac{4kBT}{R_L})}$$

APD noise

ro noise

APD user‘s guide (Hamamatsu)

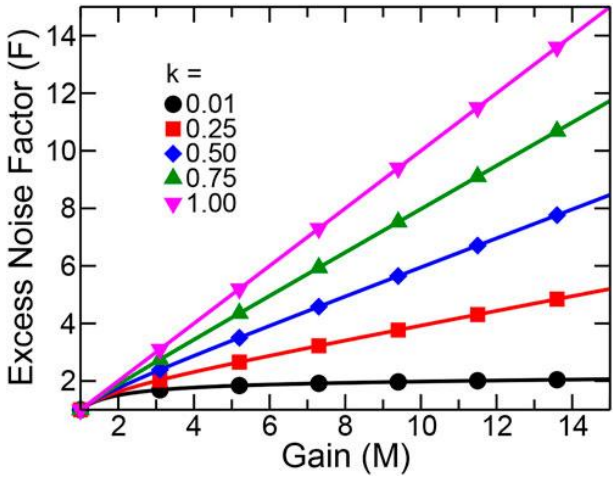
I – non amplified photocurrent
M – amplification
I_{dv} – dark current of silicon volume (amplified)
I_{ds} – surface generated dark current (not amplified)
F – excess noise factor
B – bandwidth
R_L – load resistance
q – electron charge
k_B – Boltzmann constant
T - temperature

Stochastic nature of the multiplication process:

Excess noise factor

$$F = M * k + (2 - \frac{1}{M})(1 - k)$$

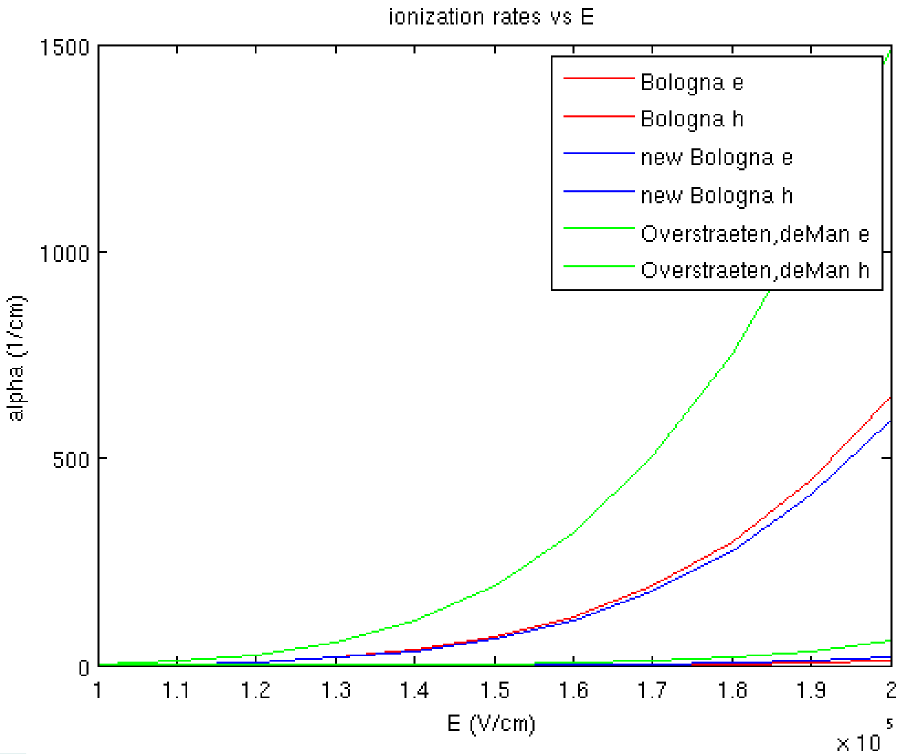
$$k = \frac{\alpha_h}{\alpha_e}$$ ratio of ionization rates



A. Pilotto et. al. (2022)

Ionization rates $\alpha(E)$ (material constant)

Number of generated electron-hole pairs per drift length of an electron or hole along the electric field, resp.

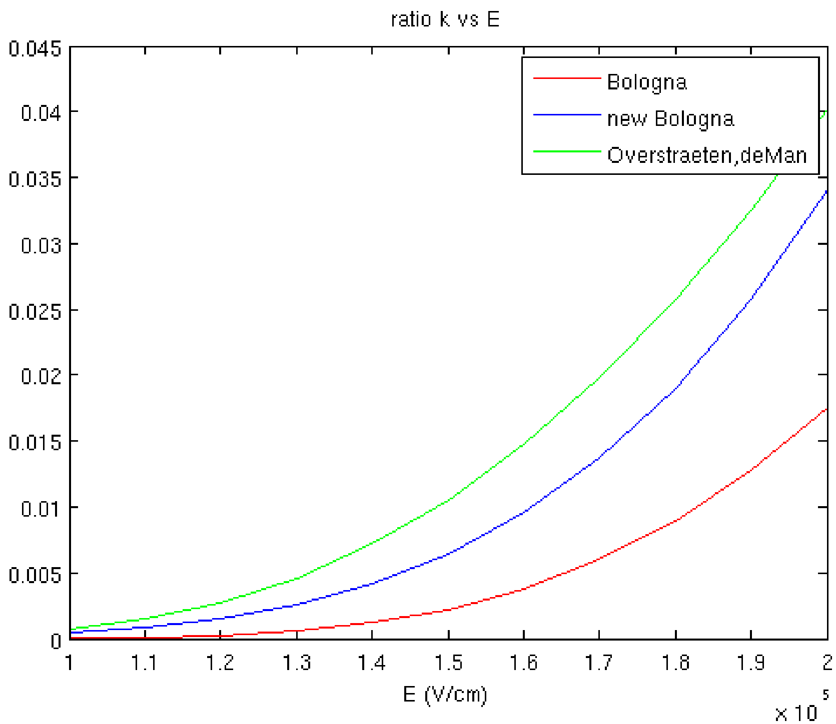


$1/\alpha$ - doubling length

Silicon best material for prop. APDs

$$k = \frac{\alpha_h}{\alpha_e} < 1$$

The lower E the lower k
the lower the noise but the lower gain!



A bit math

Calculation of gain M - electron amplification only
$\alpha(E)$ - ionization coefficent for electrons (1/cm)

$$M = (1 + \underbrace{\alpha * x_i}_{\text{gain per stepsize } x_i})^N$$

Same Ansatz as compound computation of interest Zinseszins-Rechnung

$$N = \frac{t_{hF}}{x_i}$$

t_{hF} thickness of high field region

to get rid of x_i

$$M = \lim_{x_i \to 0} (1 + \alpha * x_i)^{t_{hf}/xi}$$

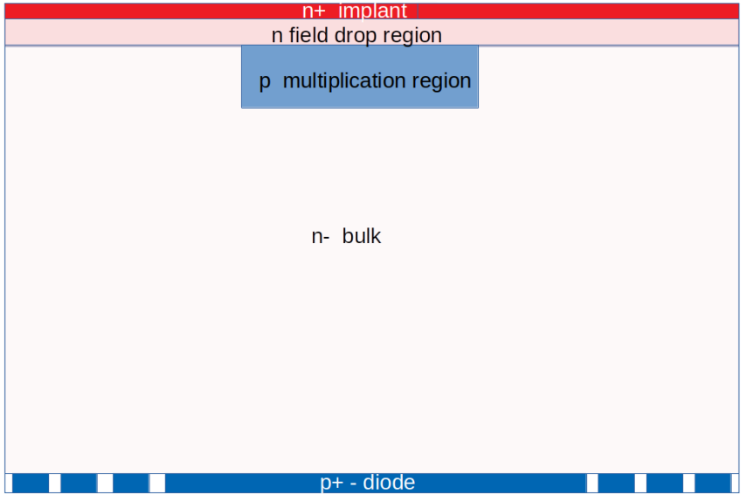
$$\boxed{M = e^{\alpha t_{hF}} \qquad (E = \text{const.} \rightarrow \alpha = \text{const.})}$$

Thanks to Wolfram Alpha

Let‘s go for a wide high field region to obtain lower noise !

DIO12 HE implantation test (P – pxd13, **B – pad_ava**)

Simple diode production with high field implantation on the back side



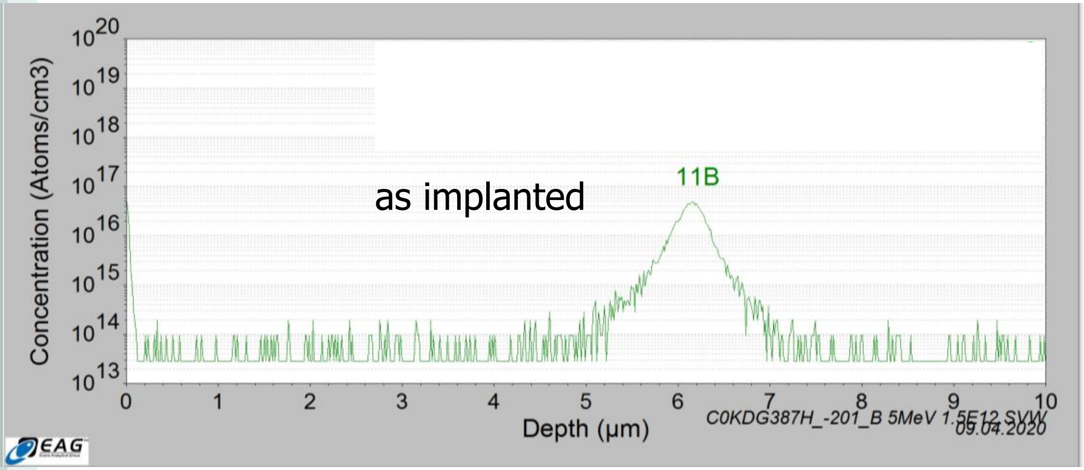
multi guard

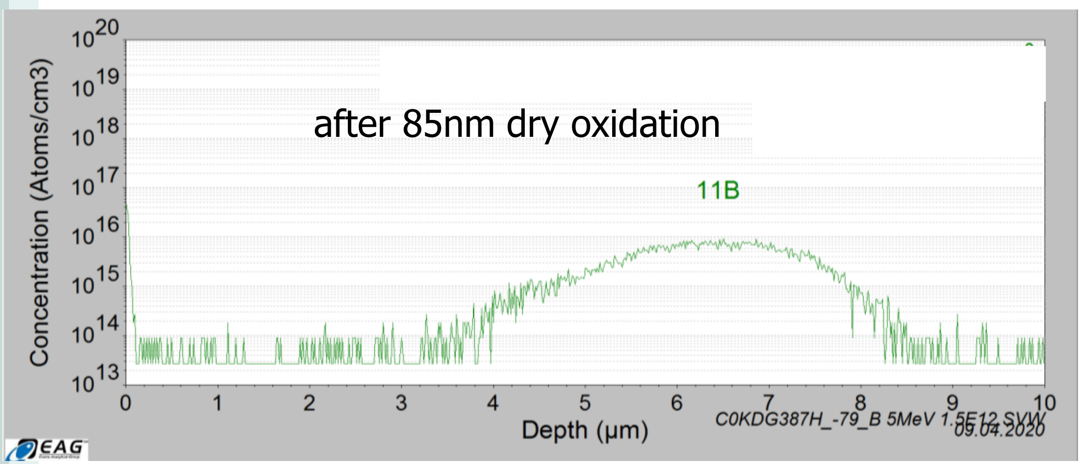
- particle contamination (external facility HZDR)
- masking of the HE implantation
- annealing, leakage current
- Vbd ?
- Gain ?

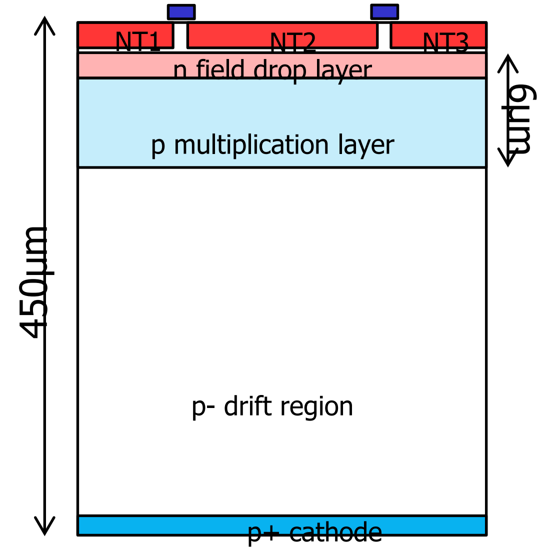
still on n- bulk instead of p-bulk !

Gain defined by dose and depth (energy). Energy fixed to 5MeV can be shielded by thick 9µm photo resist

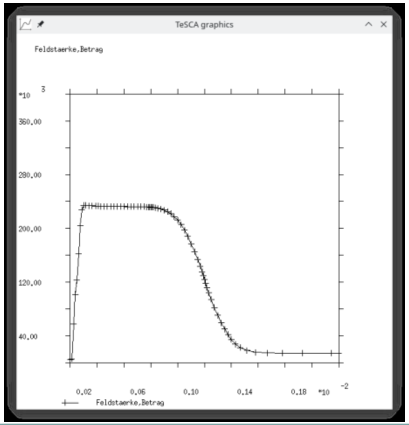
High field implant





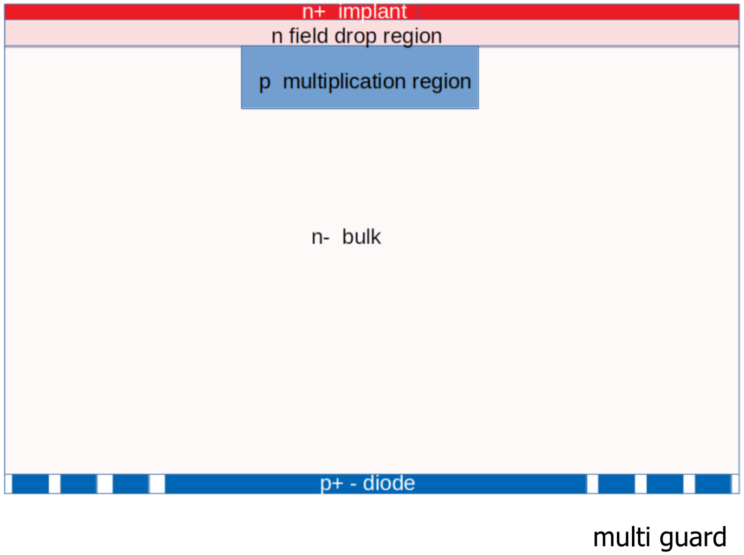


Relative flat 'plate capacitor like' field distribution
-> lower field -> low k -> lower excess noise



DIO12 HE implantation test

Simple diode production with high field implantation on the back side

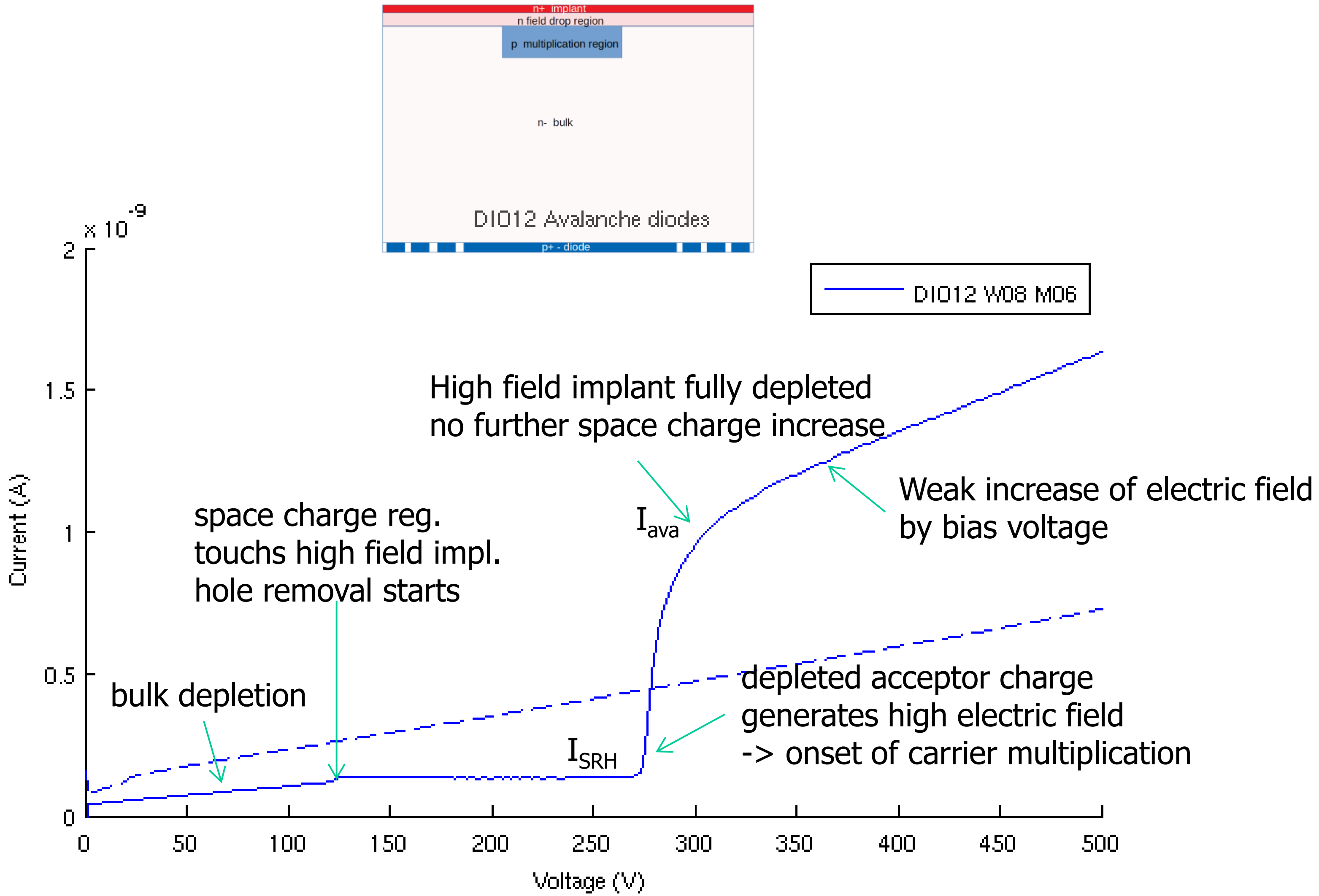


- particle contamination
- masking of the HE implantation
- annealing, leakage current
- can be shielded by thick photo resist?

- Electrical test ?
- Vbd ?
- Gain ?

still on n- bulk instead of p-bulk !

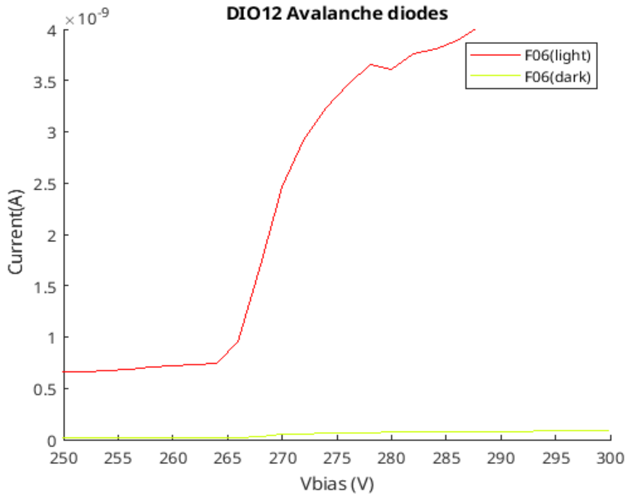
DIO12 avalanche diode IV curve

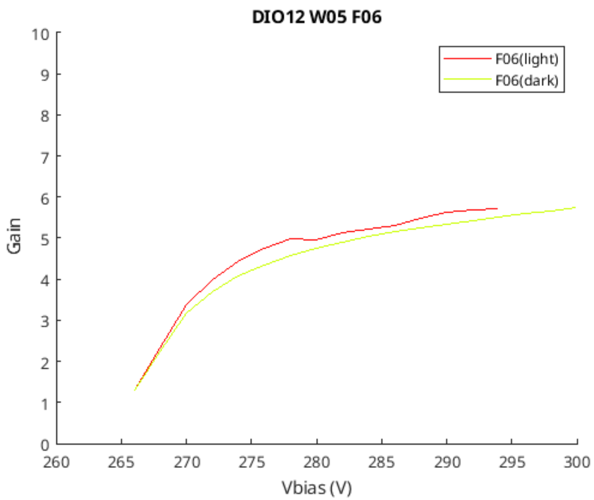


Gain estimate: $I_{ava} / I_{SRH} \approx 10$

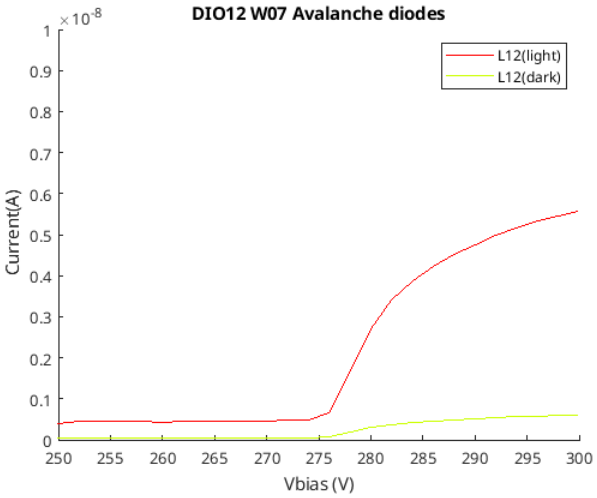
‚Signal' amplification ;-) – little bit light trough the door of the dark box

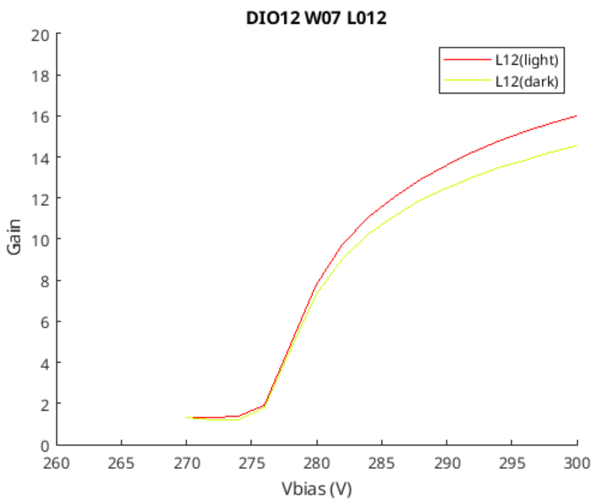
W05 med. dose





W07 higher dose

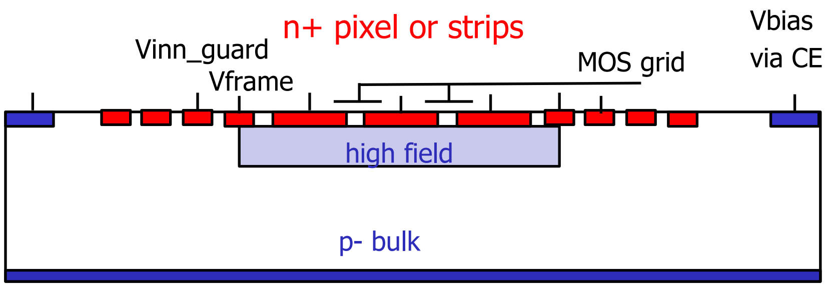




First prototyping on thick (standard) wafers

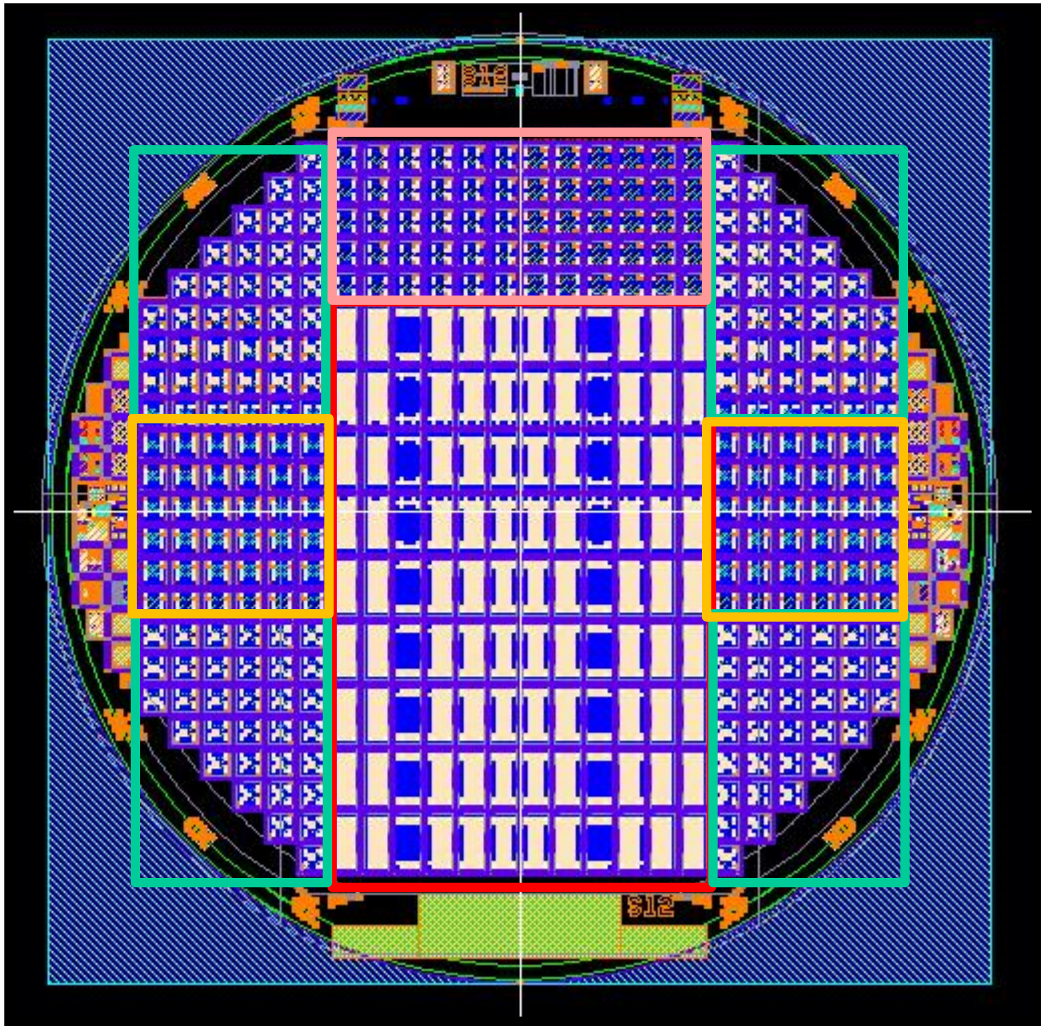
Aims

- proof of principle
- Efficiency, gain, cross talk and noise studies (vs T)
- find a reliable narrow guard ring structure
  (in view of high voltage operation, buttable arrays)



backside p+ entrace window
non structured, no Al

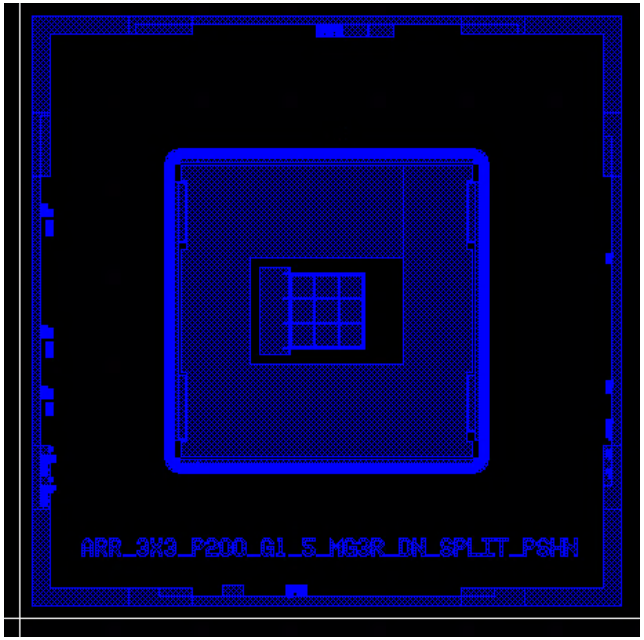
Pad_ava design

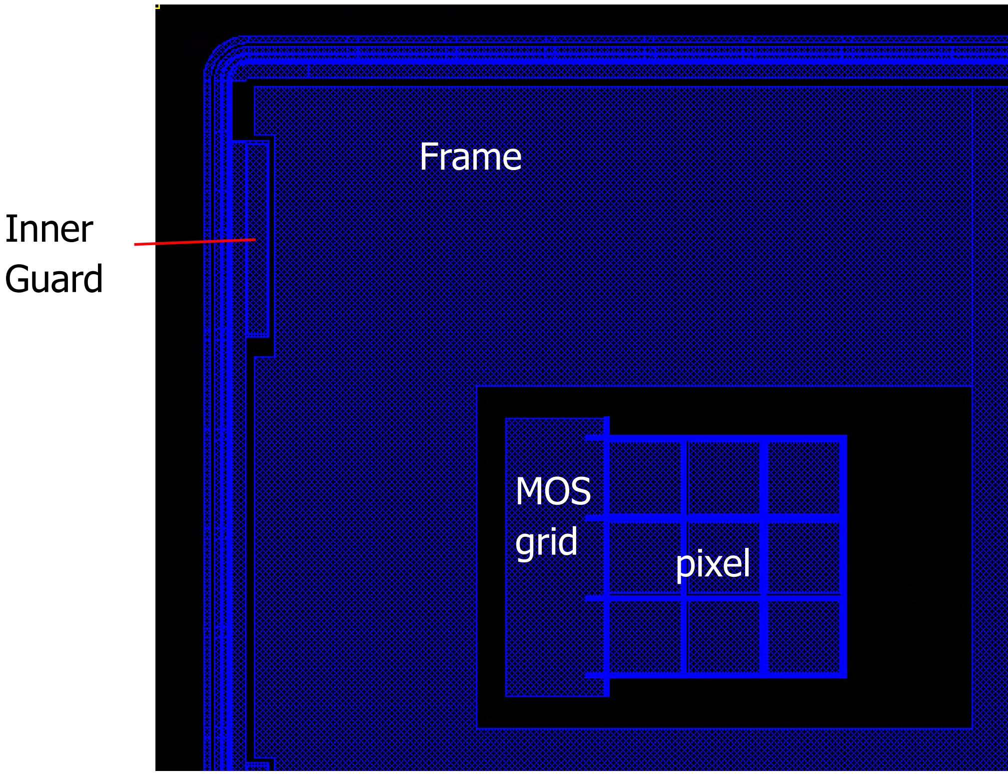


Pixel
Strips
Diodes
MGR Diodes

to be finished soon ☺

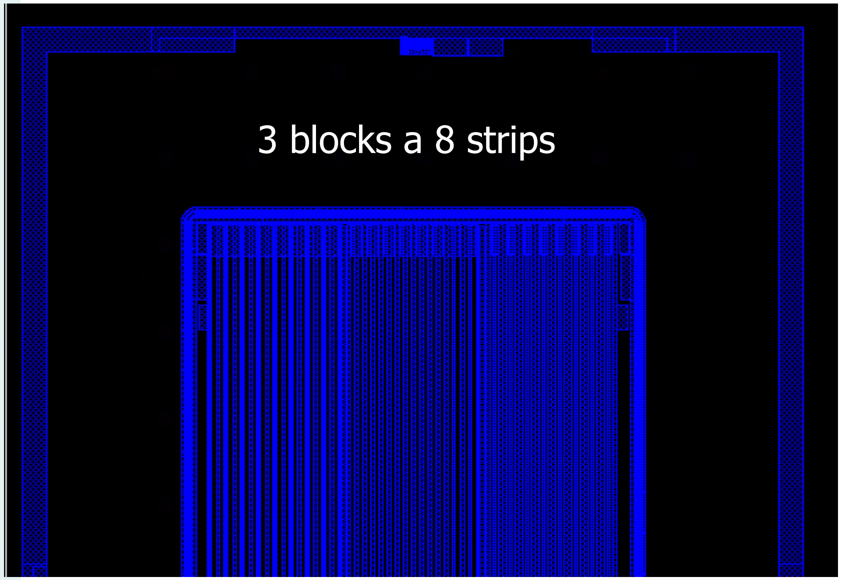
Pixel

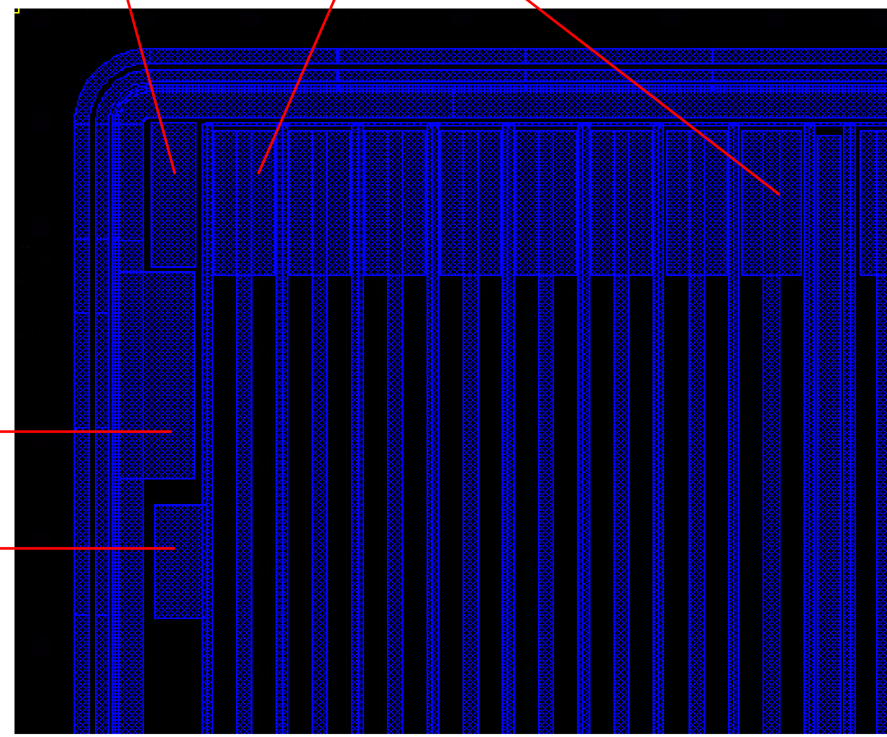




Pixel chips: 3x3 pixel, pitch 50µm and **200µm**, chip size 5x5mm²
Variations: pixel n+ gap 1, 1.5, 2, 2.5, 3µm and multi guard ring structures

Strips

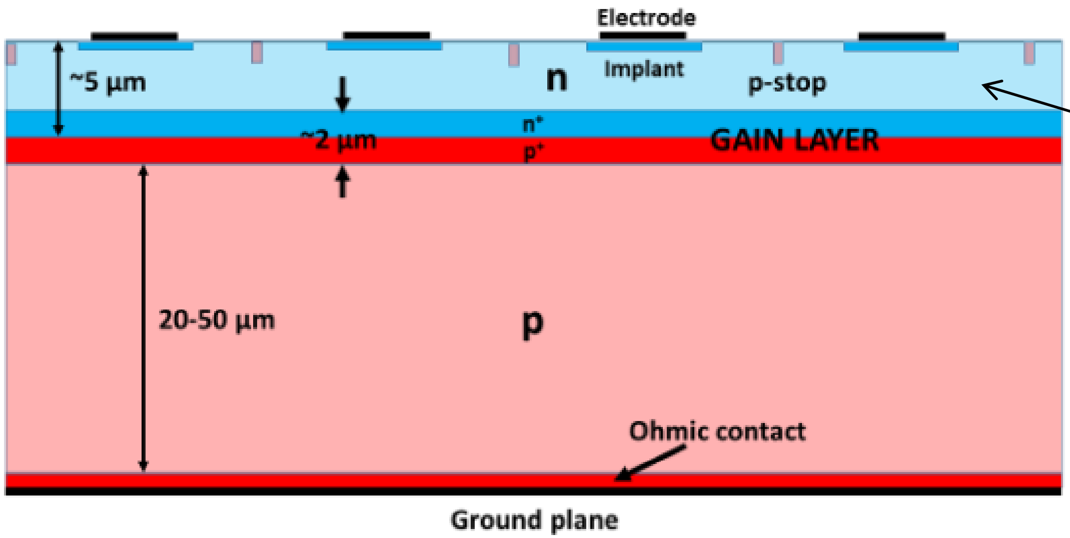




Strip chips: 3x8 strips, pitch 50µm and **100µm**, chip size 5x10mm²
Variations: strip n+ gap 1 … 50µm and multi guard ring structures

We are not alone anymore

Deep Junction LGAD
same principle for E peak suppression



Thick epitaxial layer
instead of HE implantation

Optimized for particle detection

S.M. Mazza et al, Univ. of Santa Cruz (2022)

Summary

Martha – a new approach for an APD pixel array

operated in RT proportional mode

(almost?) no inter pixel dead space by suppression of edge breakdown

suitable for large pixel arrays ?

low excess noise due to HE high field implantation

encouraging pre test results (Dio12)

First proto typing – small APD arrays and strips will be finished soon

next steps:

Prepare measurements (already ongoing)

Start discussions with potential users and ASIC designers

Show stoppers ?

Temperature effects

- temperature gradients introduced bc ro chip
  - > gain gradients

Hard errors by heavy ion induced charge generation

Temperature behavior of avalanche pixel array

Leakage current

SIPM very sensitive – ideally each generated e/h pair triggers a signal

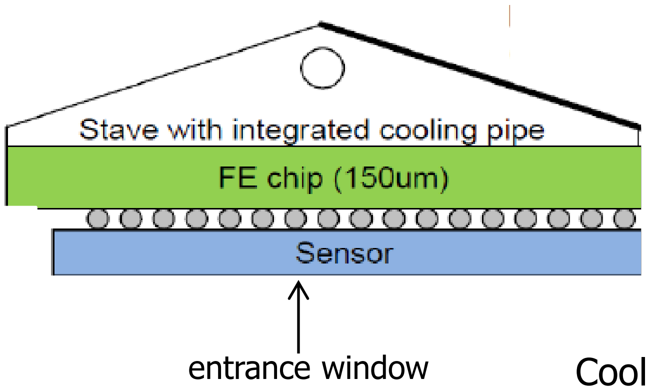
Quite different for classical proportional APDs
very different for APD arrays !

Gain and Noise vs T

Temperature gradients within an array

What is a optimal Temperature?

Temperature effects I - Heating of APD array by bumpbonded ro chip



Cooling through FE chip !

Sensor cannot get colder than FE chip

Temperature affects in APDs ?

Leakage current (SRH) gets amplified - no dark rate problem as in SiPMs

Back on the envelope …

HLL leakage current level better 100pA/cm² at RT

Scaling to a 1µm² -> 1e-18 A about 10 electrons/second

Assuming a 100x100µm² pixel size -> 1e-14 A or 1e5 electrons/s

Assuming an APD response time of 100ns -> 1e-2 electrons within 100ns

Typical soft xray signal of 200eV -> ≈ 60 electrons

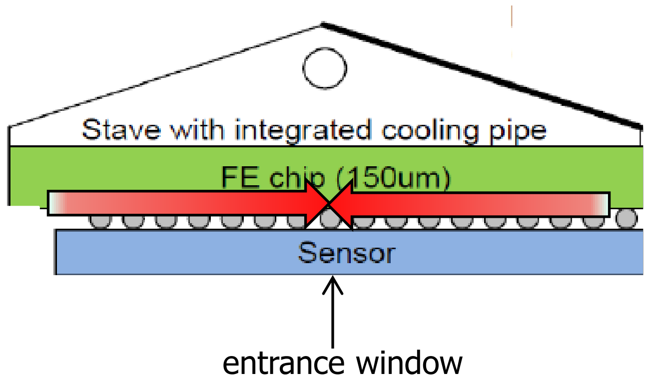
Thanks to the pixelation - head room for warming up

An increase by a factor 100 (would 1e-2 e- -> 1e-) still leads to $S/N_{leakage} \approx 60$

Taking the rule of thumb that leakage current doubles every 7 grd

$$100 \approx 128 = 2^7 \rightarrow \Delta T\ (7x7grd) \approx 50° \rightarrow T_{op} \approx 70°C$$

Temperature gradients introduced bc ro chip - > gain gradients



Cooling through the FE chip !

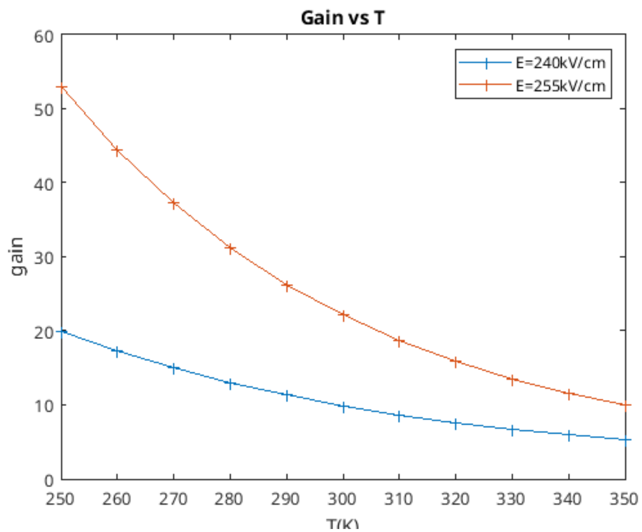
The hotter the latice, the more vibrations,

the shorter the mean free path for carriers in the electric field,

the less energy can gain between two collisions, the lower the avalanche gain

Avalanche gain has a negative temperature coefficient

Simple Estimations

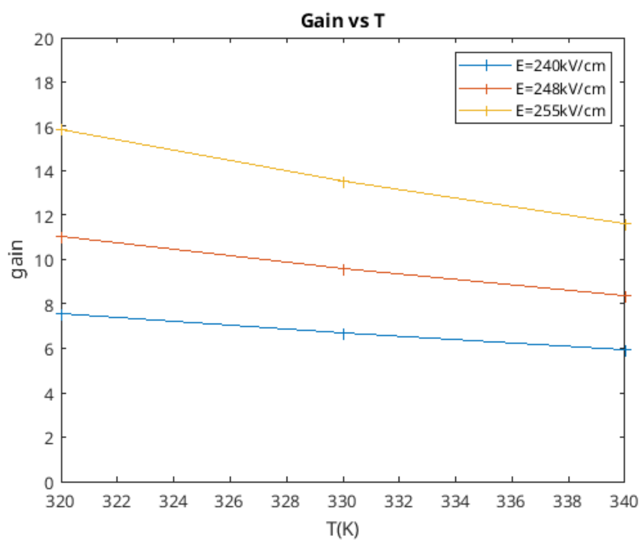


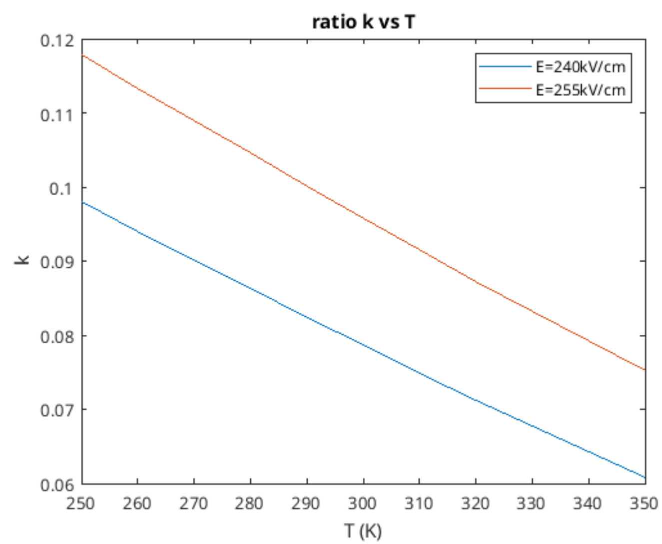
$$M = e^{\alpha\, t_{hF}}$$

E = const., but α = f(T) reduced mean free path (Overstraeten, de Man)

t_{hF} = 5.5µm

lower gain estimate no holes are involved





Excess noise vs T is not an issue

Slope @50C°: -0.14/K @gain=10

M should be adapted (by implanted dose) to expected T_{op}

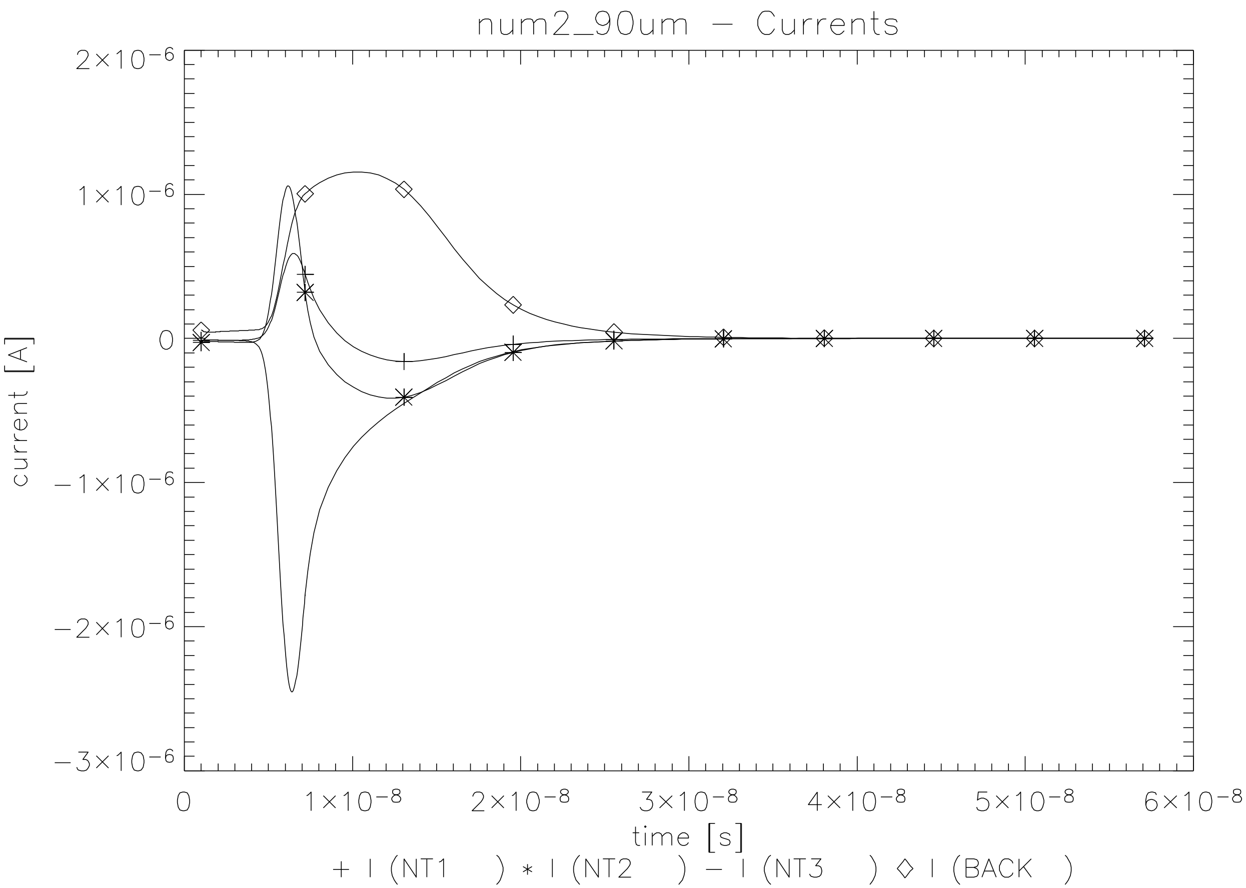
Hard errors ?

In the 80's
scaling of DRAMs – smaller charge stored at capacitors of 1T cells
spontaneous soft errors were observed "0" (less charge state) switched to "1" (more charge state)
??

Spurious radioactive element (U and Th) contaminations in Al and Si
radioactive decay –> alpha particle emission -> generation of more than 10^6 e/h pairs
-> collection by capacitor -> soft error (not destructive)

If this happens in an APD array …
(partially) shorts the diode high voltage -> sensitive amplifier input sees part of
the voltage drop and could be destroyed – hard error ☹

Counteractions ?
input protection for RO electronics (simple clamp diodes, Andreas)
thinner sensors (voltage reduction – drift region)
thinner high field region (voltage reduction, but more excess noise)

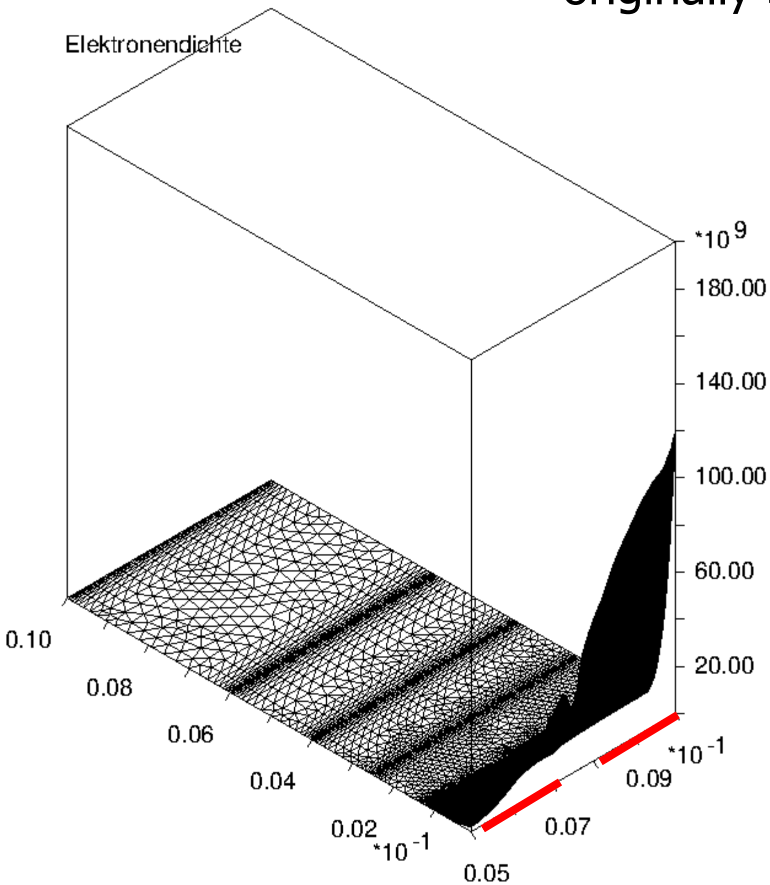

num2_90um – Currents
current [A]
time [s]
2×10⁻⁶
1×10⁻⁶
0
−1×10⁻⁶
−2×10⁻⁶
−3×10⁻⁶
0
1×10⁻⁸
2×10⁻⁸
3×10⁻⁸
4×10⁻⁸
5×10⁻⁸
6×10⁻⁸
+ I (NT1) * I (NT2) – I (NT3) ◇ I (BACK)

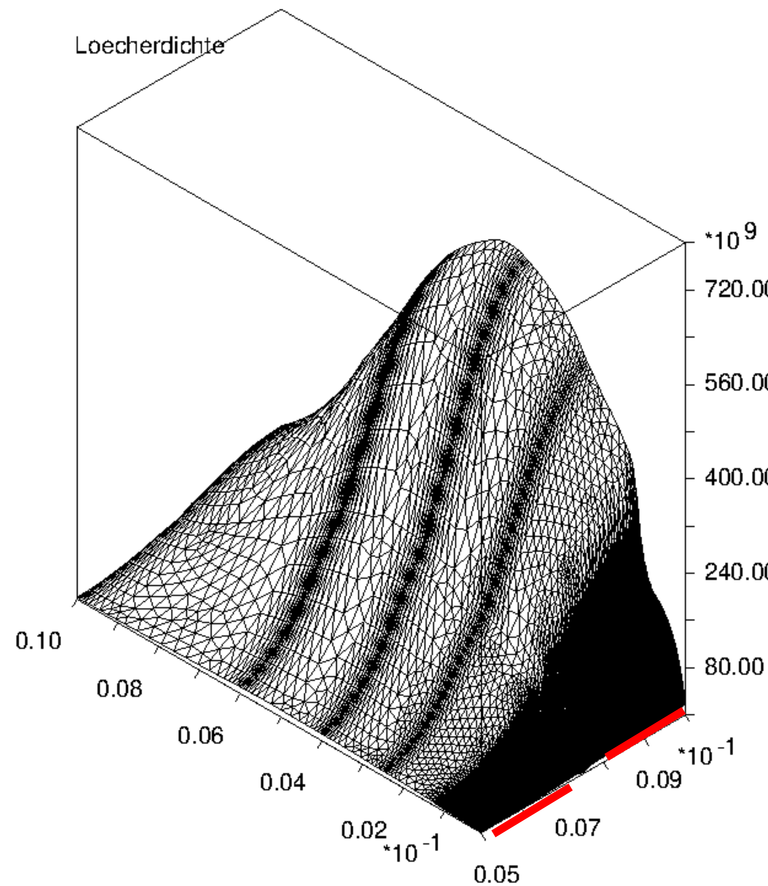
Charge carrier densities 6.1ns after signal arrival

Electrons

Holes

originally same amount of





Electrons are rapidly extracted towards the anode
Not seen by the neighbors

Holes are still on their way to the backside
clearly seen by the neighbors