The EDET 80k Sensor Concept

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for the EDET collaboration and HLL

Design and technology
Belle heritage
Special requirements
Rad hardness

Sensor Requirements – 256k pixel quadrant

80kHz frame rate	-> fast (rolling shutter, 100ns per row)
High position resolution	-> thin sensor, small pixel
Rad. Hardness	-> multiple measures
Compact module design	-> ASM with bump bonded control and ro chips

Almost same as Belle2 PXD requirements

4 quadrants a 256k pixel

ASM module with thinned sensor region (suppression of multiple scattering of medium energy electrons)

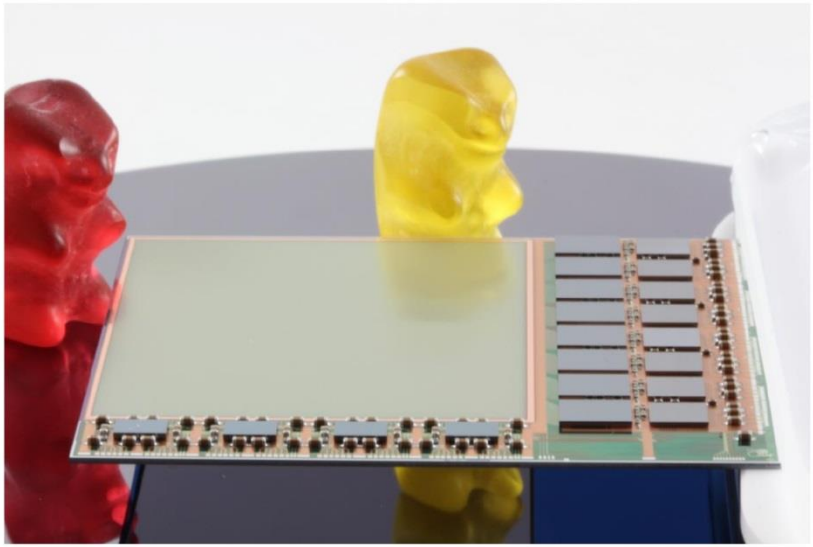
Two-side buttable (narrow gaps between quadrants)

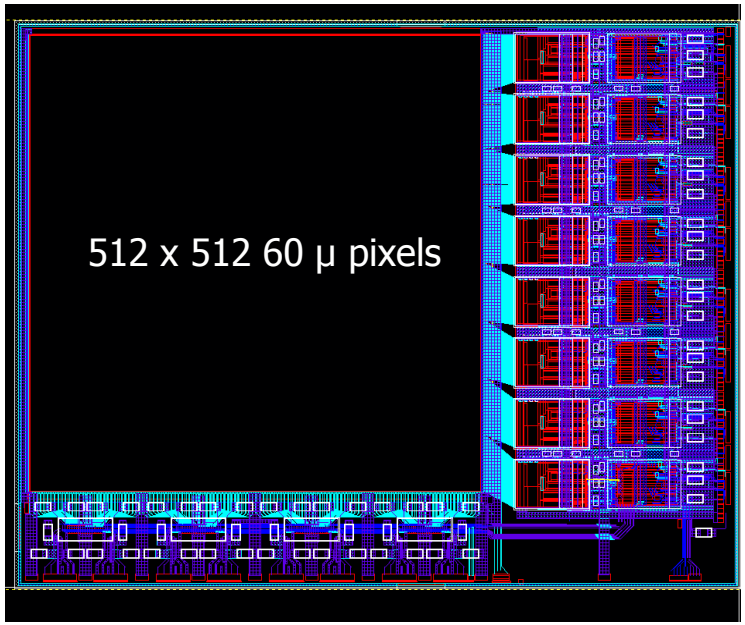
Two thichness options 50µm and 30µm

Flip chipped control (Switcher) and readout chips (DCD-E, DMC) connection via bump bonds

Operation in rolling shutter mode (only activated row consumess power)

Operation in vacuum –> no active cooling of thinned region

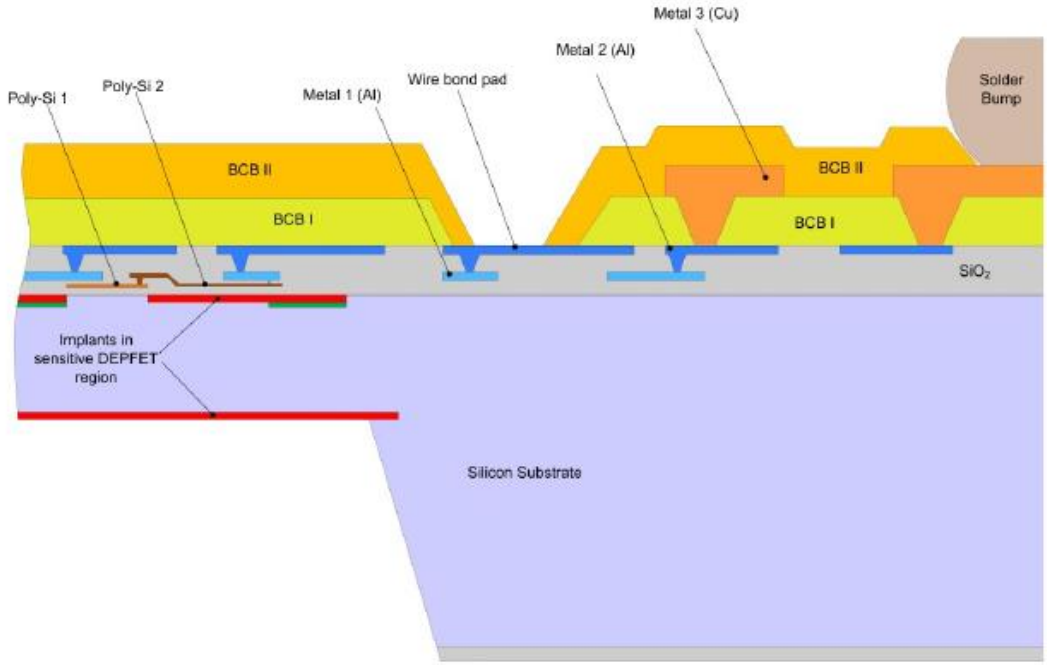




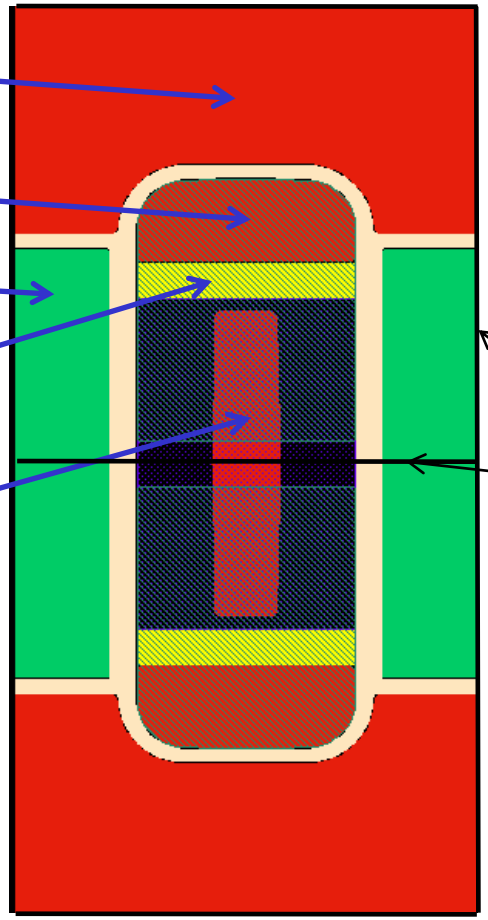
Belle-like technology with some modifications

Starting material top wafer (30µm or 50µm, resp.) wafer bonded to thick handle wafer

- Production in three phases, 19 lithography steps
  - ↳ 9 implantations, 2 poly-silicon layers
  - ↳ 2 aluminum layers
  - ↳ last metal copper and thinning of sensitive area



Flipped Double Cell Concept (poly layers and implants only)



Drift

Drain

Clear

DEPFET Gate
(poly 2)

Source

Clear Gate/
Separator
(poly 1)

Squared Pixel

Neighboring pixels share
Clear, Drift and Source

-> compact design - pixel 60µm size

Pixel borders

Suitable for fast 2-fold or 4-fold
readout

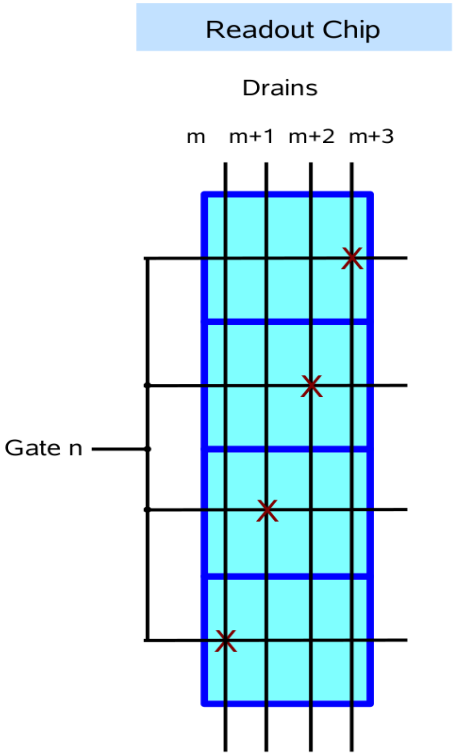
P doped regions: red

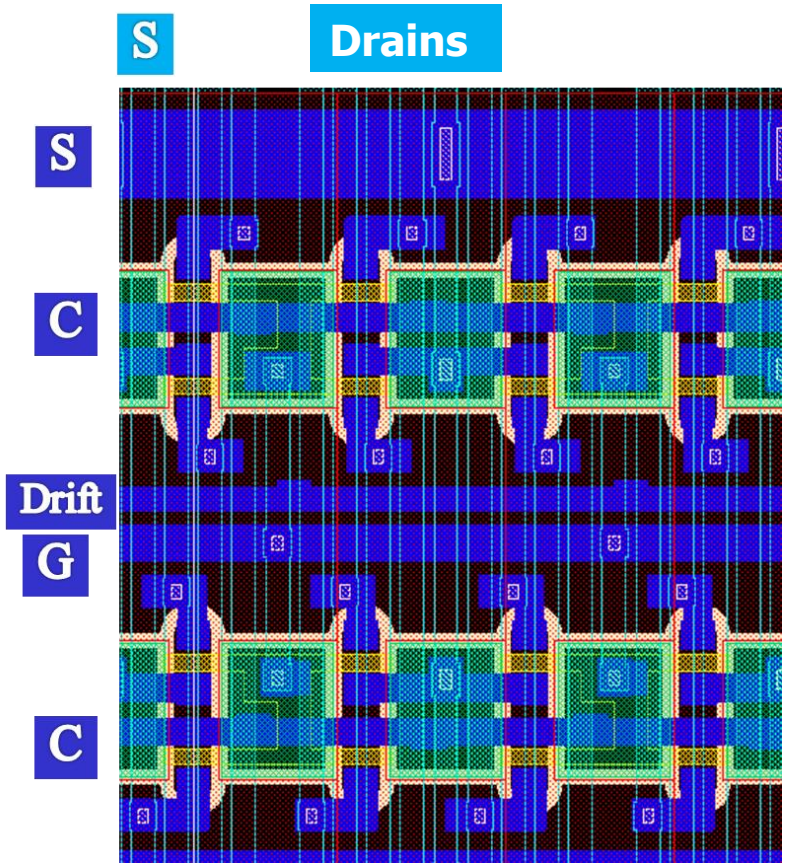
N doped regions: green

4-fold readout

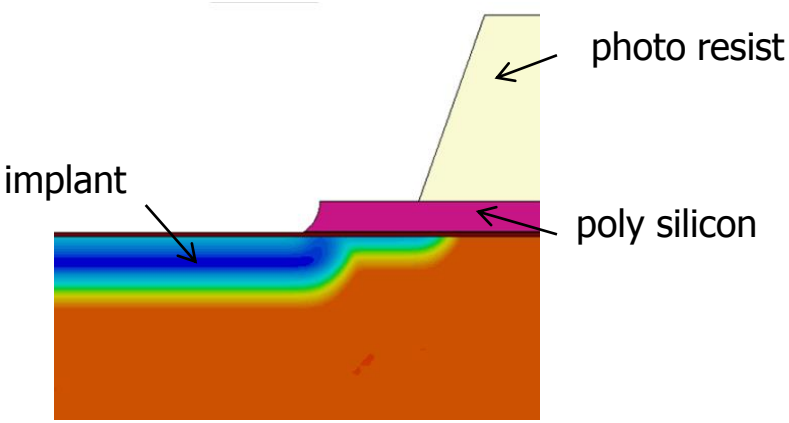
Readout of 4 physical pixel rows simultaneously

4x less switcher channel
but 4x more drain readout lines (DCD)
4x higher frame rates (rolling shutter)





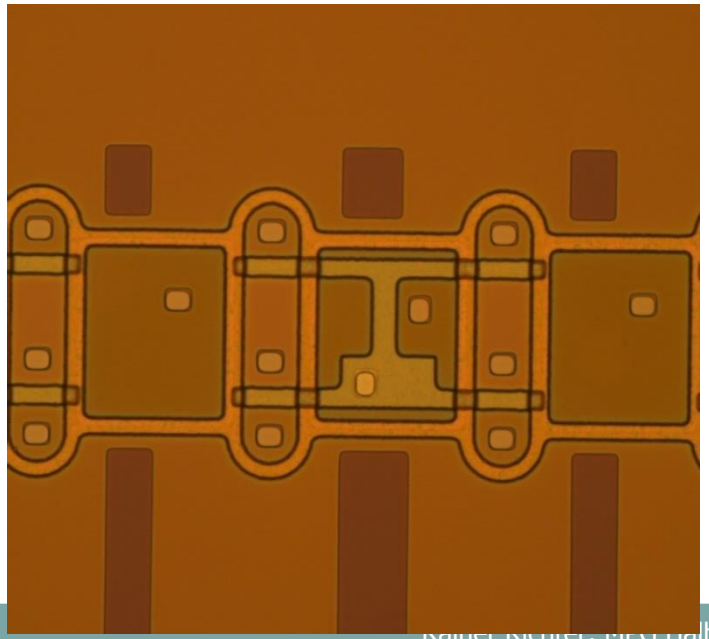
Self-aligning technology



Self alignment of implants w.r.t. polysilicon
using the stopping power of poly for implants

Reproducibility of charge collection
and amplification within matrix
defined by lithography alignment tolerances
of poly layers and implants

just one sensitive alignment tolerance
Poly2 -> Poly1

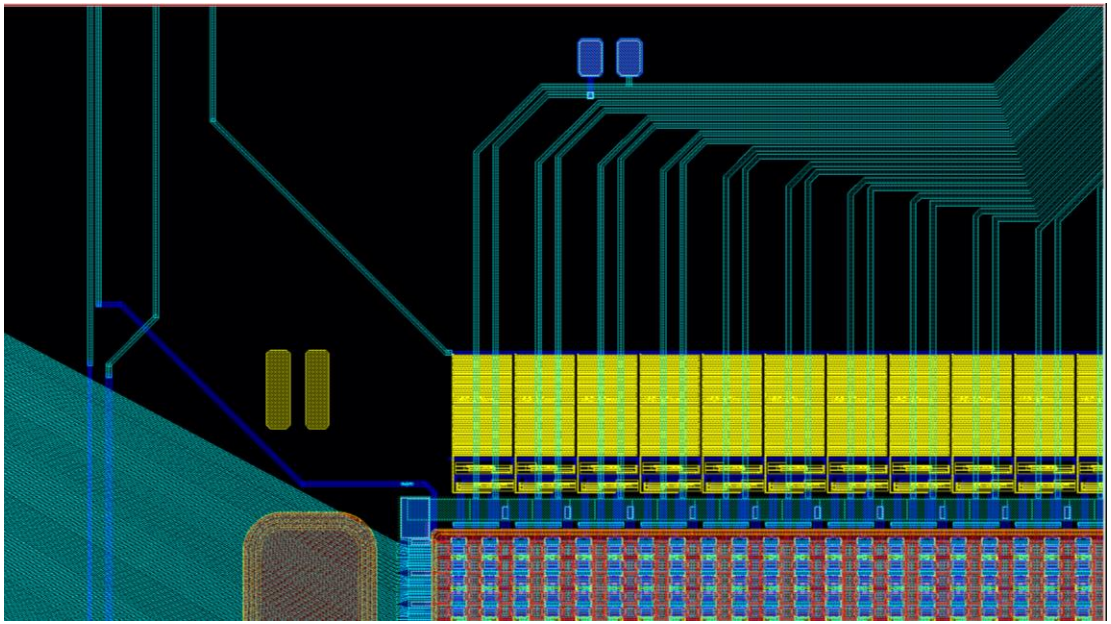


Testability – simple methods but important ones

Poly silicon Bias resistor for each **control line (Gates and Clears)**

Setting the whole matrix in bias state with minimum voltage supplies

Used for testing (looking for severe failures – metal shorts at a production state where repairing is possible))

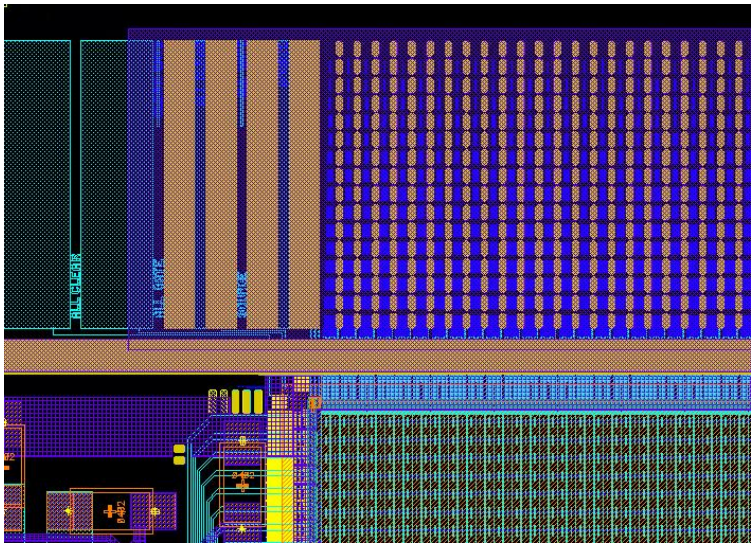


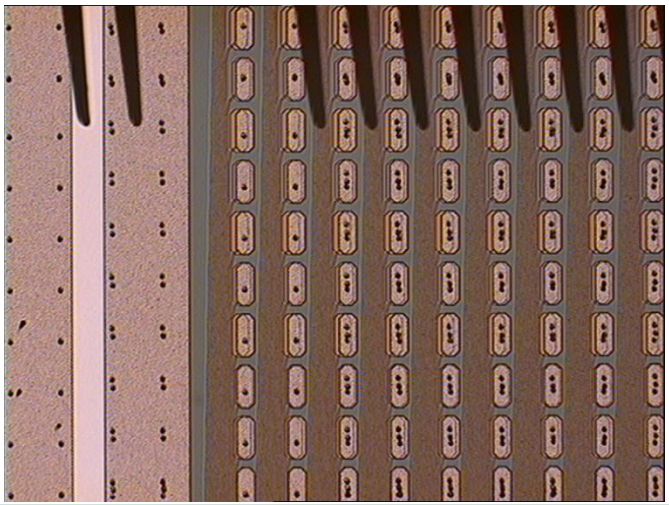
Inline Testing

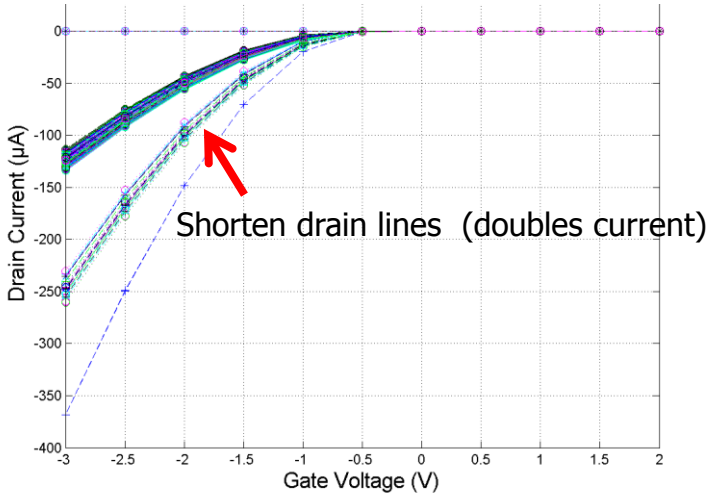
Readout lines (Drains) are connected via test fanout connected by probe card
Test of the transistor row (simple IVs)

Disconnection of test fanout when tests are finished

activating 1 Gate (depfet row) measuring drain currents
-> sample of IV curves
-> any shorts between drain lines
-> any interrupted darin lines (opens)
non adressed gate rows are kept passive by resistor bus structure





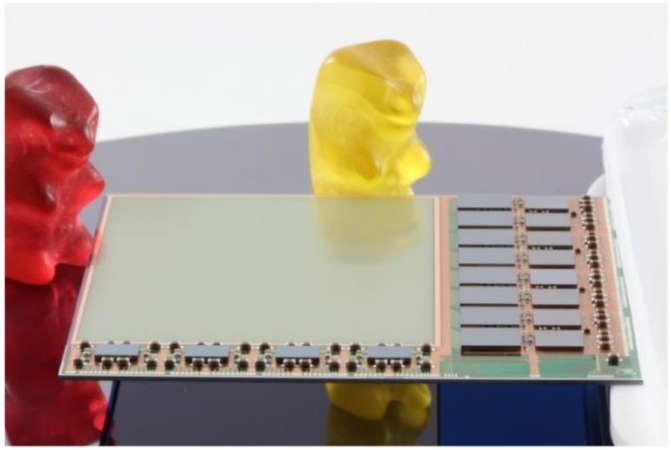


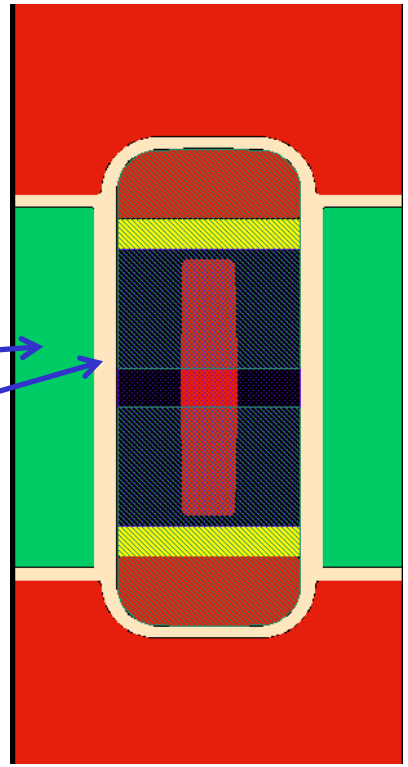
More fancy design feature - CCCG

Actually DEPFET has three control lines: Gates, Clear, and ClearGate
No space at balcony for an additional switcher chip
and within pixel for a futher metal line

Saving one switcher channel (for Clear Gate) by a design feature
called capacitively coupled clear gate (CCCG)

Making use of the 'parasitic' overlapp capacitance
between Clear and 'floating' ClearGate





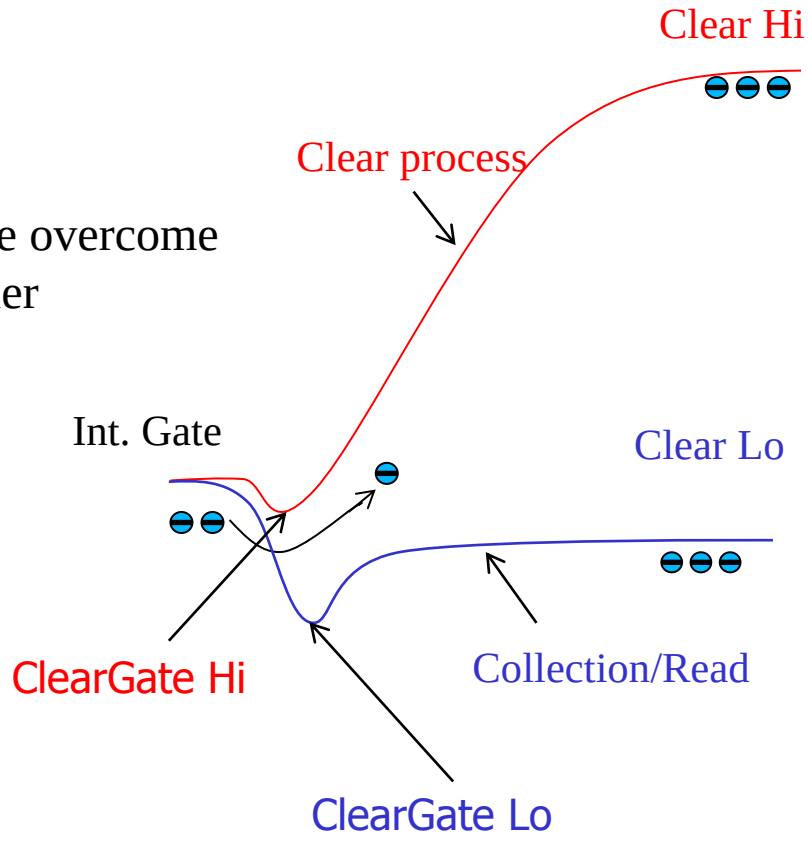
$$\Delta V_{clg} = \Delta V_{cl} * \frac{C_{Cl\_CLG}}{\sum C_{CG\_i}}$$

Coupling factor 0.2 (estimate),
complete Clear at Vclear = 15V (Edi Prinkler)

Principles of Clear process – potential in IG, CG, Cl region

N-buried channel MOST operated in source follower mode

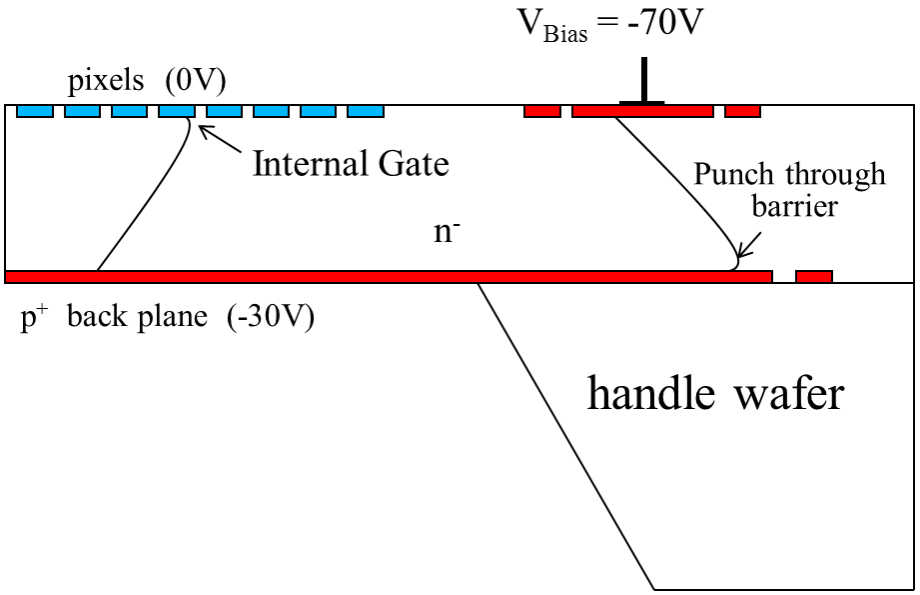
electrons in the Int. Gate overcome
the small potential barrier
by punch through



ClearGate Hi increase by 1V saves about 3V … 4V of Clear Hi

Full module biassing from top side

Back side biassing via puch through mechanism from top facilitates module construction



EDET:
50µm (30µm) thickness
-> V_{bias} about -30V

Idea for biassing SDDs by C. Fiorini, A. Longoni, Peter Lechner, 2000

Almost the same requirements as for Belle

80kHz frame rate	-> fast (rolling shutter)
High position resolution	-> thin sensor, small pixel
Rad. Hardness	-> multiple measures
Compact module design	-> ASM with bump bonded control and ro chips

Large charge handling capability

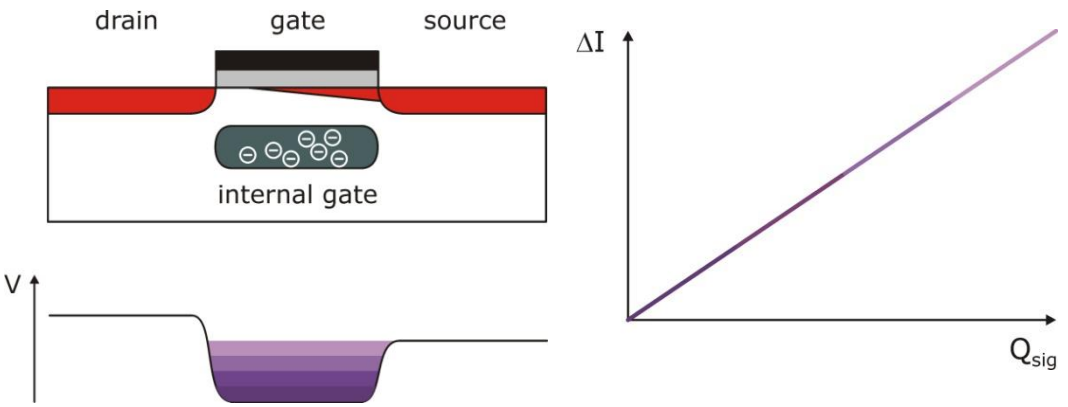
Internal Gate of Belle pixel stores about 50 k electrons

For EDET we need about 1M !

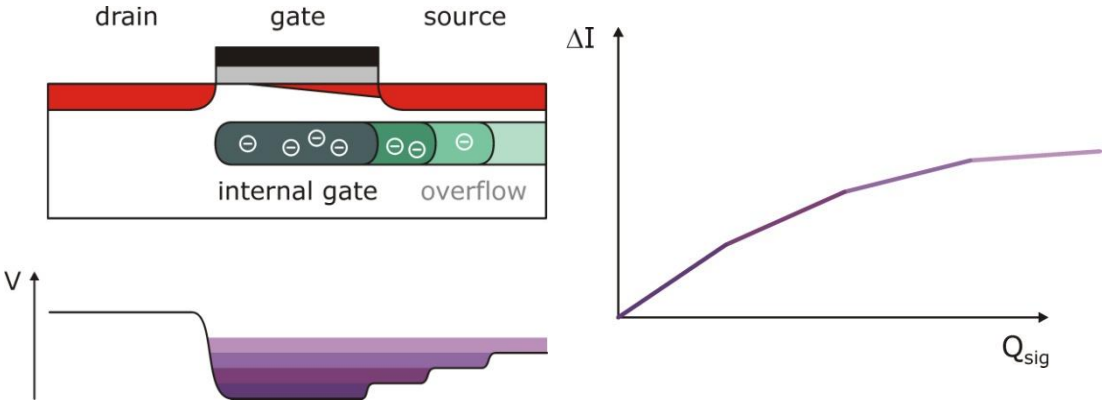
But there was a solution which we had to adapt

DEPFET with Non-linear Gain

- spectroscopy-type DEPFET
  - all signal charges stored under FET channel
  - all signal charges cause an equal effect on the FET current
  - **linear $\Delta I/Q_{sig}$ characteristics**



- DSSC-type DEPFET
  - signal charges at high levels also stored under source
  - less/no effect on FET current
  - **non-linear $\Delta I/Q_{sig}$ characteristics**
  - gain curve engineering by dose & geometry of implantations

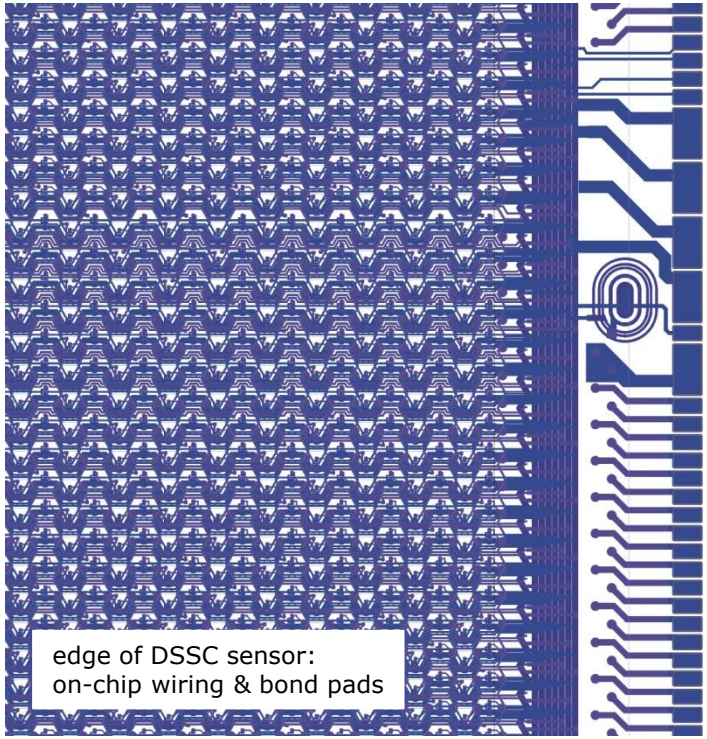


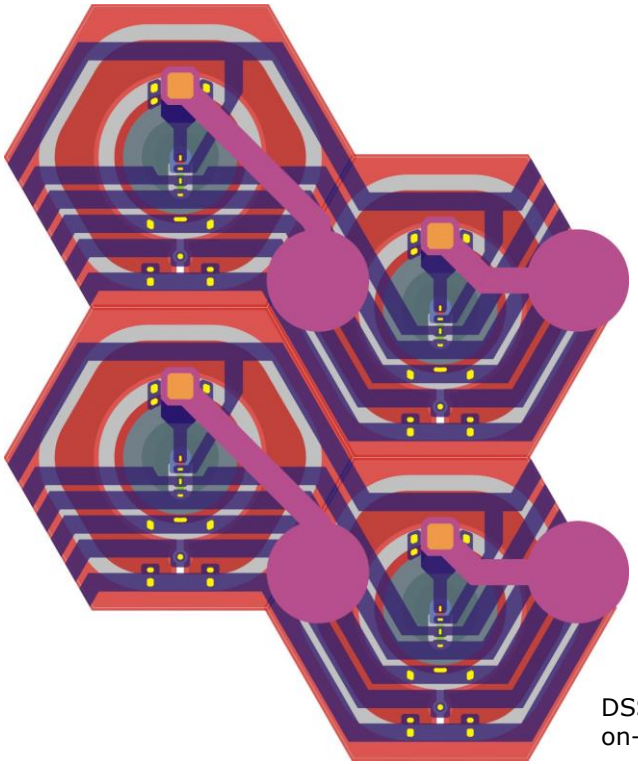
- calibration of non-linear gain curve
  - pixel by pixel
  - calibration procedure defined

NP1.M-230, mon
G. Weidenspointner
DSSC calibration

Xray photon counter

- layout
  - ▷ DEPFET & SDD, hexagonal pixels
  - ▷ pitch in x/y 204/236 µm
  - ▷ sensor format 128 x 256
  - ▷ zig-zag row-wise supply lines
  - ▷ irregular routing from hexagonal sensor pixels to landing pads in rectangular asic cells in ubm layer





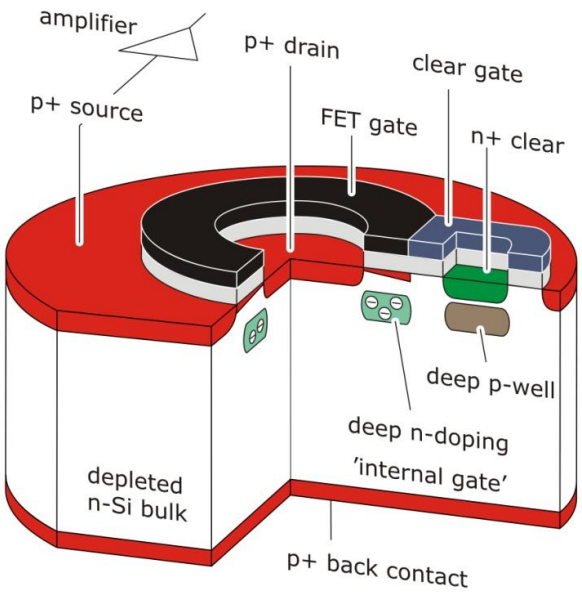
DSSC pixels,
on-chip wiring

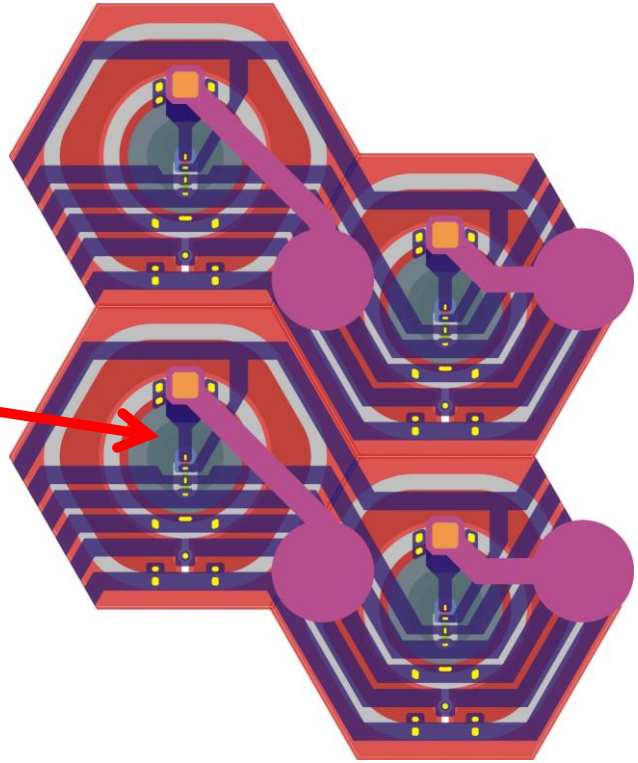
- ▷ horizontal supply lines end in vertical bus strips
  - ↳ connected to wire bond pad
  - ↳ supply of 64 x 64 pixel subunit
- ▷ bump & wire bond pads for ASIC i/o lines

See talk by Matteo Porro on Wednesday ☺

Circular Depfet surrounded by drift rings

very fast: 5MHz
Hybrid pixel detector approach (bump bonding)
thick silicon – 450µm

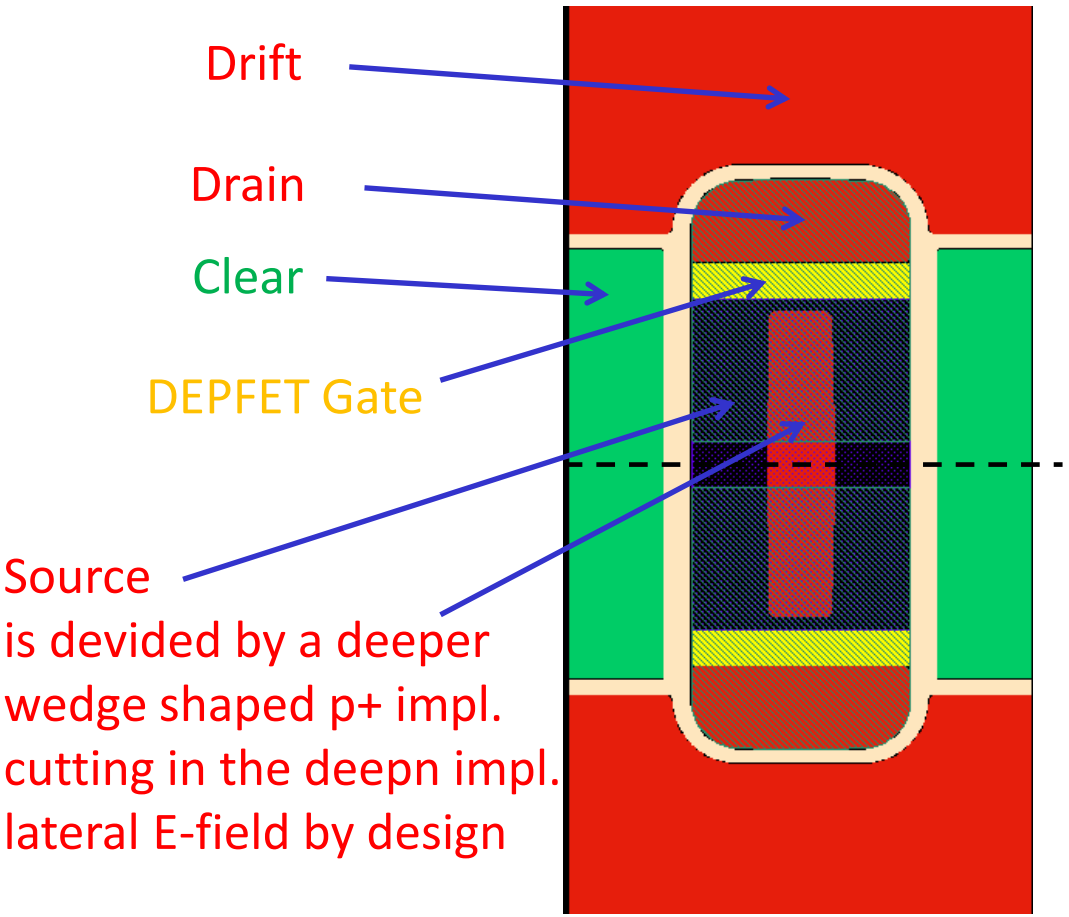


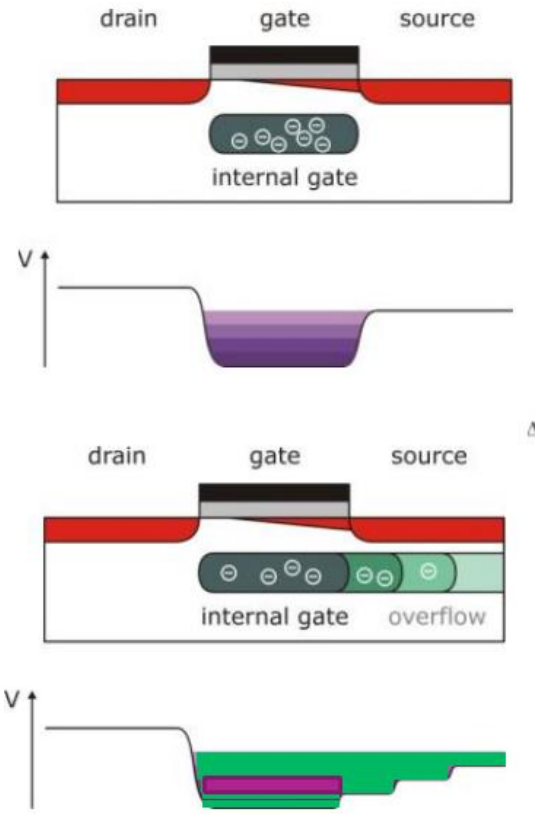


- DEPFET & SDD, hexagonal pixels
- pitch in x/y 204/236 µm

for EDET 80k - three problems: pixel size , mass, speed

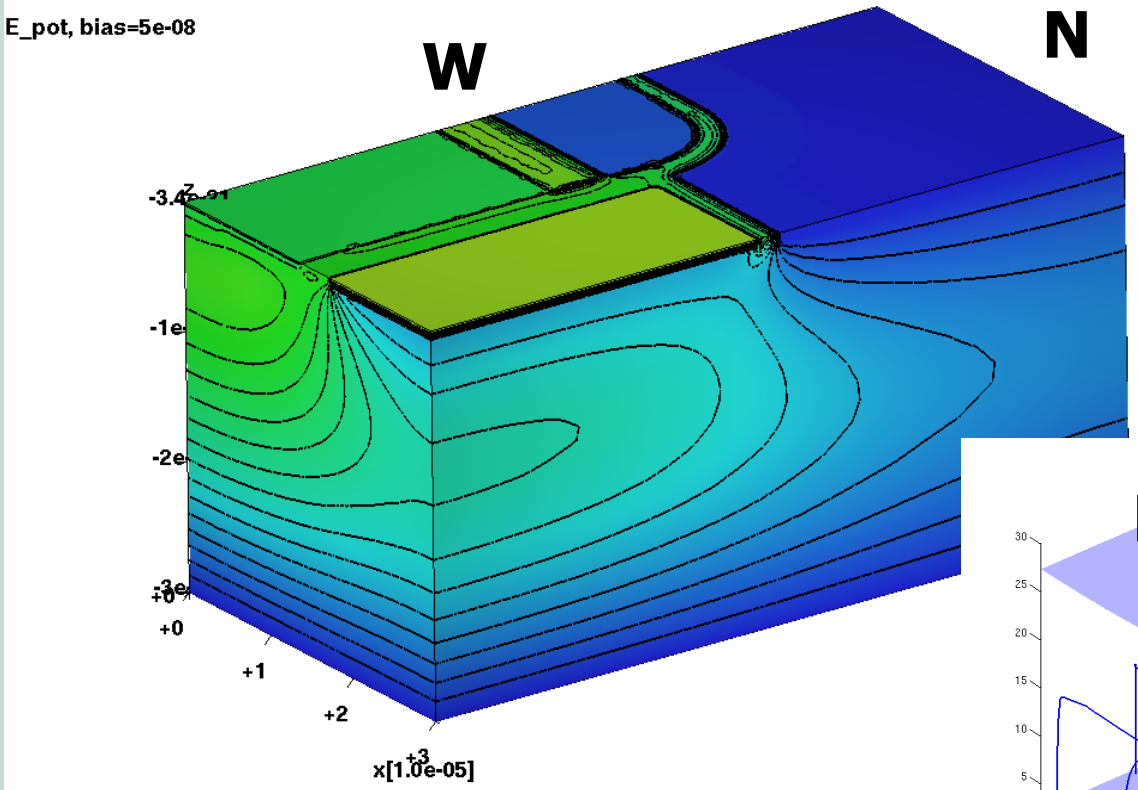
EDET approach – smaller linear transistor

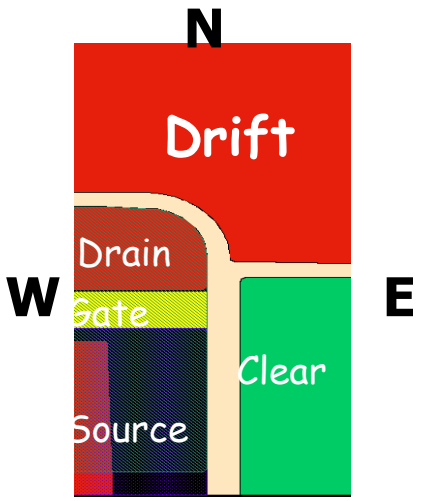


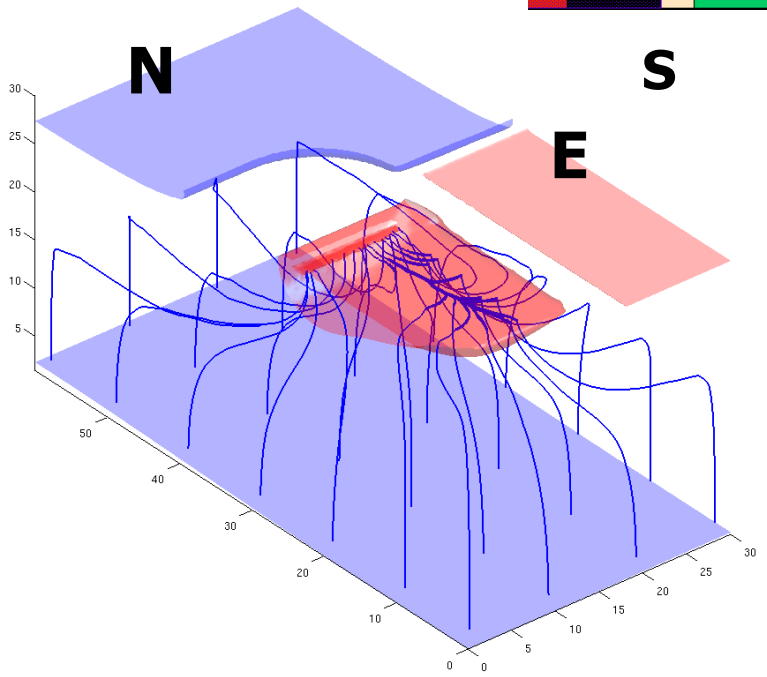


No need of multiple deep n-implantations as in circular designs

View from SE (Clear Side)

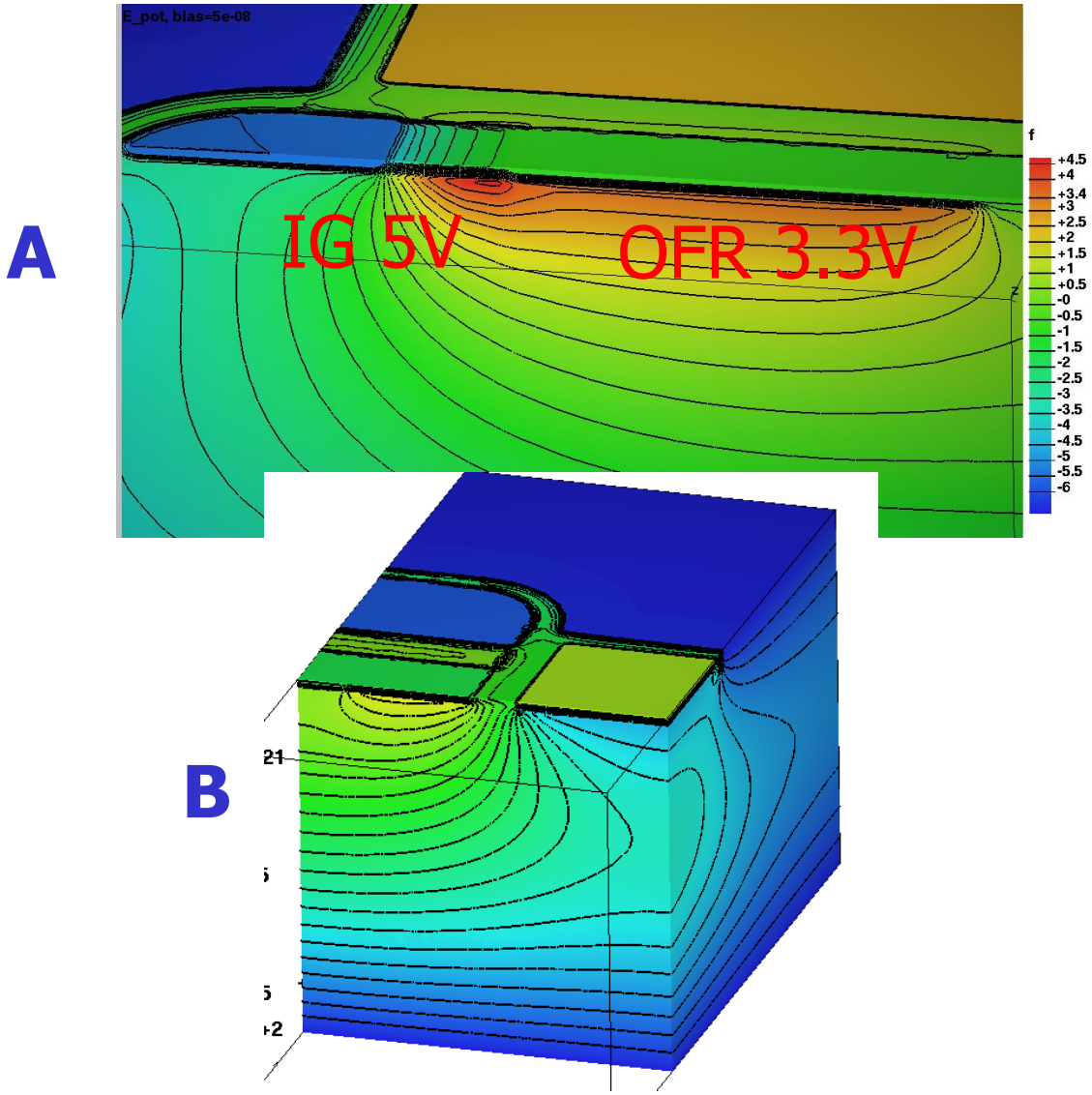


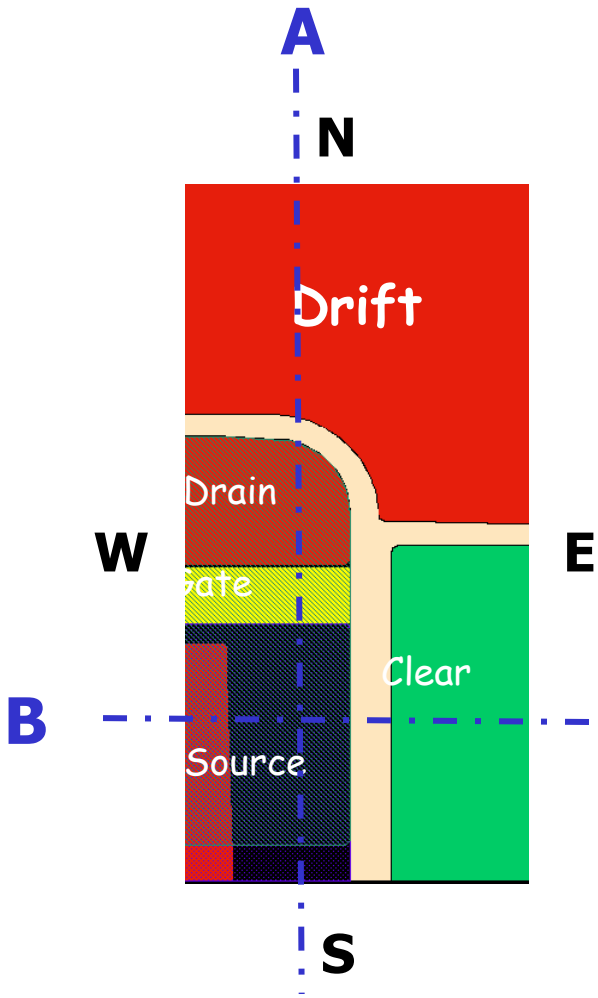




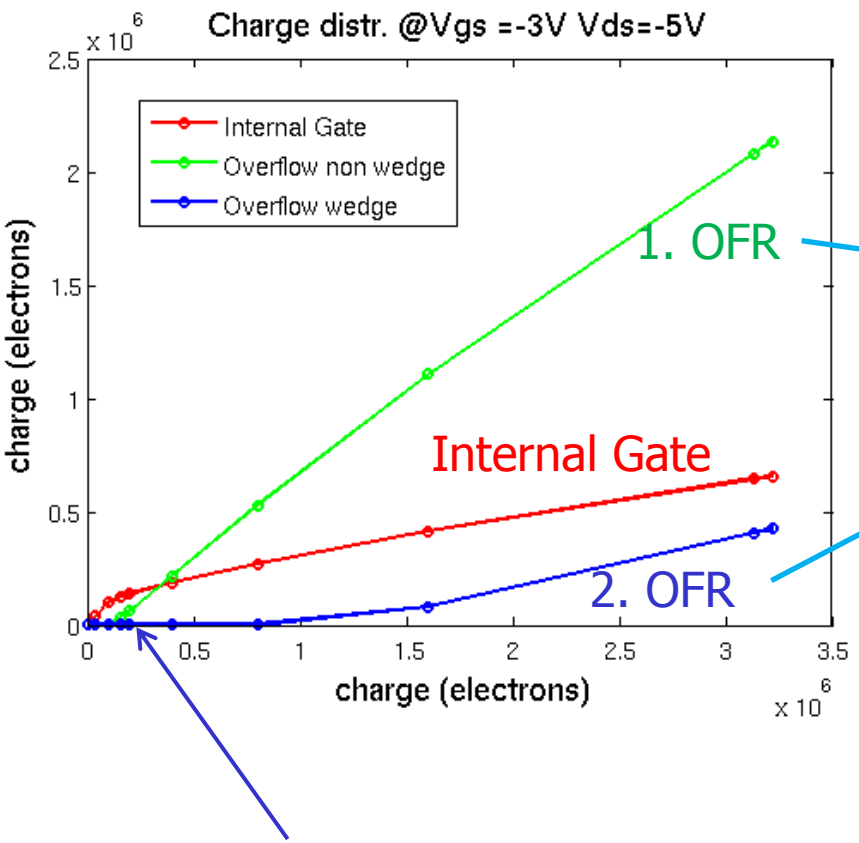
Simulated with Oskar3 (K. Gärtner)

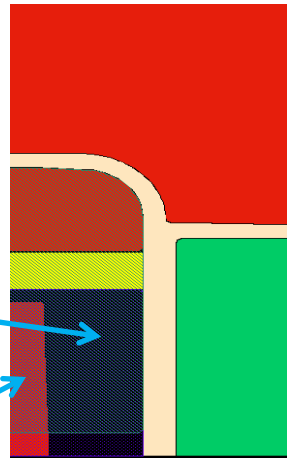
Charge overflow regions (OFR)

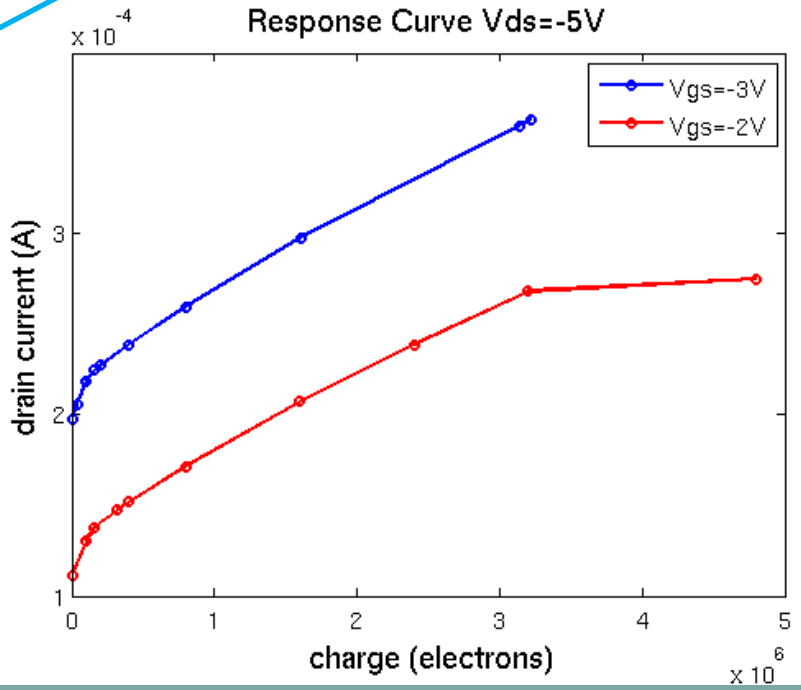




Charge distribution in storage regions and current response



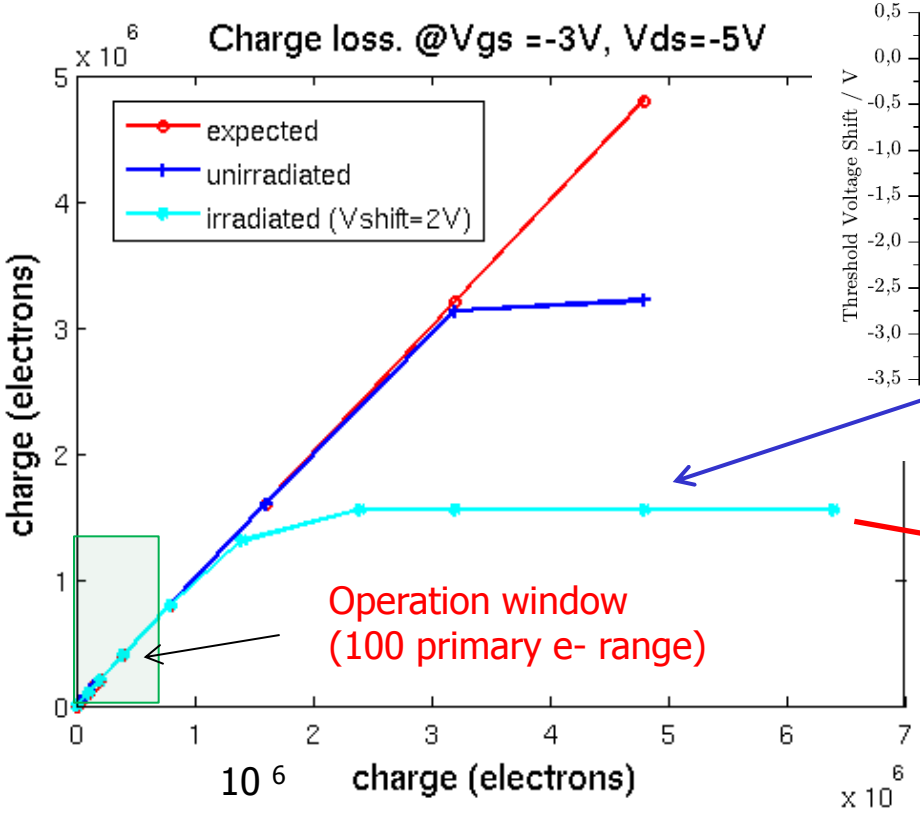


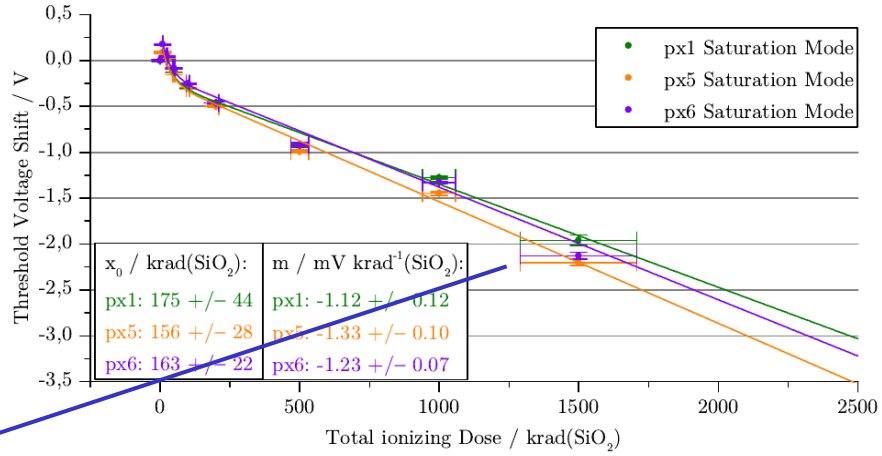


Onset of overflow

= onset of signal compression

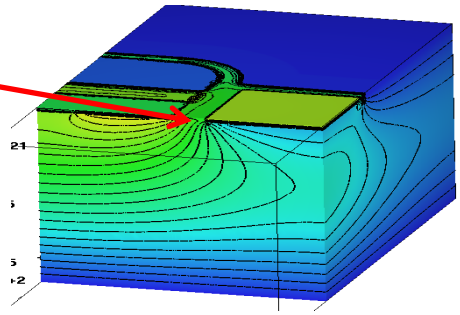
Challenge: Radiation Hardness





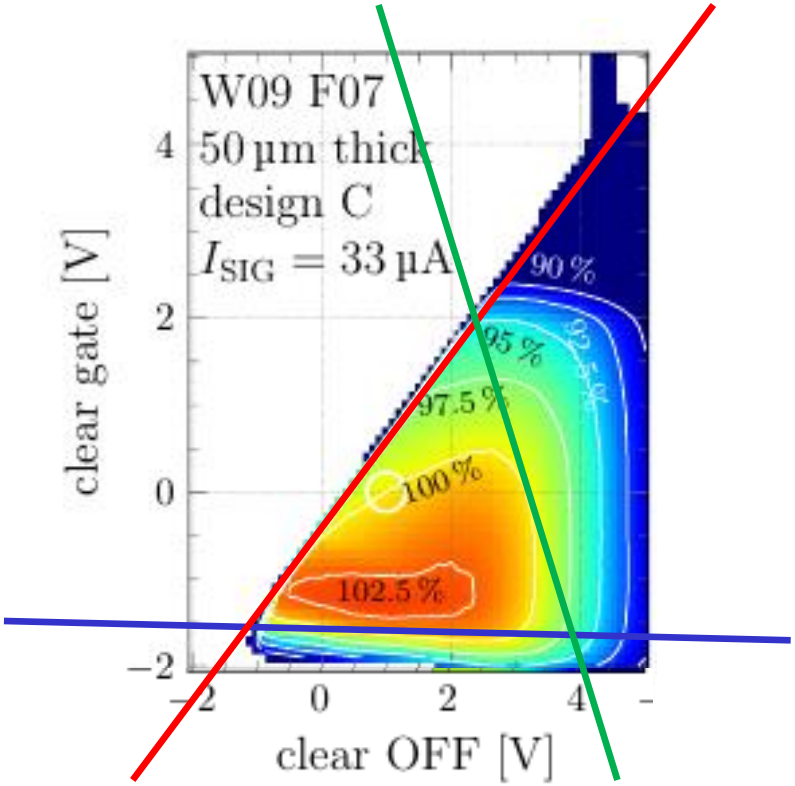
Operation window
(100 primary e- range)

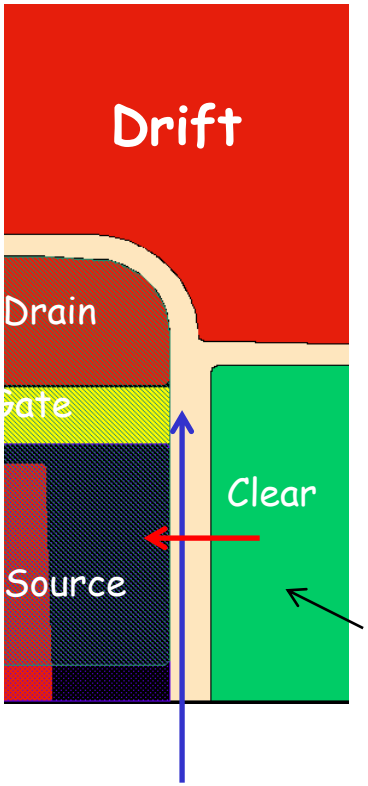
MOS



More radiation hard Clear Gate region !?

Clear/ClearGate voltages - operation window





Back emission of electrons from Clear

Fraction of signal charge Is 'collected' by Cl/CG

Parasitic hole current beneath Clear Gate

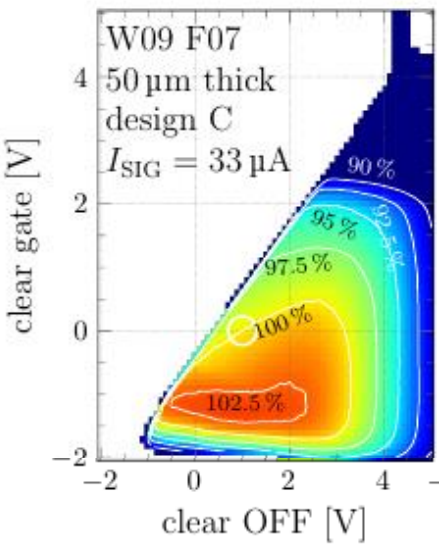
The larger the triangle the safer the operation ☺

Operation window vs storage charge

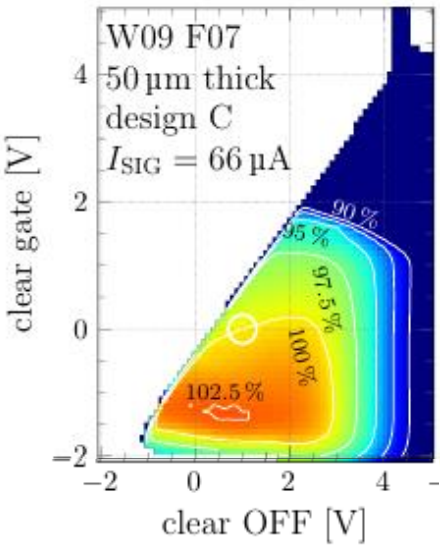
Assuming: Gq = 80pA/e- in signal compression mode

Measurements
by Mitja Predikaka

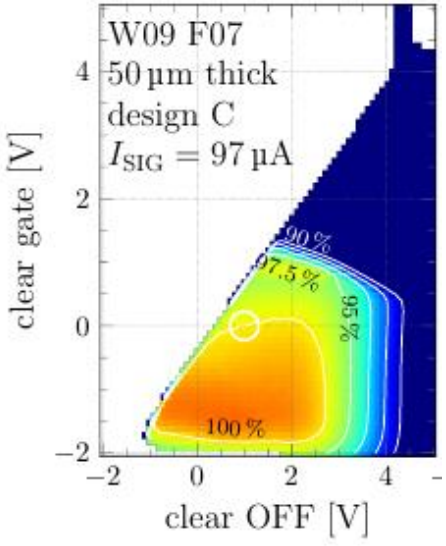
412 ke-



824 ke-



1210 ke-

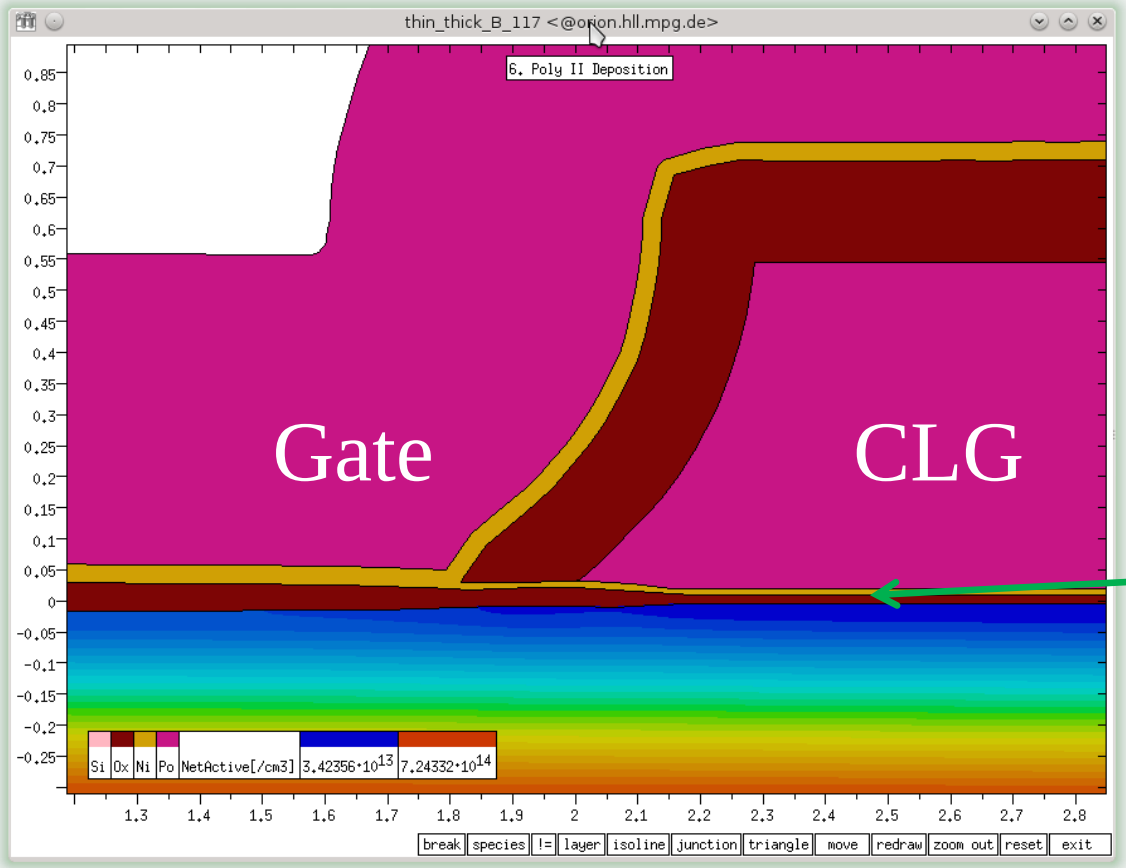


Operation window decreases if storage charge increases because
Barrier hight to ClearGate gets smaller
Storage regions become more negative and less attractive for additional electrons

Charge handling capability is very vulnerable to potential fluctuation beneath ClearGate
inhomogeous radiation damage

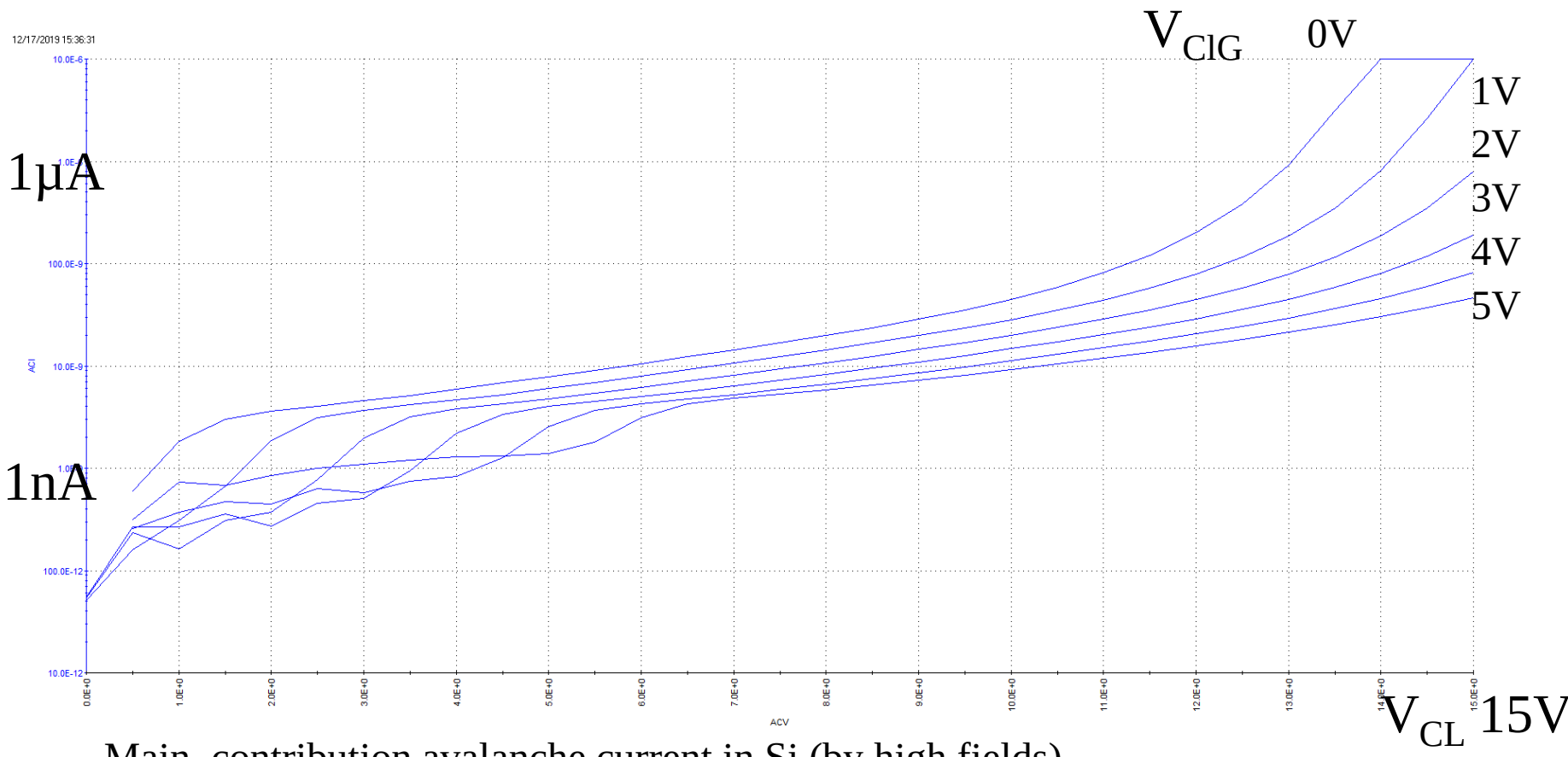
The thinner the gate dielectics the more rad hard

We processed Depfets with rather thin dielectrics beneath ClearGate



15nm nitride on
10nm oxide

Thin oxides survived - small test matrice

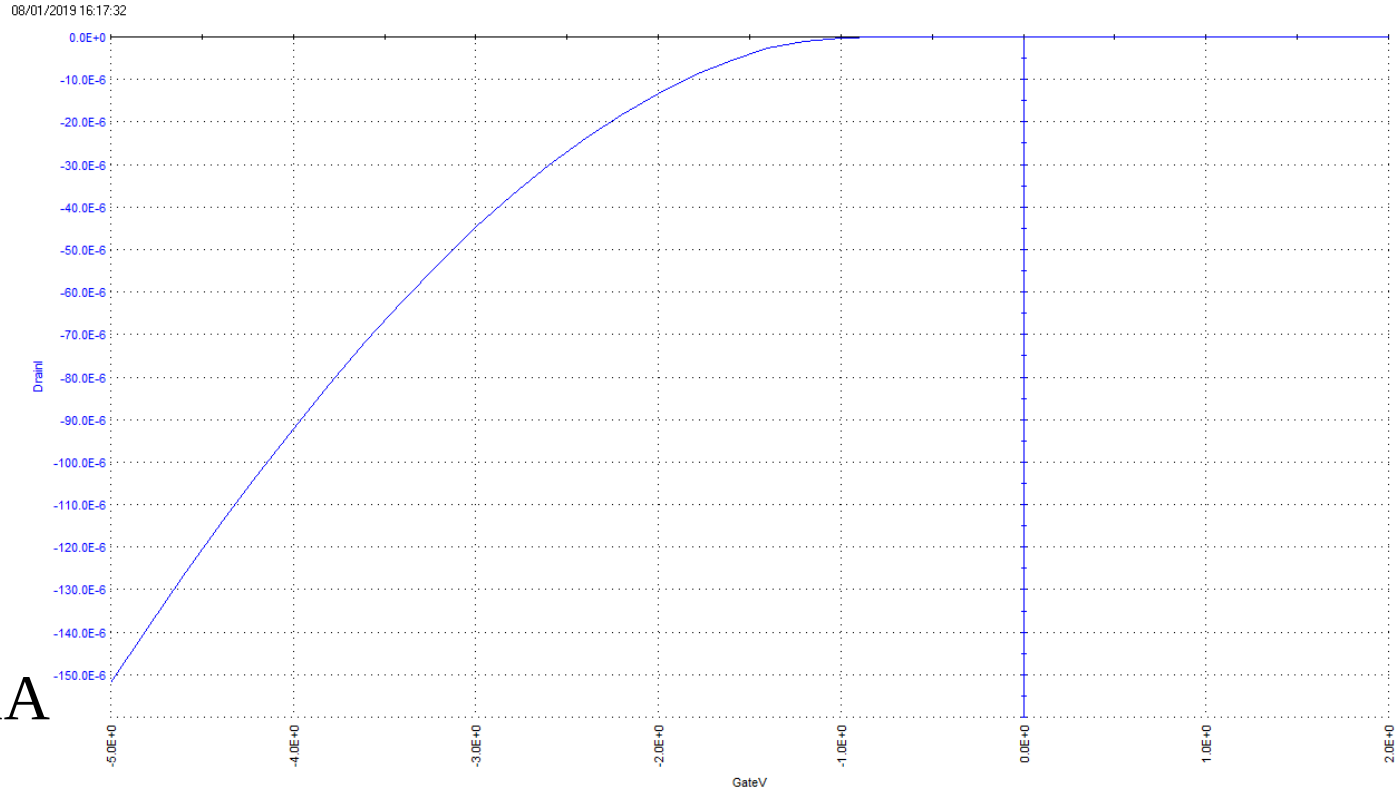


Main contribution avalanche current in Si (by high fields)

Insulator leakage is about 2-3 orders of magnitude smaller

Be carefull with Clear High Voltage – 14V … 15V max !!

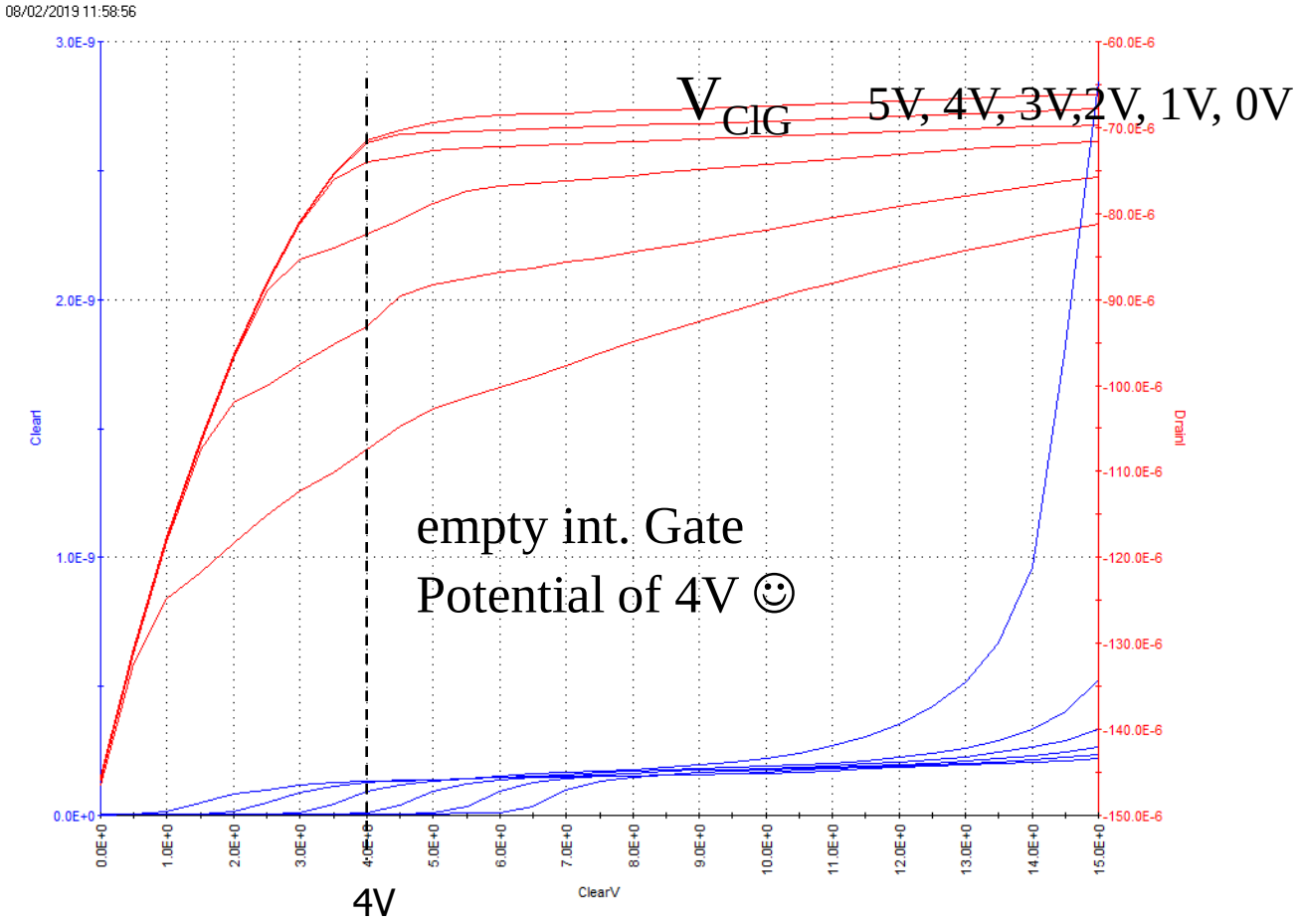
Typical transfer IV Id vs VG (Vcl=7V, Vclg=5V)
W15 H04 upper righ trans.



150µA

-5V

Measurement of empty Internal Gate potential monitoring clear gate currents (W14 H04) upper right trans. W/L=10/6



Radiation test and matrix operation see talk by Ch. Koffmane

Summary

- Survey through the EDET 80k sensor technology and design features
- Basic technology and many design ideas are taken from Belle PXD

- Differences
  even thinner very pixel regions (50µm or 30µm)
  rectangular DEPFET pixels (60µm x 60µm) with signal compression
  having a charge handling capability of > 1Mio. electrons
  (corresponding to > 100 primary electrons of 300keV)

- Inhomogeneous oxide damage in clear gate regions (poly 1) detoriates potential barriers affecting charge handling capability

- Prototype EDET sensors with very thin ClearGate oxide are under investigation

Thanks for your attention

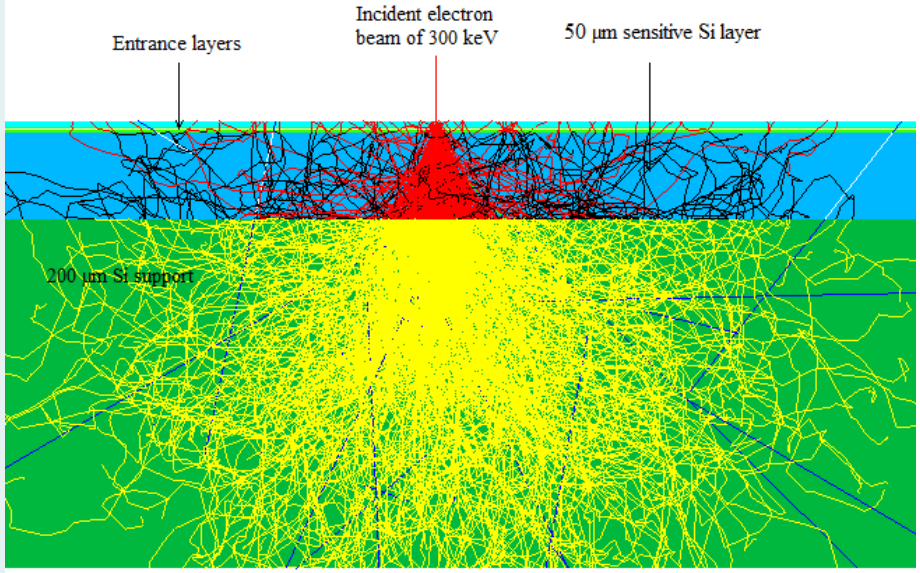
Position Resolution and Contrast

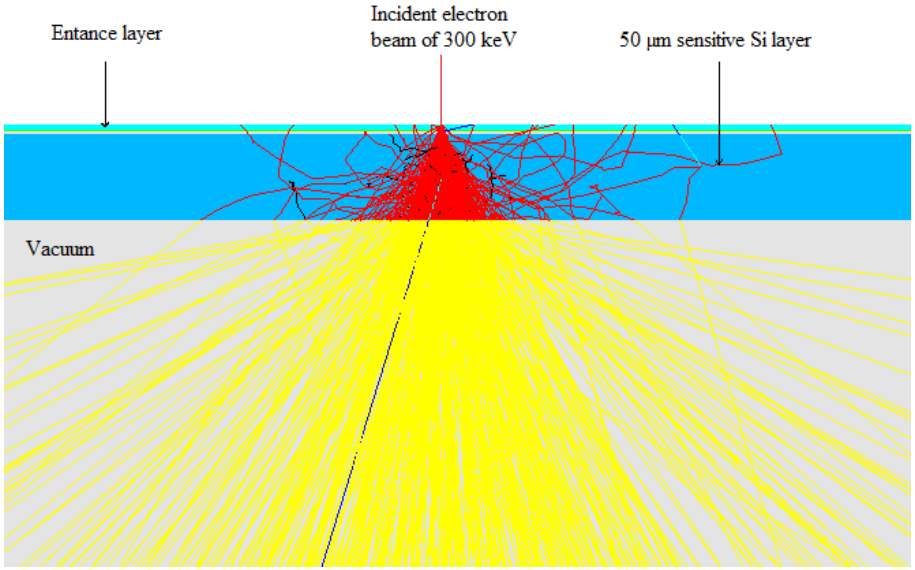
What do we need?

thin detector

50µm thick detector
with 200µm passive Si support structure

50µm thick detector without support structure
beam stop 20mm beneath





works only at very low power consumption for thermal reasons !

DEPFET operation principle

DEPFET integrated amplifier

p-FET on depleted n-bulk

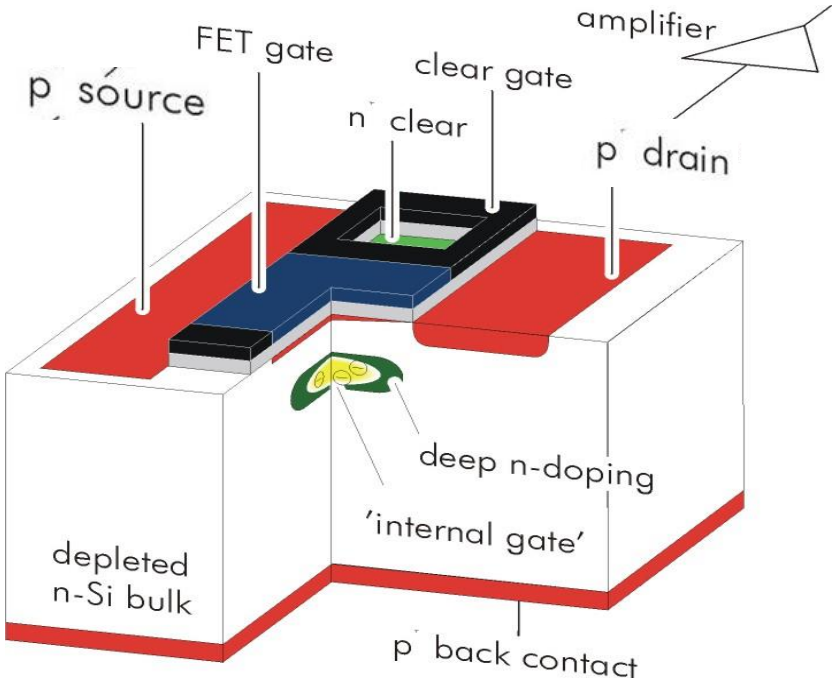
signal charge collected in potential minimum below FET channel

“Internal Gate"

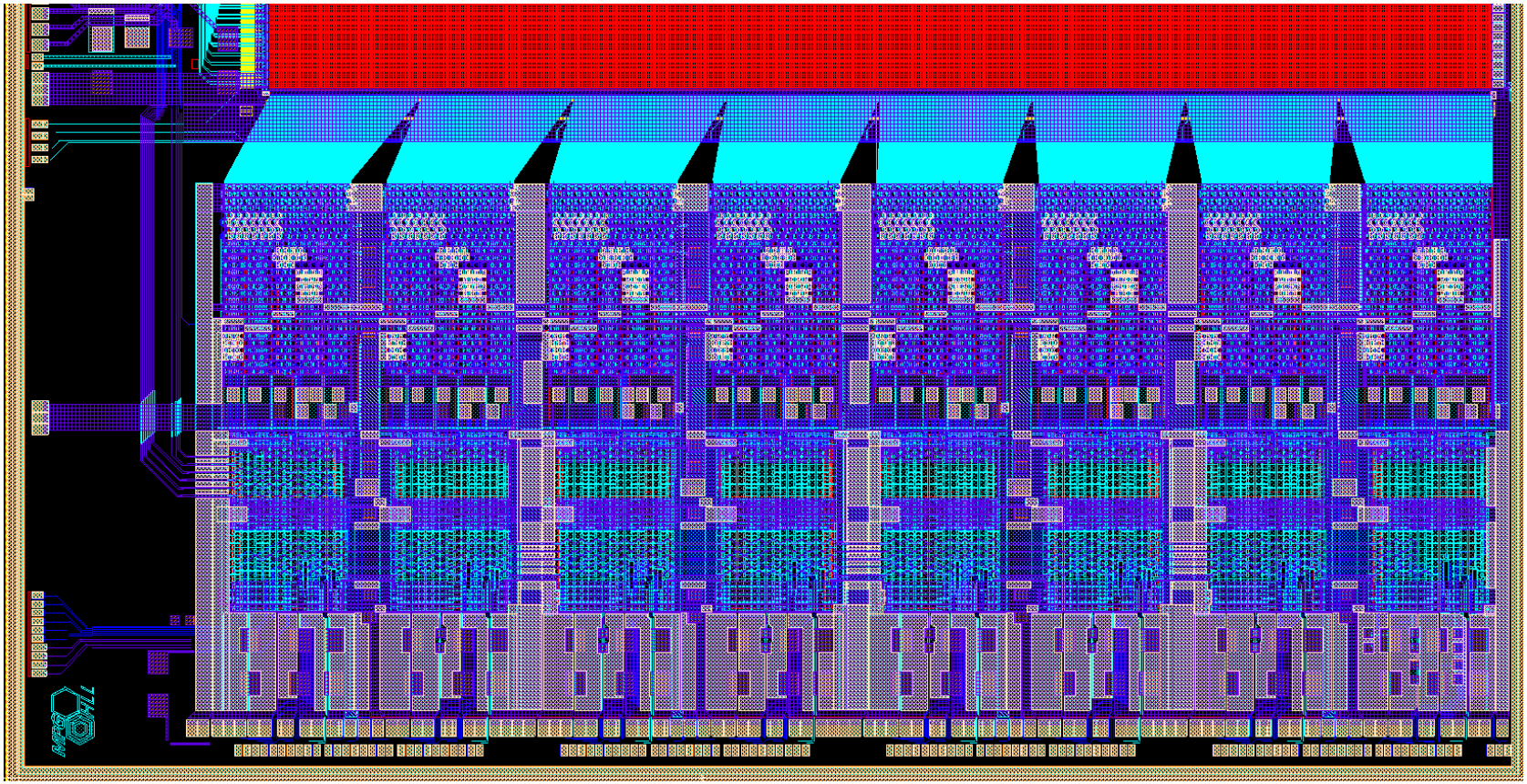
FET current modulation ≥ 300 pA/el.

reset via n-FET (called Clear)
low capacitance & noise

charge storage, readout on demand
(rolling shutter mode)

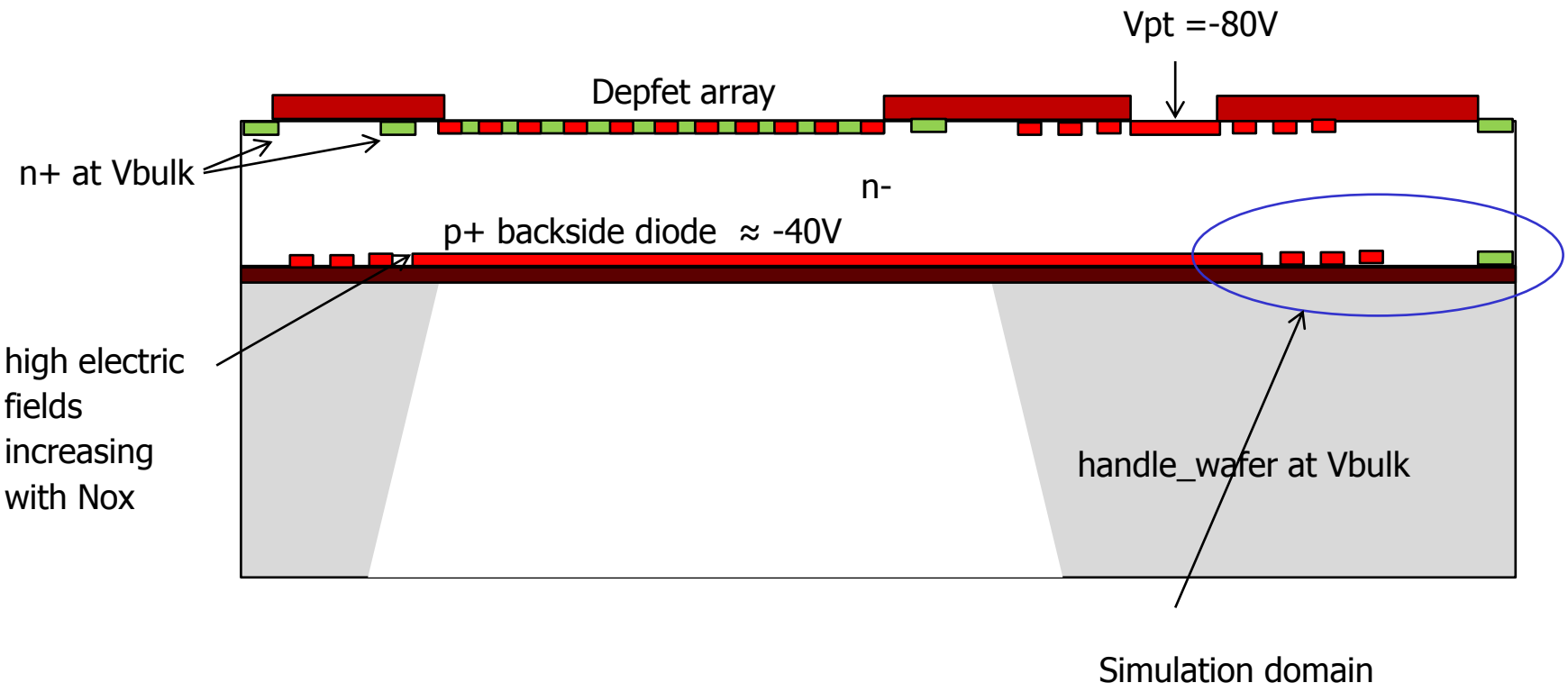


EDET 80k 512 x 512 Module : view on ro-electronics



Similar to Belle2 – lateral Cu lines, vertical Al lines -> power sensing
DHP is replaced by DMC (footprint very similar)
Direct bonding to PCB panel (no copper soldering) – saves space
50um pixel -> 60µm pixel wider matrix - larger gaps inbetween RO chips, better power connection

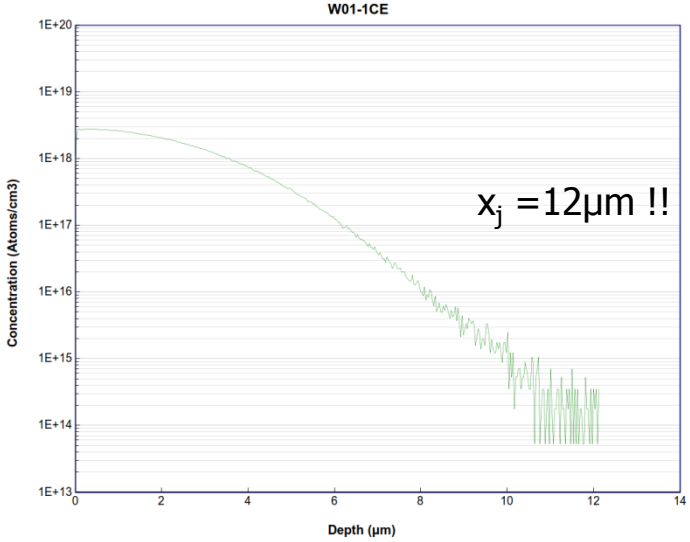
Module cross section



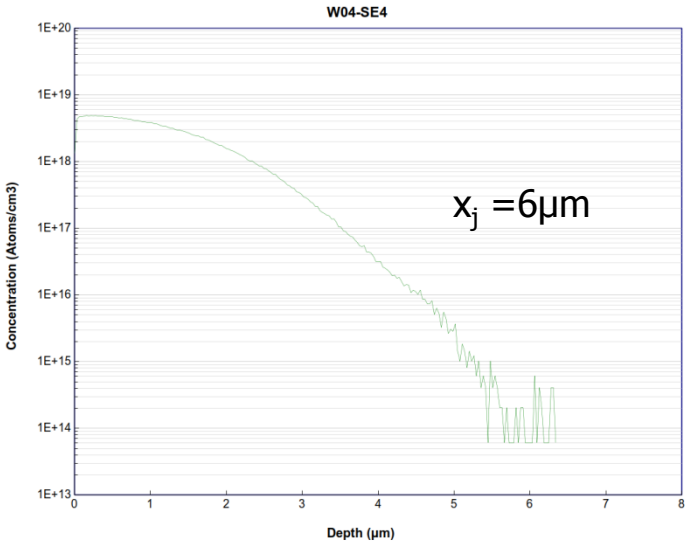
New SIMS measurements – completely different than before

this time from backside surface

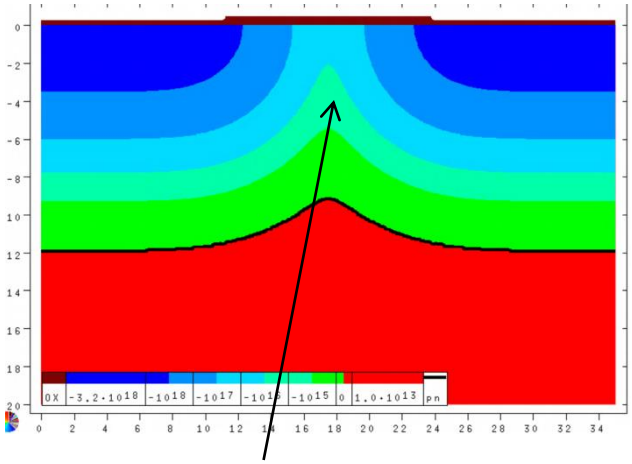
ICEMOS



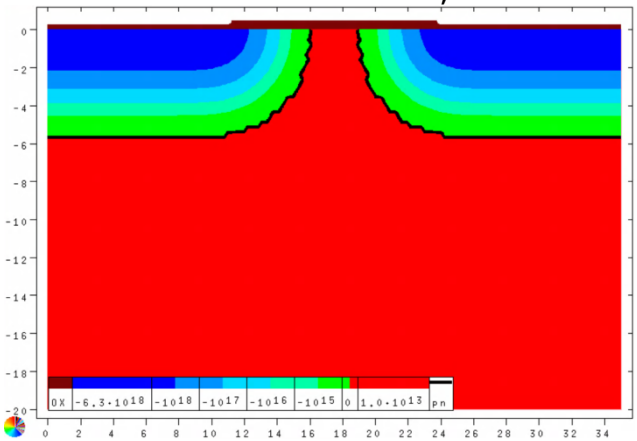
Shinetsu



Simulation: T =1200°C, 360min



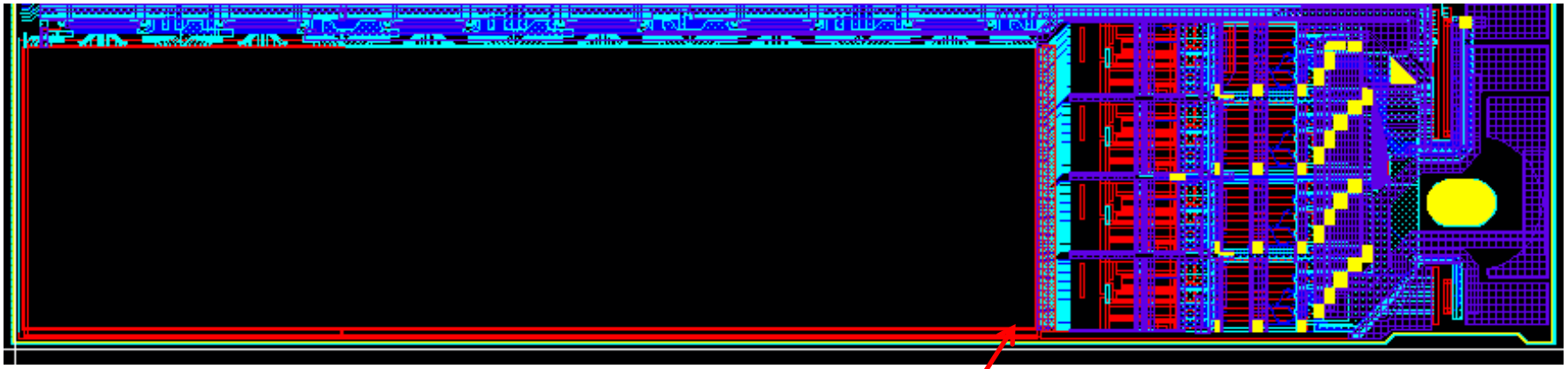
Simulation: T =1100°C, 360min

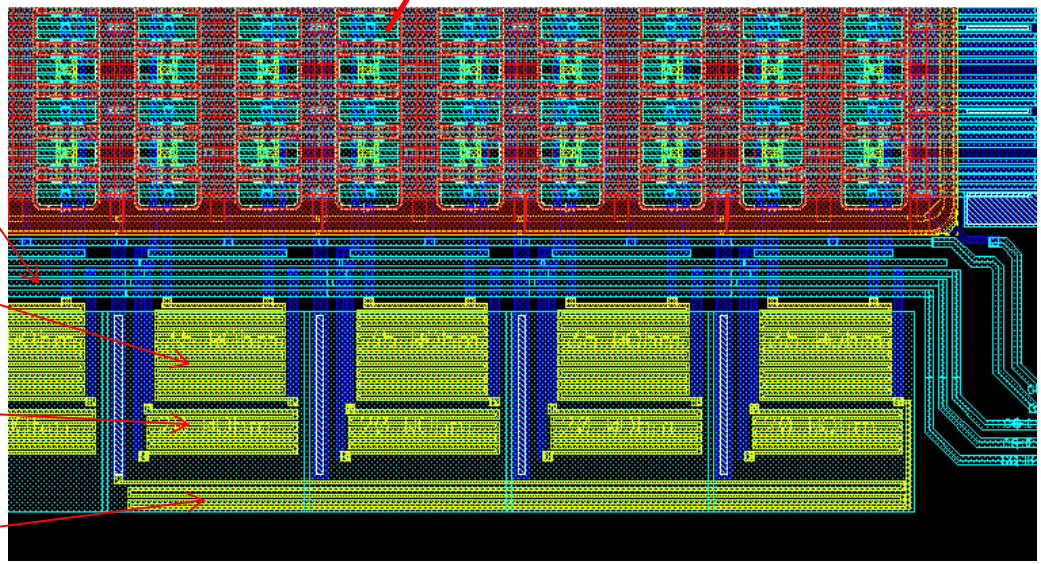


No n-doping, no space charge, no pot. barrier

some n-doping, some charge, weak pot. barrier

Inner forward module (iii)





- Triple clear gate lines
  to cope with inhomogeneous radiation
- Bias resistors for the cap. coupled Clear Gates
- Bus resistors for Clears
- ESD protections resistors for the poly lines Gate and

PowerPoint-Präsentation — Okular

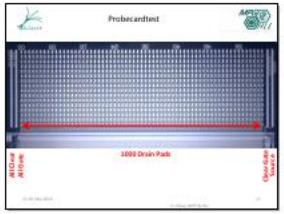
Datei Ansicht Bearbeiten Gehe zu Lesezeichen Extras Einstellungen Hilfe

Durchsuchen | Bereichsauswahl | Gelber Textmarker | 19 von 45 | Verkleinern | Seitenbr

Vorschaubilder

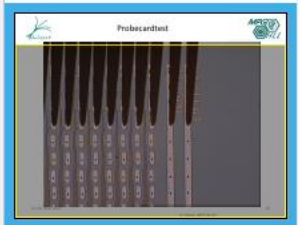
Suchen ...

16

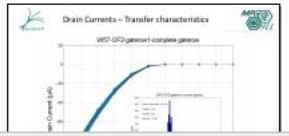


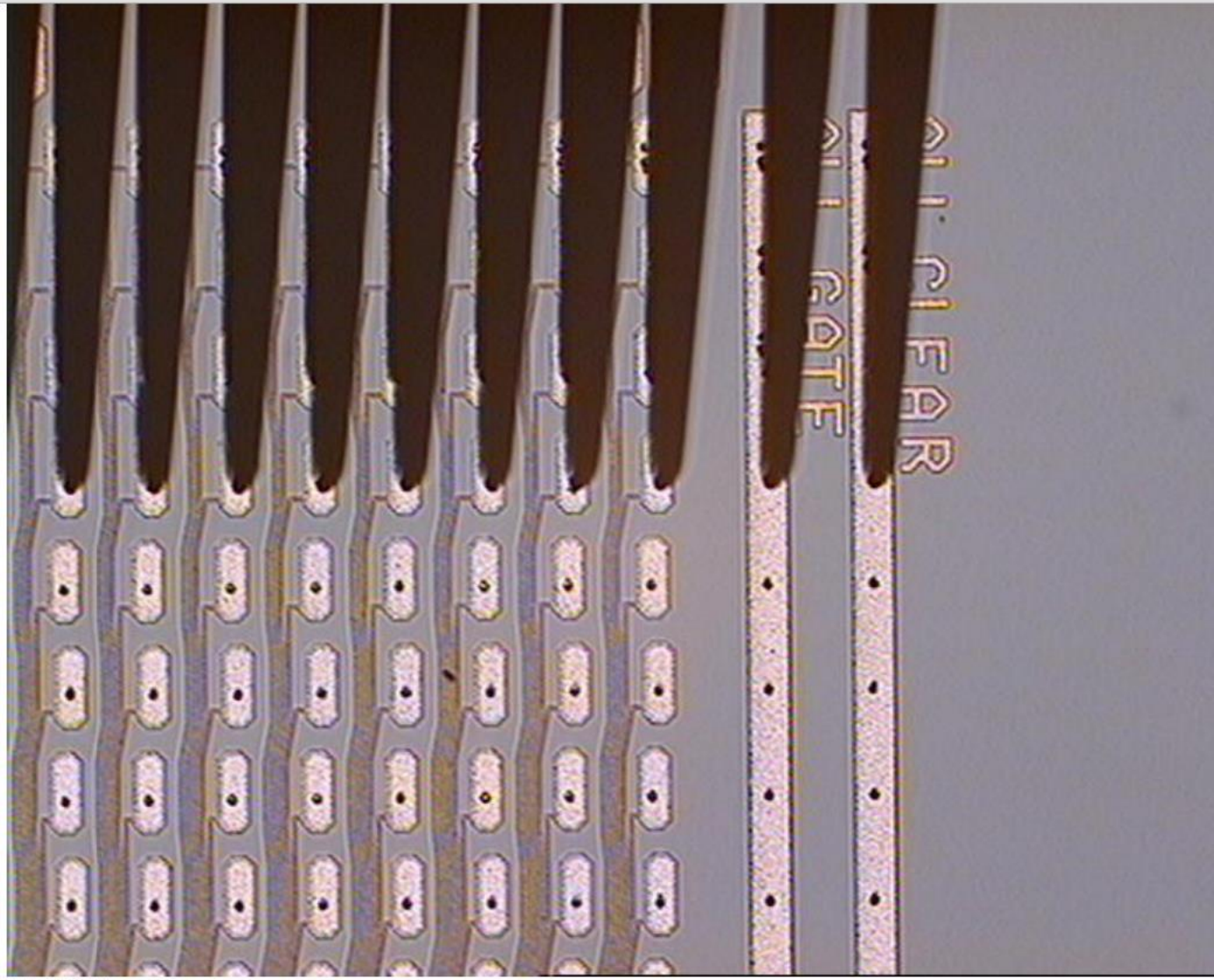
17

18



19





27-29. Mai 2019

D. Klose, MPP & HLL

Simula... Design Mail&Z... Priv System

Wien 2012

We want to see something …

50 (better 100) primary electrons
per pixel provide enough contrast

100 primary e- (300keV, 50µm Si)

-> 800 000 signal electrons
to be stored per pixel

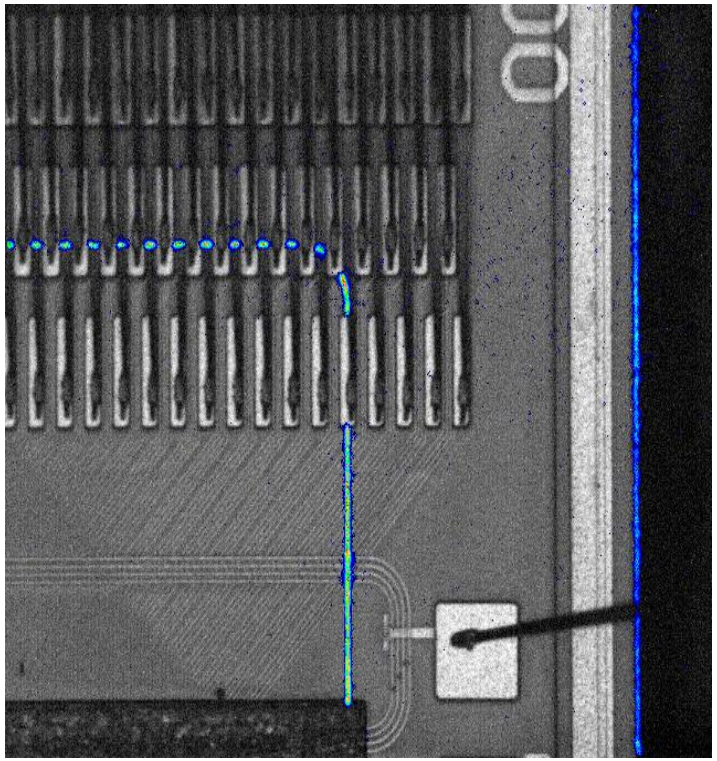
Dynamic range problem !

For example:

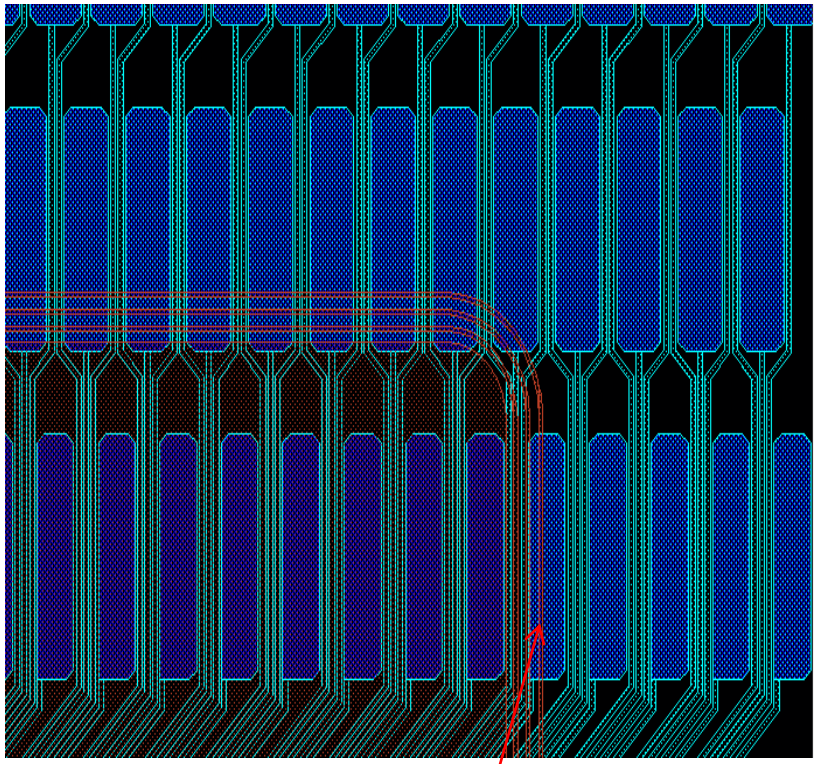
Charge handling capacity of
a Belle2-PXD DEPFET: 50 000 e-

☹

H5.0.29



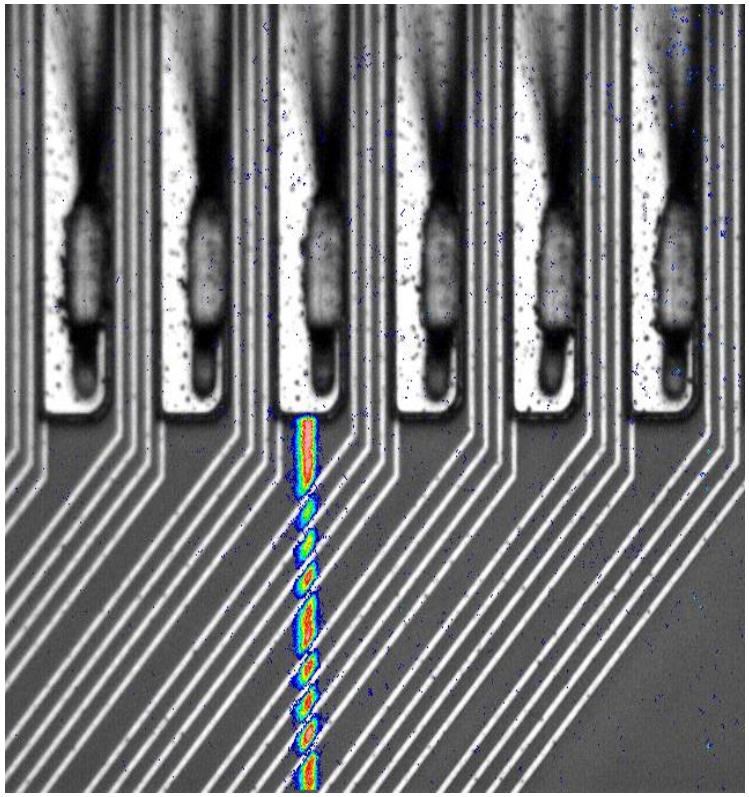
Lens: x5
Camera: InGaAs



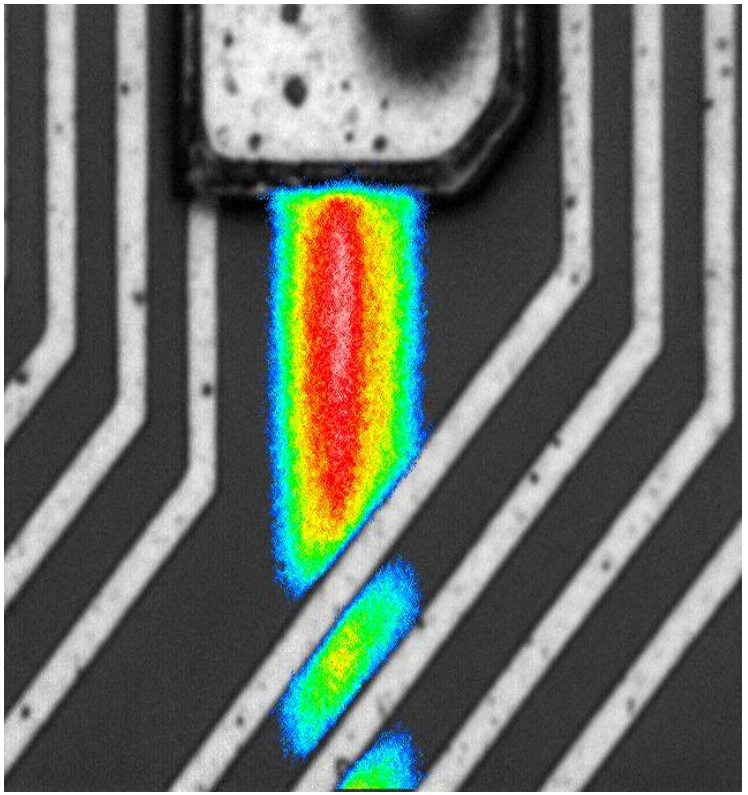
PXD9 layout: poxp & al2n

Break through at **outer most** guard ring!
(against all expectations)

H5.0.29



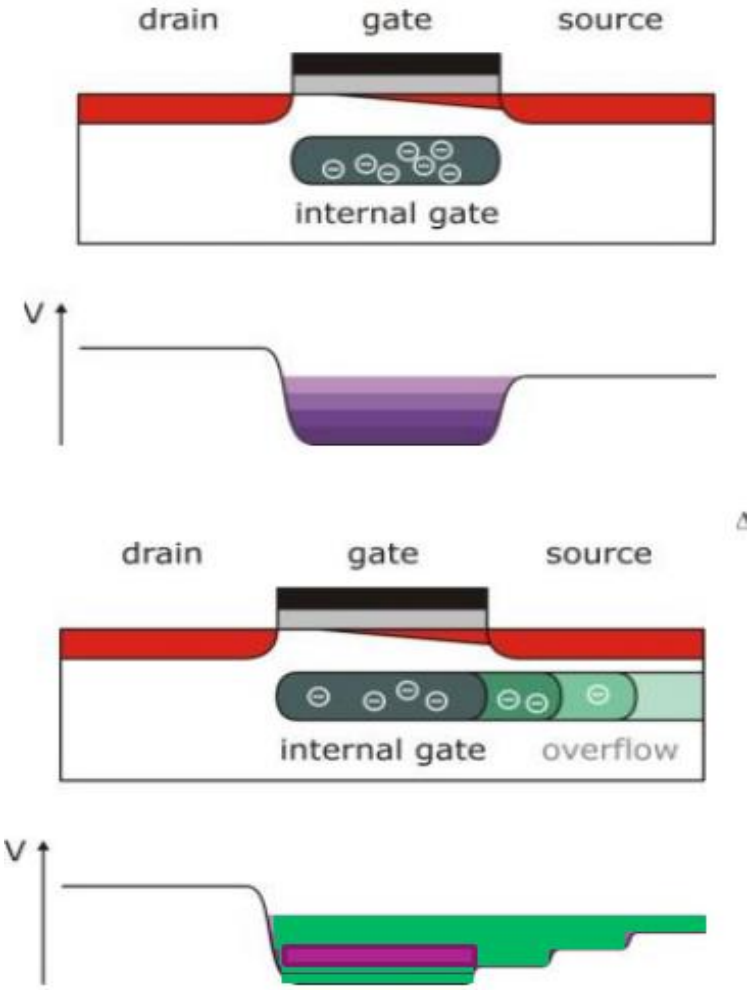
Lens: x20
Camera: InGaAs



Lens: x100
Camera: InGaAs

What happens if the Internal Gate is full?

DEPFET technology offers a simple natural solution



Internal amplification

gq = dI/dQsig

for a given transistor :

gq ~ channel carrier velocity

gq ~ fraction of mirror charge

influenced in the channel by Qsig < 1

Multiple n-implants to create
an electric field towards the Internal Gate
and to tailor the response

With courtesy:
P. Lechner et al DEPFET Active Pixel Sensor with Non-Linear Amplification IEEE NSS, Valencia 2011