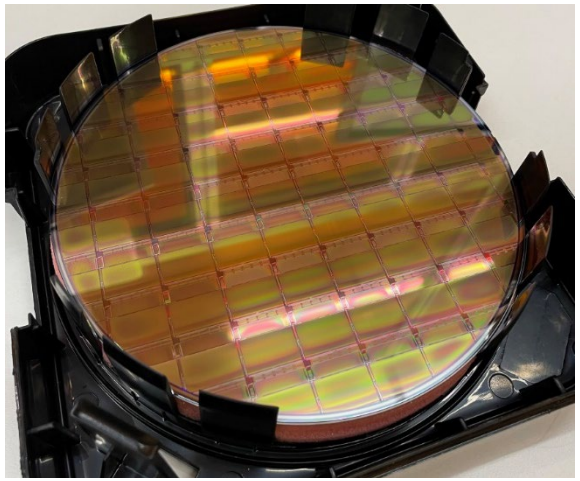
MAX PLANCK
SEMICONDUCTOR
LABORATORY

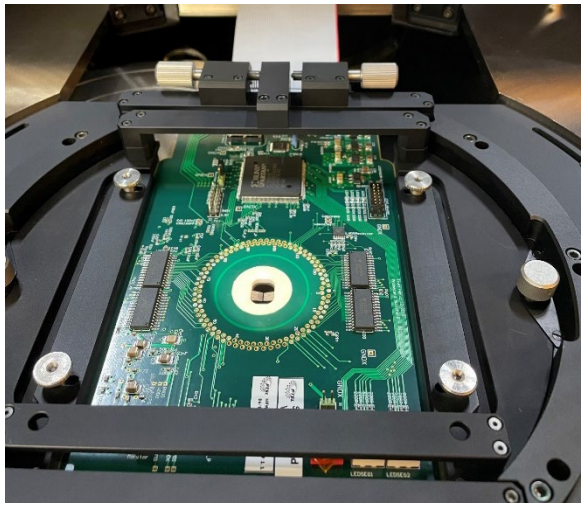
SWITCHER-B 2.3 – PROBE CARD TESTS

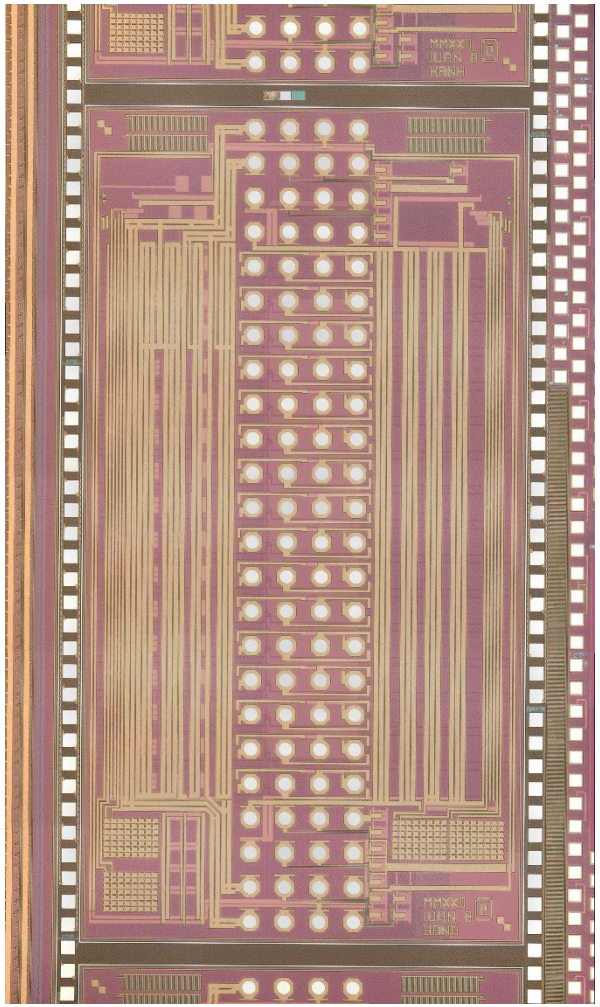
Treis, Koffmane

SWITCHER-B 2.3

- Two 200 mm wafers were received end of 2022
- SwticherB with pads (no bumps yet)
- Dedicated probe card ordered in 2022 for test on pads
- PA200 4inch probe card holder ordered and installed in 2022

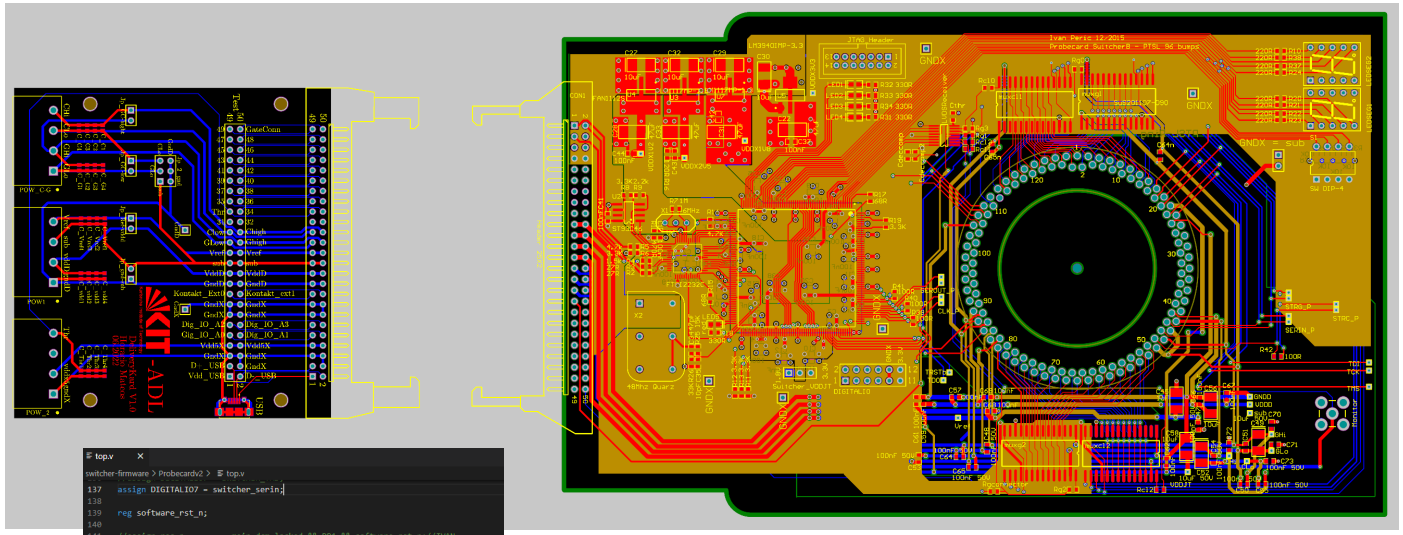




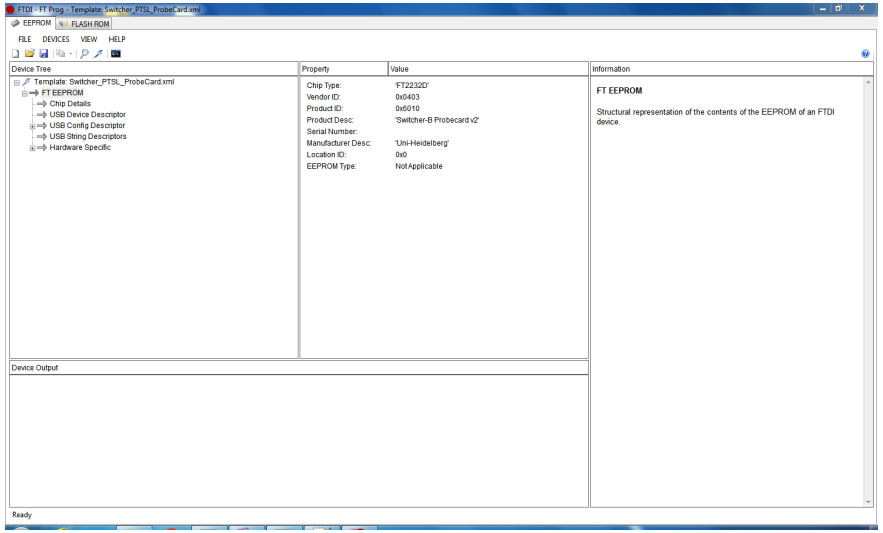


SETUP ISSUES

- Pin header orientation mirrored on delivery card (work around possible)
- short due to solder paste under the micro USB connector
- EEPROM for the configuration of the USB interface not programmed on new probe card (FT2232C default settings don’t fit to probe card)
- res_n assignment commented in Verilog code (all blocks in reset, no USB communication)

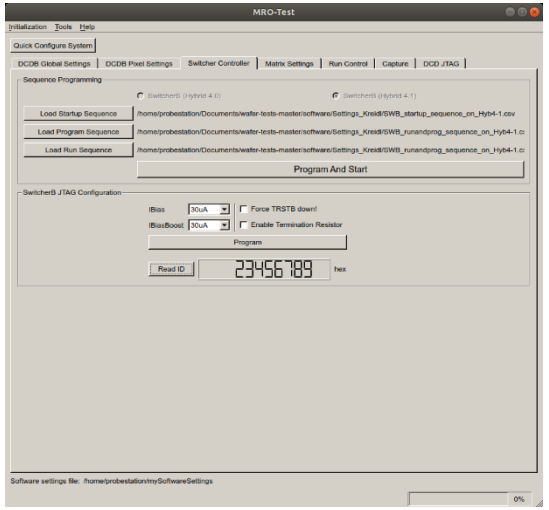


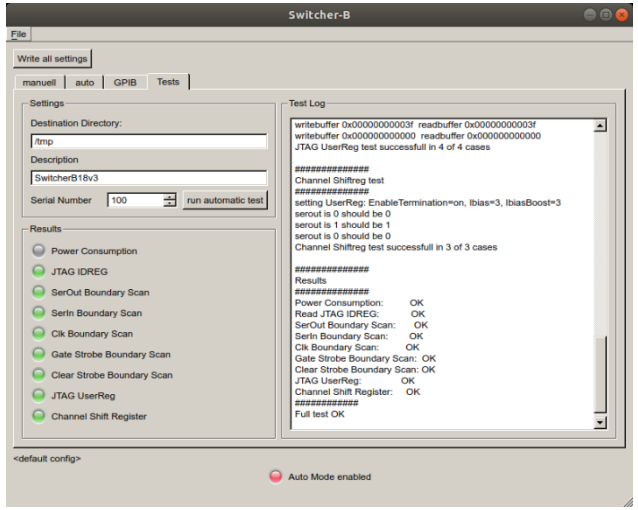
```
assign DIGITALIO7 = switcher_serin;

reg software_rst_n;

//assign res_n        = main_dcm_locked && PB1 && software_rst_n;//IVAN
assign SWITCHER_TRSTB = !SWITCHER_TRST;

main_clk instance_name (
    .CLKIN_IN(CLK48),
    .RST_IN(1'b0),//was pb
    .CLKIN_IBUFG_OUT(/*unused*/),
    .CLK0_OUT(main_clk),
    .LOCKED_OUT(main_dcm_locked)
    );

OBUFDS obufds_switcher_clk_I (
    .I(switcher_clk),
    .O(SWITCHER_CLK_P),
    .OB(SWITCHER_CLK_N)
);

OBUFDS obufds_switcher_serin_I (
    .I(switcher_serin),
    .O(SWITCHER_SERIN_P),
    .OB(SWITCHER_SERIN_N)
);

OBUFDS obufds_switcher_gstr_I (
    .I(switcher_gstr),
    .O(SWITCHER_GSTR_P),
    .OB(SWITCHER_GSTR_N)
);

OBUFDS obufds_switcher_cstr_I (
    .I(switcher_cstr),
    .O(SWITCHER_CSTR_P),
    .OB(SWITCHER_CSTR_N)
);

IBUFDS #(.DIFF_TERM("TRUE")) ibufds_switcher_serout_I (
    .O(switcher_serout),
    .I(SWITCHER_SEROUT_P),
    .IB(SWITCHER_SEROUT_N)
);

//Sub module instantiations

jtag_engine jtag_engine_I(
  //infrastructure
  .clk(main_clk),
  .res_n(res_n),

  //interface to USB: Data to JTAG
  .data_to_jtag_clk(main_clk),
  .data_to_jtag(data_usb2jtag_reg),
  .data_to_jtag_valid(data_valid_usb2jtag_reg),
  .data_to_jtag_almost_full( /* NOT USED */),
```

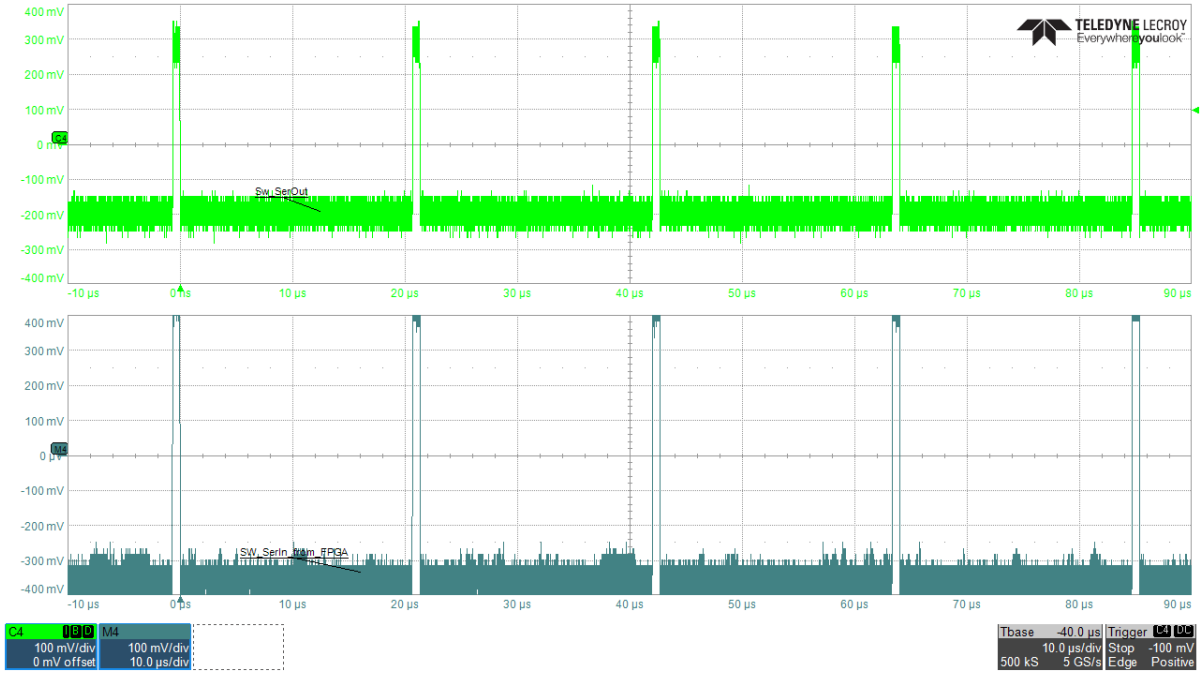


TEST RESULTS

- SW-VDDD 1.8 V, 3 mA
- JTAG chip ID readback okay (0x23456789)
- SW_SerOut okay, probed on pads on probe card
- random channels (gate0/clear0, gate1/clear1, gate28/clear28) probed on pads on probe card with different timings
- skipping gate1 applied in software and checked on the scope (gate0 is extended)
- Sw-Sub connected to GND, GateLow and ClearLow set to 0 V, GateHigh = 5V, ClearHigh = 7V







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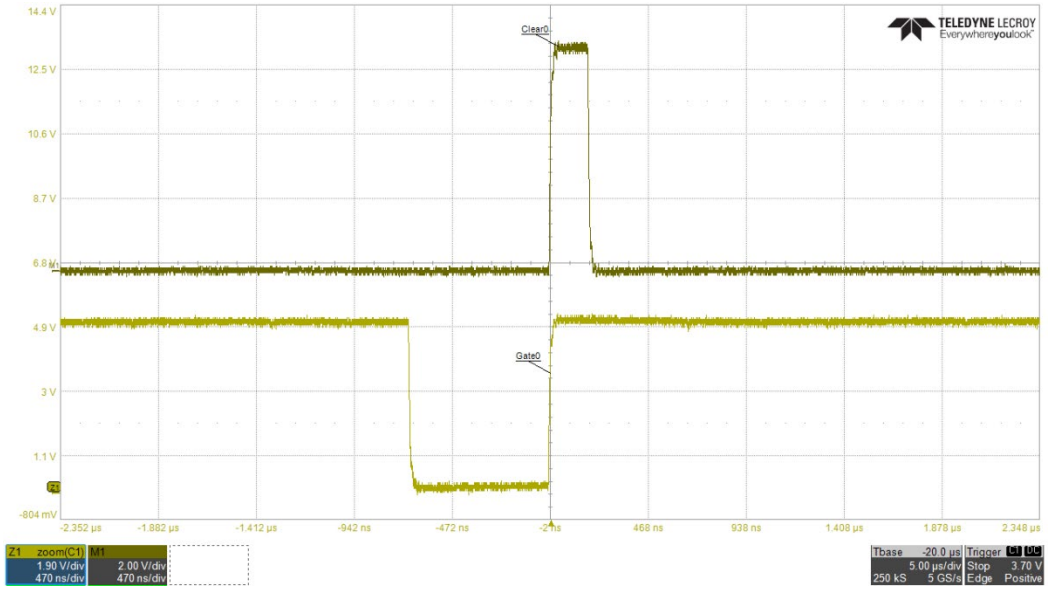
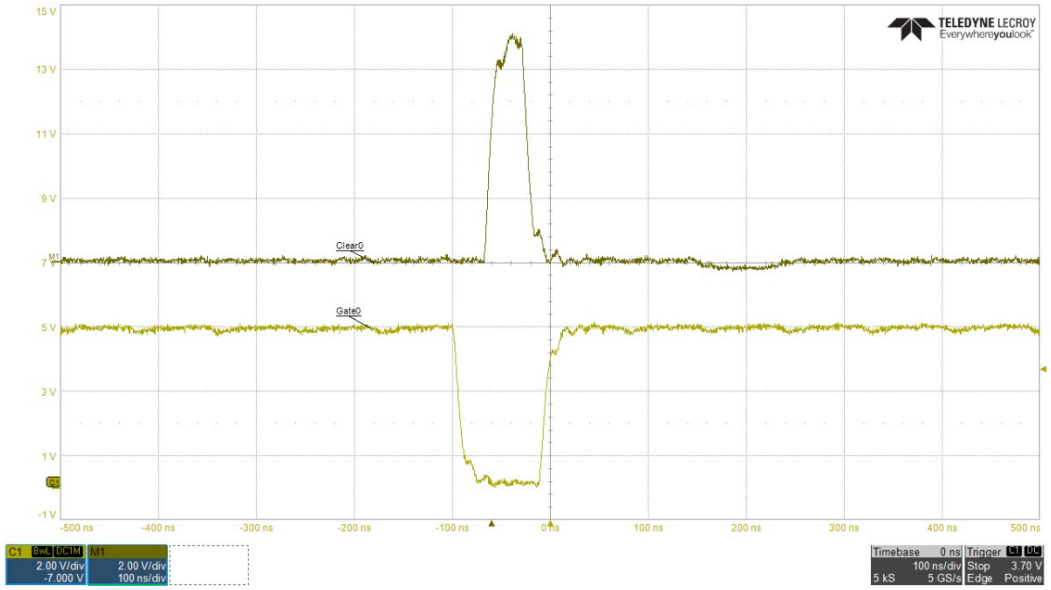
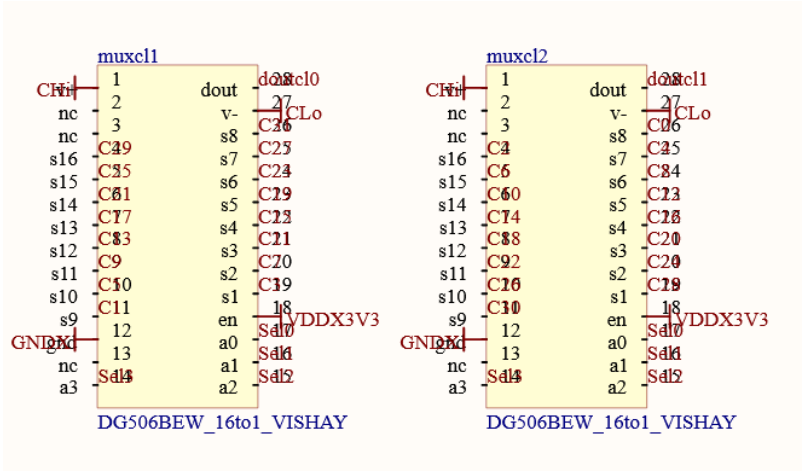




OPEN TOPICS

- Test with application like Sw-Sub, GateLo and ClearLo voltages
- Re-work probe card for bumped SwitcherB (needles not in a good shape)



SCHEMATIC DIAGRAM Typical Channel