Investigation of Device Damage Due to Electrical Testing

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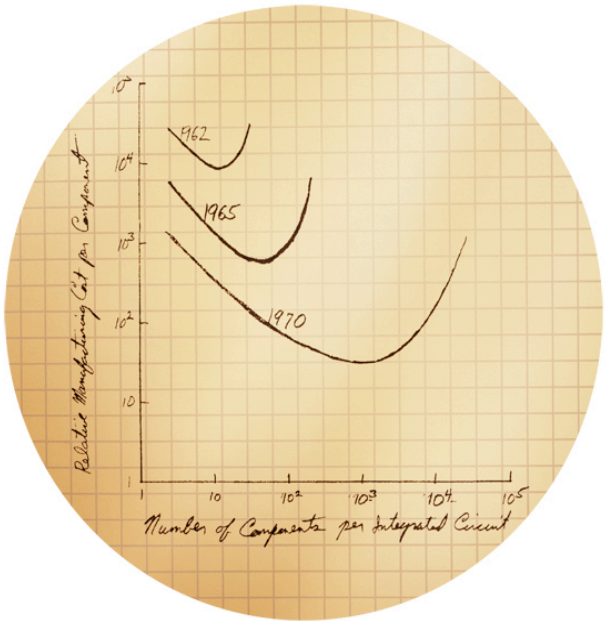
Abstract

This paper examines the potential failure mechanisms that can damage modern low-voltage CMOS devices and their relationship to electrical testing. Failure mechanisms such as electrostatic discharge (ESD), CMOS latch-up, and transistor gate oxide degradation can occur as a result of electrical over-voltage stress (EOS). In this paper, EOS due to electrical testing is examined and an experiment is conducted using pulsed voltage waveforms corresponding to conditions encountered during in-circuit electrical testing. Experimental results indicate a correlation between amplitude and duration of the pulse waveform and device degradation due to one or more of the failure mechanisms.

I. Introduction - Technology Trends

CMOS geometries have been scaling down with time, approximately as Moore's law has predicted as early as 1965 (see Figure 1).



"With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip." **Gordon E. Moore** April 19th 1965

Figure 1. Original Moore's law Diagram (Source: Intel Corporation).

CMOS device power, speed, density and size have continued to improve with each successively scaled generation of silicon. In the "constant field" scaling approach [1], decreased transistor feature size is accompanied by both a reduction in the gate oxide thickness and (as shown in Figure 2) a reduction in supply voltage for both the integrated circuit core and input/output (I/O) circuitry.

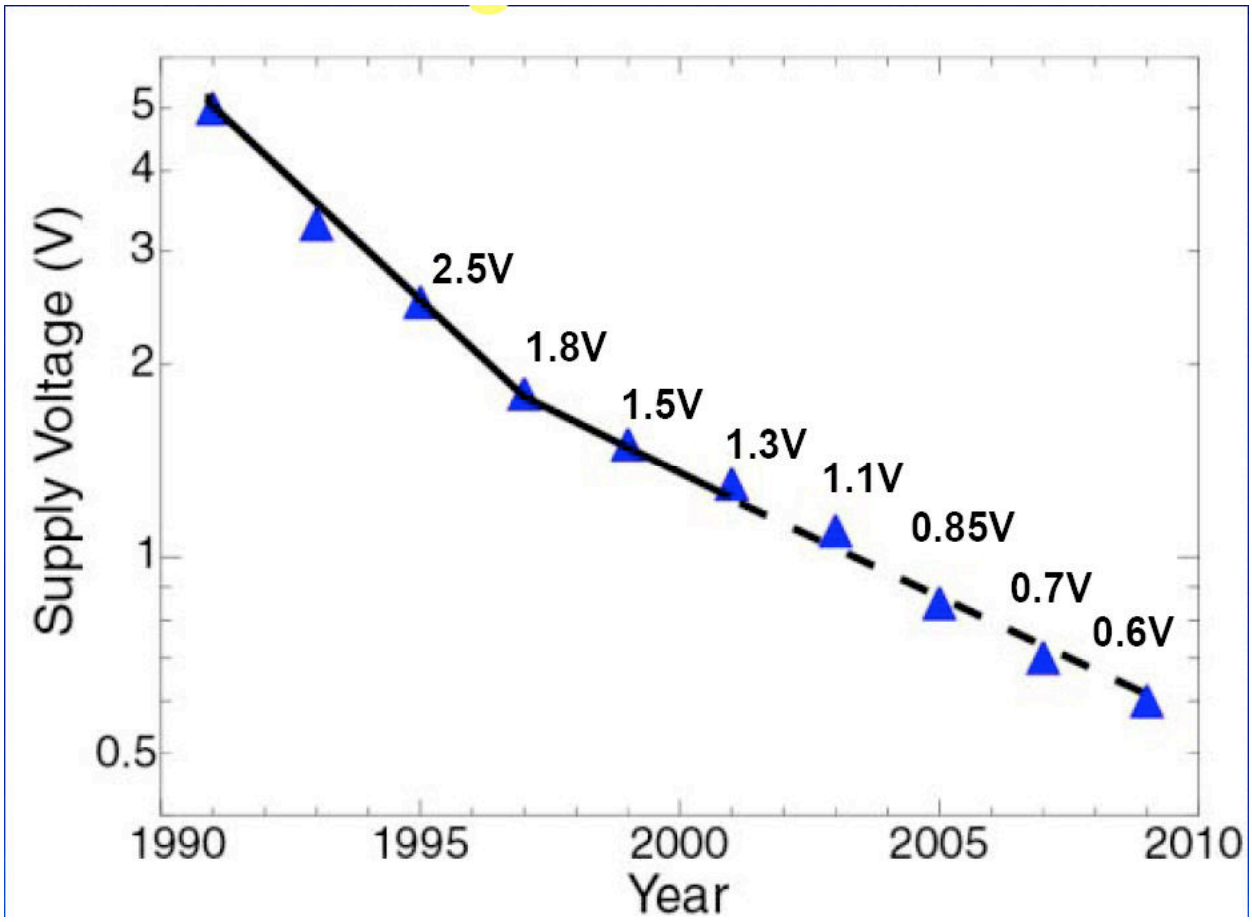


Figure 2. Supply Voltages from 1990 to 2010 (Source: Intel Corporation).

The advantages of CMOS scaling are power reduction and increased speed, with the tradeoff of potentially increased susceptibility to damage of the thin gate oxide due to EOS conditions. Although circuit techniques are available for protecting devices from events such as ESD and EOS, the robustness of these I/O protection circuits tend to decrease in the face of increasing speed requirements and the need for reduced power consumption [2, 3].

In addition to the threat of damage to an integrated circuit during normal handling and operation, electrical testing can produce voltage and current conditions exceeding those expected during normal low-voltage operation. The voltage and current conditions experienced during electrical test were not a problem for early generations of CMOS devices with large geometries and thick oxides. However, as CMOS geometries have scaled to submicron dimensions, these conditions in testing can potentially cause immediate device failures, or (more insidiously) performance degradation and early life failure after apparently passing electrical test. The purpose of this paper is to present experimentally measured data showing that voltage and current conditions experienced during electrical test can damage submicron CMOS devices, and that this damage can be understood and predicted given existing models for CMOS device degradation.

This paper is organized as follows: Section II describes device failure mechanisms that can be activated by the voltage and current conditions associated with electrical test. Section III describes testing methods and the technology issues that can cause over-voltage and over-current conditions. Sections IV and V describe experiments showing that measured failure and degradation rates are consistent with known device failure mechanisms. Conclusions are presented in Section VI.

II. Potential Device Failure Mechanisms

A. ESD Diode Damage

Designing ESD devices to protect small geometry, low-voltage CMOS circuits is becoming an increasingly difficult challenge. Oxide breakdown voltages decrease with thinner oxide technologies and approach the ESD snapback voltage, making it difficult for manufacturers to guarantee adequate protection during an ESD event [2, 3]. More robust, larger ESD devices have high capacitances that cannot be tolerated at faster signal speeds. The tradeoffs between speed and reliability make these circuits more difficult to protect from EOS occurring at final electrical test.

ESD protection devices are designed to withstand very large currents for a very brief period of time. As an example, a device that can tolerate a 2kV human body model (HBM) ESD event must be capable of carrying 1.3A with a rise time of 10ns and a decay time (to 30% of the peak voltage) of 150ns [4]. However, these same devices typically cannot carry more than about 100mA for durations greater than several milliseconds. Depending on the circuit design, ESD diode stress damage can occur if subjected to currents exceeding the manufacturer's maximum specification for durations that typically occur during electrical test. Since a damaged device may continue to function well enough for the entire IC to pass digital tests, electrical tests performed in the factory and field may not be able to detect the compromised ESD functionality. A partially damaged device can continue to deteriorate over time, making downstream components and the entire electrical system vulnerable to further ESD damage [5]. This would be an especially significant concern for hand held systems and other units with connections to peripherals and the exterior environment.

B. CMOS Latchup Damage

CMOS latchup, which can be initiated by a transient over-voltage condition, can cause an over-current condition resulting in catastrophic damage. This well-understood phenomenon [6] occurs when the pins of a device are driven to voltage levels that exceed $V_{DD} + V_{be}$ or fall below $V_{SS} - V_{be}$. Under these conditions, it is possible to turn on the parasitic bipolar transistors Q_{npn} and Q_{pnp} as shown in Figure 3. Large currents I_{npn} and I_{pnp} flow and form a low-impedance path across the supply terminals. Thermal damage often occurs due to these large resulting currents, causing bond wires and the entire die to heat up. If temperatures exceed 200ºC, damage to bond wires can occur. Although occurrences of CMOS latchup were more common in the early 1980s with 12V CMOS technologies, the high currents associated with latchup phenomena are still a potential damage mechanism in submicron CMOS technologies.

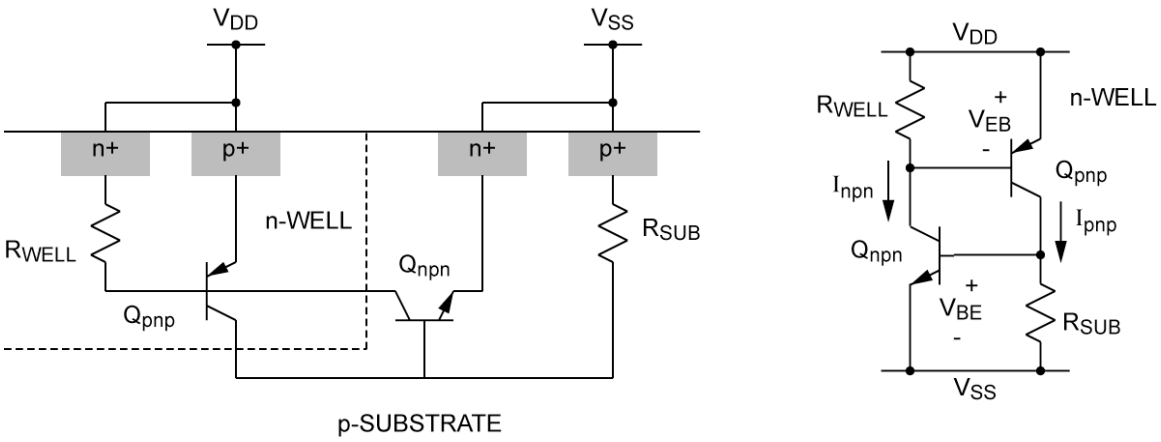


Figure 3. Parasitic bipolars in CMOS technology.

C. Time Dependent Dielectric Breakdown – TDDB

Over-voltage stress can also cause damage to the thinner gate oxide of a lower voltage device through a mechanism called Time Dependent Dielectric Breakdown (TDDB) [7]. TDDB begins with an over-voltage condition that can either be large in amplitude and small in duration, or small in amplitude and large in duration. Over-voltage conditions can generate hot carriers that are accelerated to velocities high enough to enter the gate oxide layer and generate electron-hole pairs. These electron-hole pairs generate a trapped charge in the dielectric layer of a transistor. Over time these traps attract other trap sites, accumulate and eventually form a silicon filament that results in a short from the gate to channel [7]. TDDB failures are especially troublesome because they can be latent in nature and undetectable during factory and field electrical test.

Two different models have been proposed to predict gate oxide reliability as a function of electric field E. For high values of the electric field E, an anode hole injection, or "1/E" model is used; for low fields, a thermochemical, or "E" model is more appropriate [7]. At high fields, the 1/E model shows better agreement with experimental data because of significant electron tunneling due to the Fowler-Nordheim (FN) effect [7, 8, 9, 10], and hole generation dominates over the thermochemical effects.

According to the 1/E model [10], the mean time to breakdown t_{BD} is given by

$$t_{BD} = C_1 \exp(C_2 / E_{ox}) \qquad (1)$$

where parameters C_1 and C_2 in (1) are defined [10] as follows:

Parameter		Value	Units
C_1	Time parameter; technology dependent	5.6E-13	[sec]
C_2	Field acceleration parameter	4.3E+08	[V/cm]

Note that, as indicated in [10] parameter C_1 is technology dependent. In [10] this value was determined from a best fit of the model to experimental measurements; in Section V of this paper the 1/E model is applied in a different technology and a slightly different value of C_1 resulted from the best fit to the measured data. In Equation (1), E_{ox} is the electric field in the oxide, which is given by

$$E_{ox} = \frac{V_{ox}}{T_{ox}} \tag{2}$$

where quantities V_{ox} and T_{ox} in (2) are defined [10] as follows:

Quantity		Units
V_{ox}	Voltage drop across gate oxide resulting from applied voltage	[V]
T_{ox}	Gate oxide thickness	[cm]

Figure 4 shows a plot of (1) using the parameters from [10] for oxide thicknesses of T_{ox} = 1.2nm, 1.5nm, 2nm, and 3.25nm.

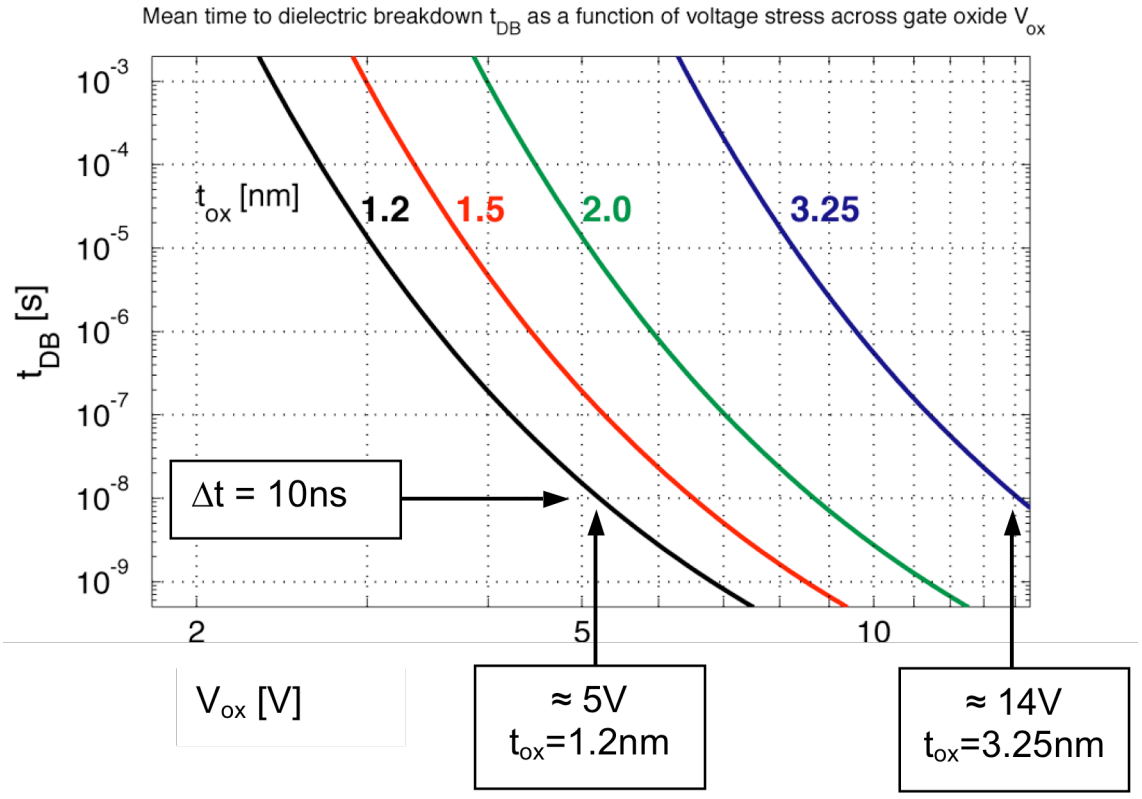


Figure 4

As an example of interpreting Figure 4, consider an applied voltage transient with a pulse duration of Δt = 10ns. What pulse amplitude would have this Δt as the mean time to

breakdown? On the 3.25nm characteristic, the applied voltage across the gate oxide V_{ox} for this condition is 14V, meaning that a 14V transient with a duration of 10ns has a significant probability of damaging a T_{ox} = 3.25nm device. Looking at future silicon generations, the situation is even worse for a T_{ox} = 1.2nm device; a transient amplitude of only 5V with a duration of 10ns has a higher probability of damaging the gate oxide.

III. Electrical Testing Issues

A. Tester Technology

The majority of in-circuit and functional testers used in manufacturing today were designed for 5V logic. As the industry moved to 3.3V logic, this was generally not a problem since 3.3V devices were designed to operate in the 5V logic region with some degree of resiliency. However, with the advent of JEDEC 8-14 Wide Volt Logic, the signal swing for new logic families extends down to 0.8V. This is problematic because test systems designed for 5V logic, which did not need 0.8V levels of accuracy, can generate signals that exceed the upper and lower thresholds.

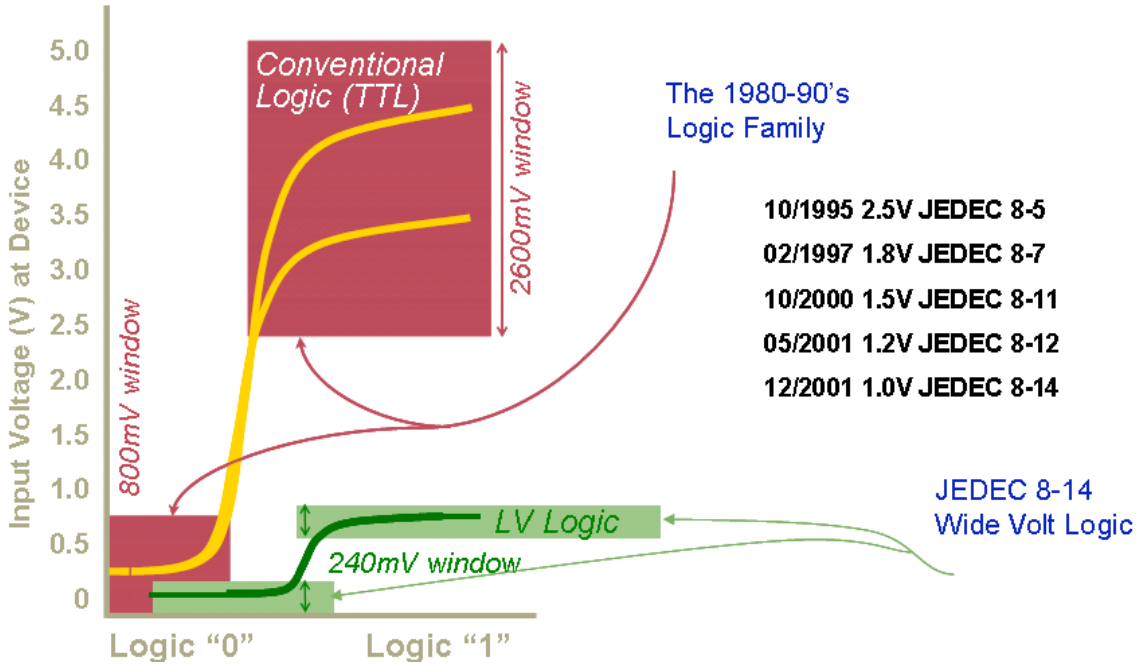


Figure 5. Logic Families

Figure 5 illustrates that there is a substantial difference between conventional logic high and low voltage windows (2.6V and 0.8V) and ultralow voltage logic levels (240mV). New 0.8V logic requires a factor of 10× improvement in accuracy over that required for 5V logic, and many conventional test systems were simply not designed to achieve such voltage accuracies.

B. In-circuit Testers and Backdriving

In circuit testers (ICT) are commonly used to perform electrical tests on digital integrated circuits assembled on Printed Circuit Boards (PCBs) [11]. ICTs often employ custom test fixtures that provide access to nearly every net on the PCB under test. Individual testing of each component is achieved using Driver/Sensor (D/S) pins capable of forcing inputs to certain logic states and sensing the resulting outputs. The drivers are voltage sources that force DUT inputs to the logic levels required for each test. It is common for the driver to force an output connected to the DUT input to an opposite state. This is called "backdriving" which can produce currents of several hundred milliamps. Studies have shown that improper backdriving can cause reliability and accuracy issues [12].

C. Over-voltage Transients

An over-voltage transient is another form of stress that can occur due to improper backdriving during electrical test. Transients can occur when there is inadequate digital isolation during testing, or when an output either changes state or is unintentionally tri-stated while being backdriven. The resulting change in current can cause voltage spikes due to energy stored in the inductive path from the digital pin driver to the DUT.

The situation is illustrated with the example of Figure 6, in which U3 is the DUT and its input at node C is forced by pin driver DRIVER2. To ensure that DRIVER2 sees a constant load, U3 can be isolated by preventing the output of U2 from changing states during the test. Isolation is accomplished by using DRIVER1 to force node B high. U1, however, is not controlled and therefore DRIVER1 does not see a constant load. The amount of current i_1 required from DRIVER1 to maintain the desired state at node B depends on the logic level at node A. If node A is high, U1 tries to drive node B low, and to maintain node B high DRIVER1 must supply a substantial backdrive current $i_1=i_{BD}$, which can be of order 50mA to 500mA. On the other hand, if node A is low, then U1 drives node B high, little or no current is required from DRIVER1, and $i_1 \approx 0$.

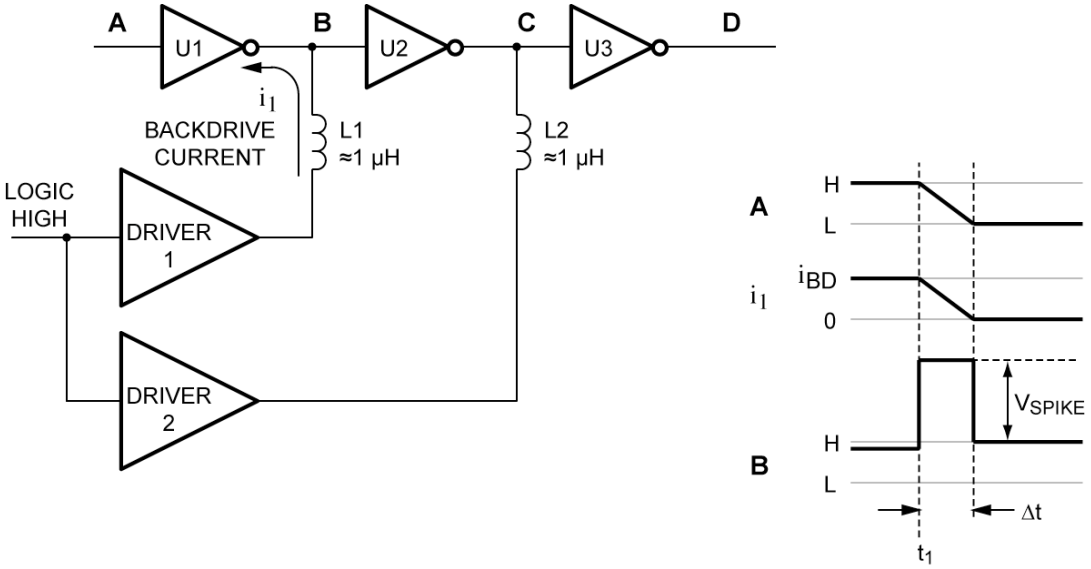


Figure 6. Example of a backdriven circuit.

The difficulty occurs if node A changes state due to on board activity during the test. For example, as shown in the timing diagram in Figure 6, suppose that at time t_1 node A transitions from high to low. The required backdrive current changes from its maximum value i_{BD} to zero over a short time scale Δt, which is within the specified transition time of this logic family. Given the sudden change in current and the inductive path from DRIVER1 to node B, there will be a voltage spike at node B, which can cause damage to devices connected to the uncontrolled node.

Typical values of L for a test path are on the order of 1µH to 10µH, depending on the PCB layout. For example, a backdrive current of 100mA and a Δt of 10ns with a path inductance of L = 1µH can cause a voltage transient of

$$v_L = L\frac{di_L}{dt} \Rightarrow V_{SPIKE} = 1\mu H\left(\frac{100mA}{10ns}\right) = 10V$$

For faster logic families, the situation worsens because the transition times Δt are lower and the lower output impedance of the gate requires higher backdrive current.

These are typical and unavoidable events on conventional ICT's unless special precautions are taken to ensure multiple levels of digital isolation and proper sequencing of the D/S isolation pins [12]. Figure 7 is an oscilloscope photo showing the measured node voltage during a backdrive transition event. The transient over-voltage condition shown in Figure 7 resulted from backdriving a 74LVT240A 3.3V DUT, then tri-stating the device. The transient condition was observed at the device output node.

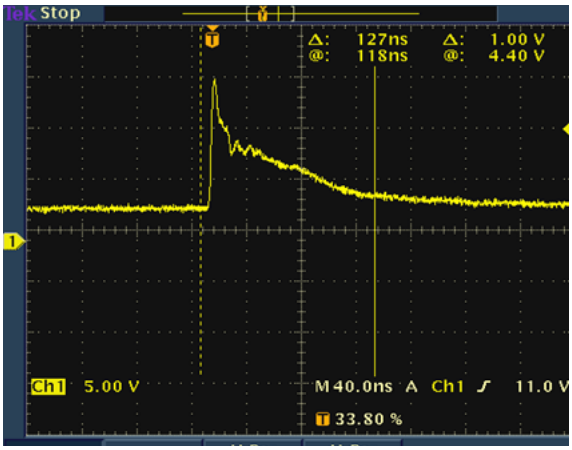


Figure 7. Typical voltage spike found on conventional ICT's.

In addition to the dangers of voltage transients, large backdrive currents also pose a threat. A 1990 study [13] concluded that thermal breakdown of bond wire was one of the major risks in using high-current backdrive in electrical test.

D. Driver Accuracy

Voltage accuracy at the DUT can be affected by backdrive current, particularly on ICTs that use high-impedance drivers [12]. Voltage errors occur due to IR impedance drops across driver output nodes along the signal path. Users of these testers can compensate for voltage errors by programming higher voltage levels in order to meet the logic level requirements for the backdriven DUT. However, this action will only work if the loading remains constant or if the system can dynamically measure current variations due to a changed part or missing device. Otherwise an over-voltage condition is possible.

IV. EXPERIMENT DESIGNED TO INVESTIGATE FAILURE MECHANISM MODELS

A. Device Selection and Specification

To quantify IC stress and damage due to various over-voltage test conditions, an experiment was conducted with a representative low-voltage device. The Texas Instruments SN74AUC16240 is a 16-bit buffer/driver (interface chip) with 3-state outputs. It is optimized for 1.8V operation and is sub-1V operable. This device is 3.6V tolerant to support mixed-mode digital operation [14]. Its latch-up performance exceeds 100mA per JESD 78, Class II, with ESD protection exceeding JESD 22. This is a very robust device, commonly used in low-voltage designs and evaluated by in-circuit or edge connector functional testers.

B. Test Circuit

Catastrophic device failures are relatively easy to detect using functional or in-circuit test. However, performance degradation of a device can be more difficult to determine. Measuring the gate oxide leakage current is a common method for detecting performance degradation [10]. Whereas a significant change in gate leakage current indicates a catastrophic failure, a permanent small change in the gate leakage current (by as little as 10% of its original value) indicates that stress induced leakage current (SILC) damage has occurred in the gate oxide, which can affect performance and reliability.

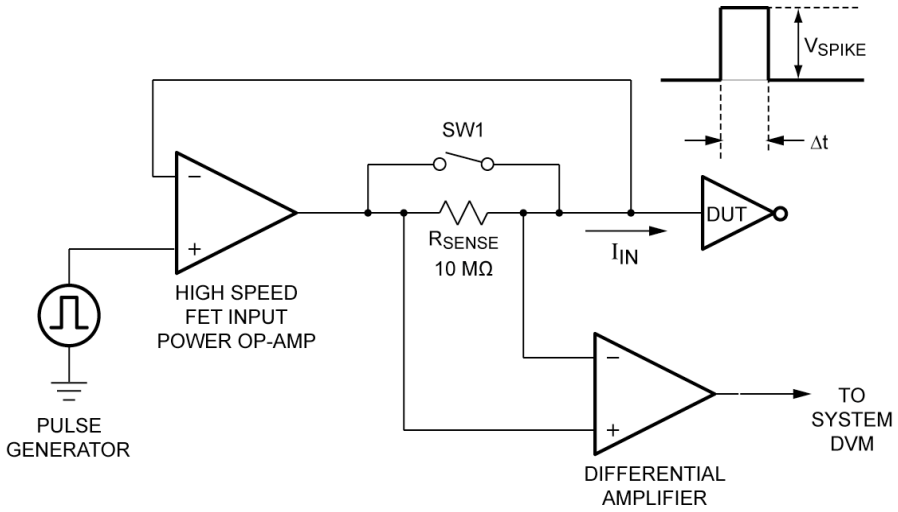


Figure 8. Equivalent Circuit of Test Arrangement

The test circuit for applying stress and measuring SILC is shown in Figure 8. To measure the input current I_{IN}, switch SW1 is opened so I_{IN} flows through the sense resistor R_{SENSE}. The resulting voltage drop across R_{SENSE} is amplified by a differential amplifier and measured by a system DVM. Since the value of R_{SENSE} and the amplifier gain are known, the current I_{IN} can be determined from the DVM voltage measurement. During current measurement, the pulse generator voltage is held constant at a valid logic level so that the DUT input is not stressed. Note that feedback for the driver op-amp is taken from the DUT input, such that any voltage drop across R_{SENSE} will not degrade accuracy in driving the DUT input voltage.

To stress the DUT input, switch SW1 is closed so that a high-speed pulse waveform can be applied directly to the DUT input. A stressing voltage was applied in pulse form to simulate the over-voltage condition shown in Figure 7. A programmable generator provided a pulse with controlled amplitude V_{SPIKE} and duration Δt.

C. Test Procedure

Each DUT was mounted in the circuit test fixture with power applied and inputs and outputs connected to a digital stimulus per manufacturer's specifications. A flowchart of the test procedure is shown in Figure 9. Nominal pulse widths were chosen over a range of 5µs to 134µs, as shown in Table 1. A voltage source was applied to one of the DUT inputs such that a programmable, repeatable test voltage could be applied for a controlled amount of time, to produce finite voltage pulses. The input current was measured in high state and the results recorded. After each pulse, the input current was measured and checked against the original current. If an increase of 10% or greater was observed, this was an indication of SILC and the device was tagged as failed. If the increase was less than 10%, the voltage amplitude was increased by 0.1V and another pulse applied.

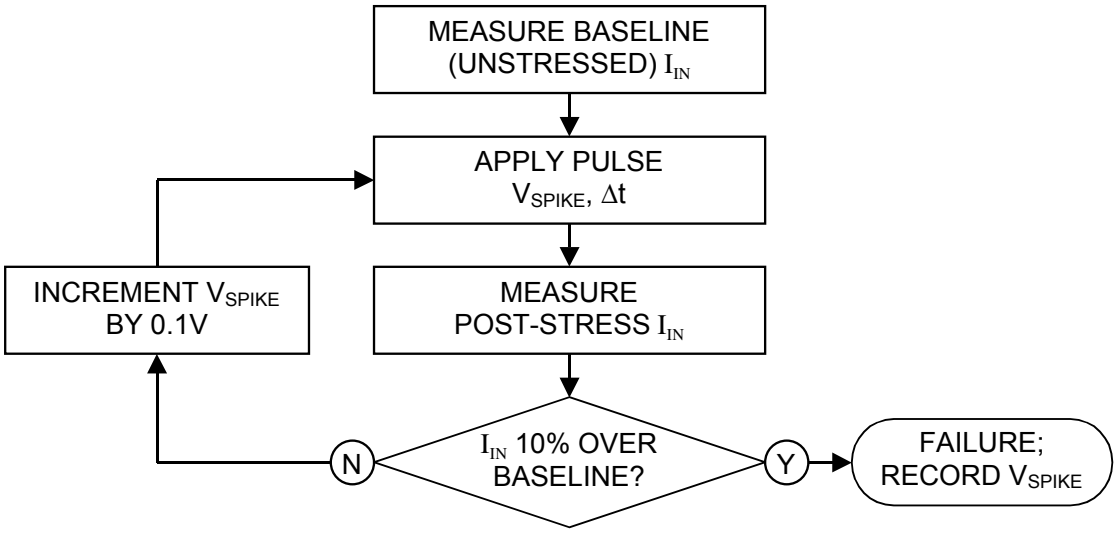


Figure 9. Test Procedure Flowchart

V. Measurement Results

The full experimental results are shown in numerical form in Table 1, and in graphical form in Figure 10.

Table 1. Experimental Results.

Stress pulse duration [µs]	Voltage at which damage occured [V]	Pre damage leakage [nA]	Post damage leakage [nA]	Change in leakage Post/Pre [%]
5.0	9.0	34.7	85.1	245%
5.0	9.5	34.7	85.1	245%
7.0	9.0	23.8	62.6	263%
8.0	8.2	29.5	73.2	248%
8.0	8.9	29.5	73.2	248%
10.0	8.0	32.1	91.5	285%
10.0	8.4	32.1	91.5	285%
12.0	8.3	25.0	83.0	332%
13.3	7.9	30.7	81.8	266%
13.3	8.3	30.7	81.8	266%
15.0	8.2	26.5	89.0	336%
16.0	8.0	34.0	95.4	281%
16.0	8.4	34.0	95.4	281%
20.0	8.0	32.2	99.8	310%
20.0	8.5	32.2	99.8	310%
30.0	7.8	28.4	102.0	359%
36.0	7.9	31.0	101.0	326%
40.0	7.9	34.0	103.8	305%
40.0	7.9	32.0	111.0	347%
40.0	8.4	34.0	103.8	305%
72.0	7.6	26.5	118.0	445%
80.0	8.2	34.7	117.6	339%
80.0	8.6	34.7	117.6	339%
134.0	7.9	30.0	130.0	433%

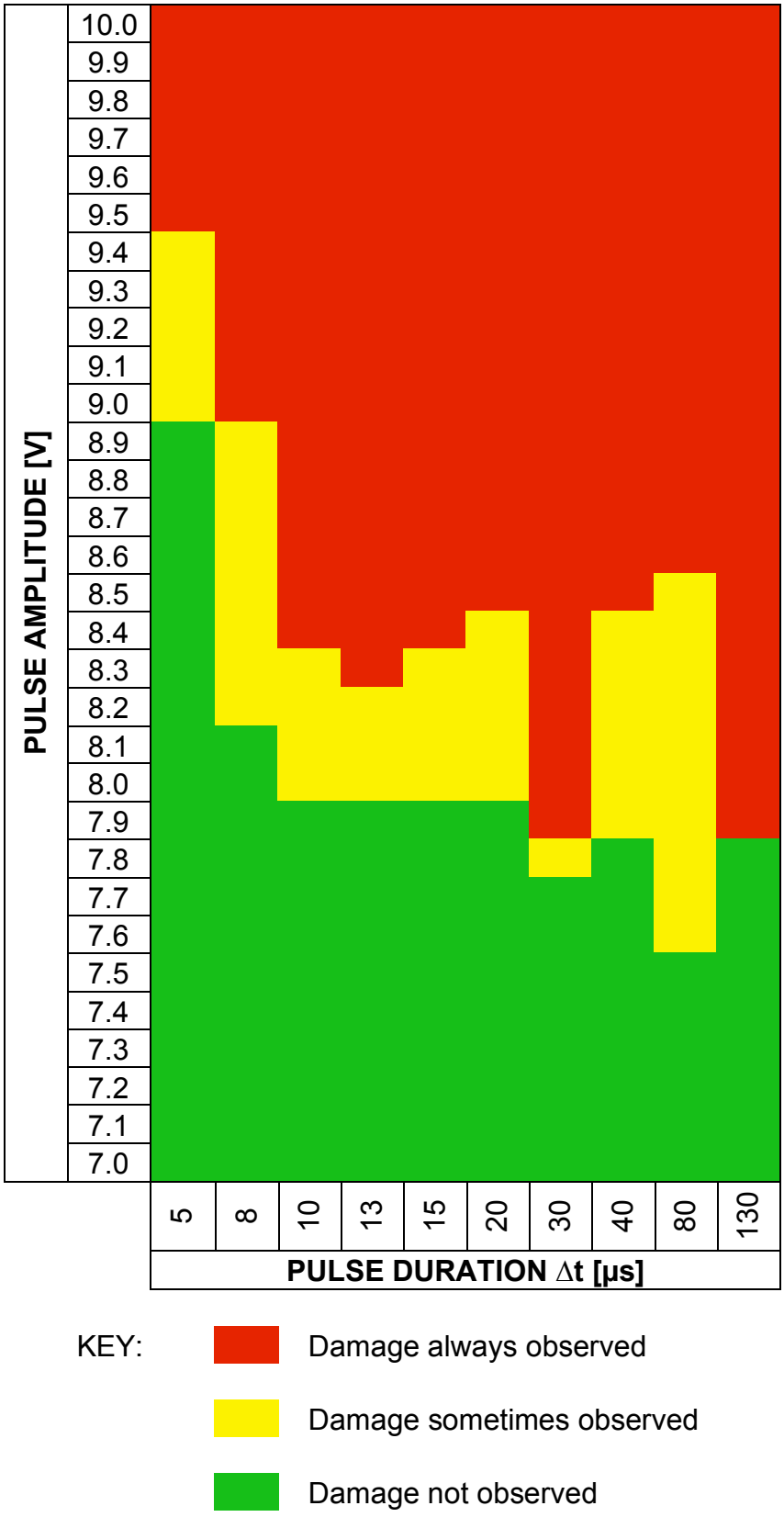


Figure 10. Graphical summary of damage as a function of pulse amplitude and voltage.

From the data in Table 1 and Figure 10, the following can be observed:

Rapid increase in leakage current: As can be seen from the data in Table 1, for a 0.1V increment in pulse amplitude, observed leakage current increased by much more than the 10% SILC criterion; a factor of 2X to 3X was more typical. This shows the sensitivity of damage to even small increases in the over-voltage stress and emphasizes the need for precise pin electronics in testing.

Statistical nature of damage: As can be seen from Figure 11, for most pulse durations there was a range of voltage for which damage may or may not occur. This is to be expected, given that a statistical measure (mean time to failure) is predicted by the 1/E model for this failure mechanism [10].

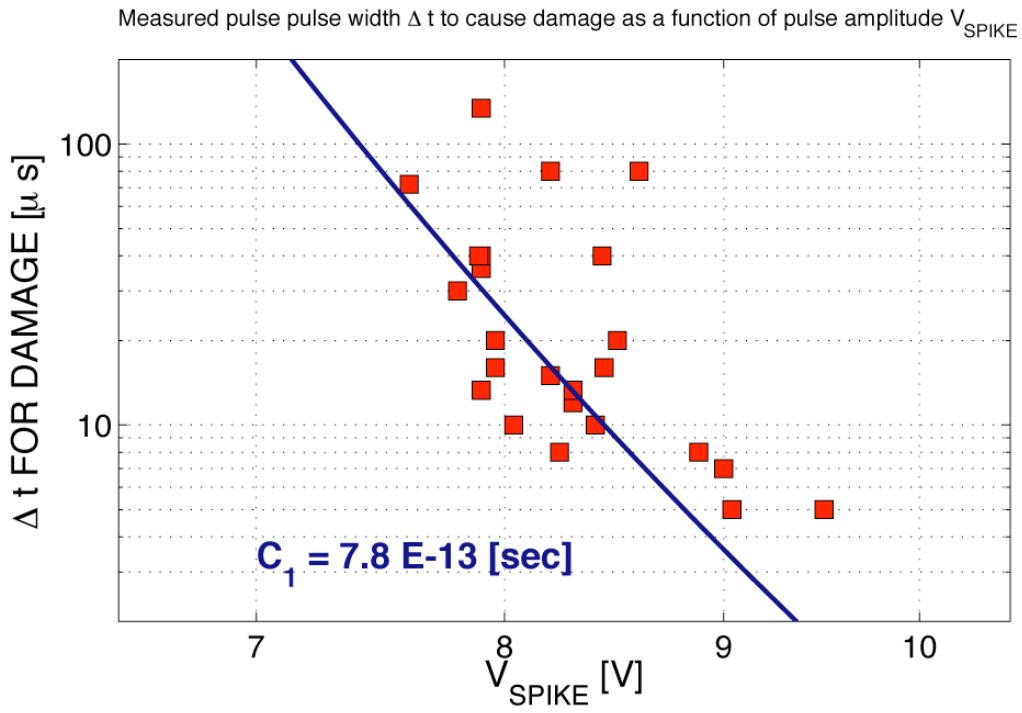


Figure 11. Failure times as a function of pulse amplitude, with 1/E model prediction.

A. Correlation of experimental data to theoretical models

The plot in Figure 11 shows the failure points where the device showed damage by exceeding the SILC threshold of 10% or more over the baseline leakage. These observed values were compared against the prediction of the 1/E model for an oxide thickness of 3.25nm for TDDB. The value of the technology dependent parameter C1 was determined to be 7.81 X 10^{-13} sec, from a best fit to the experimental data. The plot shows good agreement between the data and the model, demonstrating the validity of the model.

B. Implications for testing of thin oxide devices

The tolerance of the device to over-voltage stress becomes worse as the oxide thickness decreases. Equation 1 can be used with the C1 value from Figure 11 to predict stress behavior beyond the Δt limits of the data presented in Table 1, or for different oxide thicknesses. The analysis suggests that devices with oxide thicknesses less than 3.25nm would not tolerate an over-voltage spike as in figure 7. For example, if the backdrive condition of Figure 6 produces a 5V spike while testing a 1.2nm gate oxide device, what is the mean time to oxide breakdown? Using Equation 1,

$$t_{BD} = C_1 \exp(C_2 / E_{ox}) \quad \Rightarrow \quad \Delta t = (7.81E - 13\text{sec}) \exp\left(\frac{\left[4.3E + 8 \frac{V}{cm} \right] \left[\frac{1cm}{1E + 7nm} \right]}{\left[\frac{5V}{1.2nm} \right]} \right)$$

$$\Rightarrow \quad \Delta t = 24ns$$

This shows that a pulse duration of only 24ns can produce damage. As mentioned earlier in Section III.C, this transient time and amplitude profile is comparable to what can be expected during electrical test and could potentially damage the device.

CONCLUSION

Low-voltage digital logic devices are becoming more sensitive to damage suffered during electrical test due to shrinking feature size. Providing adequate ESD protection is also becoming more difficult without compromising the speed and performance aspects of the device [3]. Caution must be observed when testing thin oxide technologies to ensure that electrical testing will not cause potentially damaging electrical stress conditions. When developing test programs, test engineers should be aware that stress due to transient over-voltage conditions is possible in electrical test systems. The resulting damage can be particularly troublesome and costly because detection of such damage is extremely difficult during normal electrical test. Experimental results show that the anode hole injection or '1/E' model is a good tool to predict the safe stress limits tolerated as a function of over-voltage pulse amplitude and duration.

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