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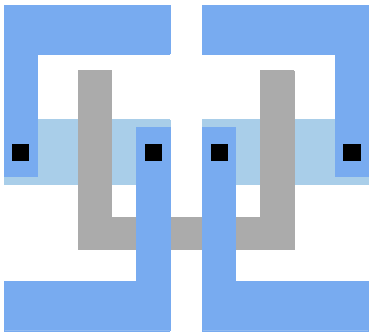
Short Summary: Current DCDB Performance



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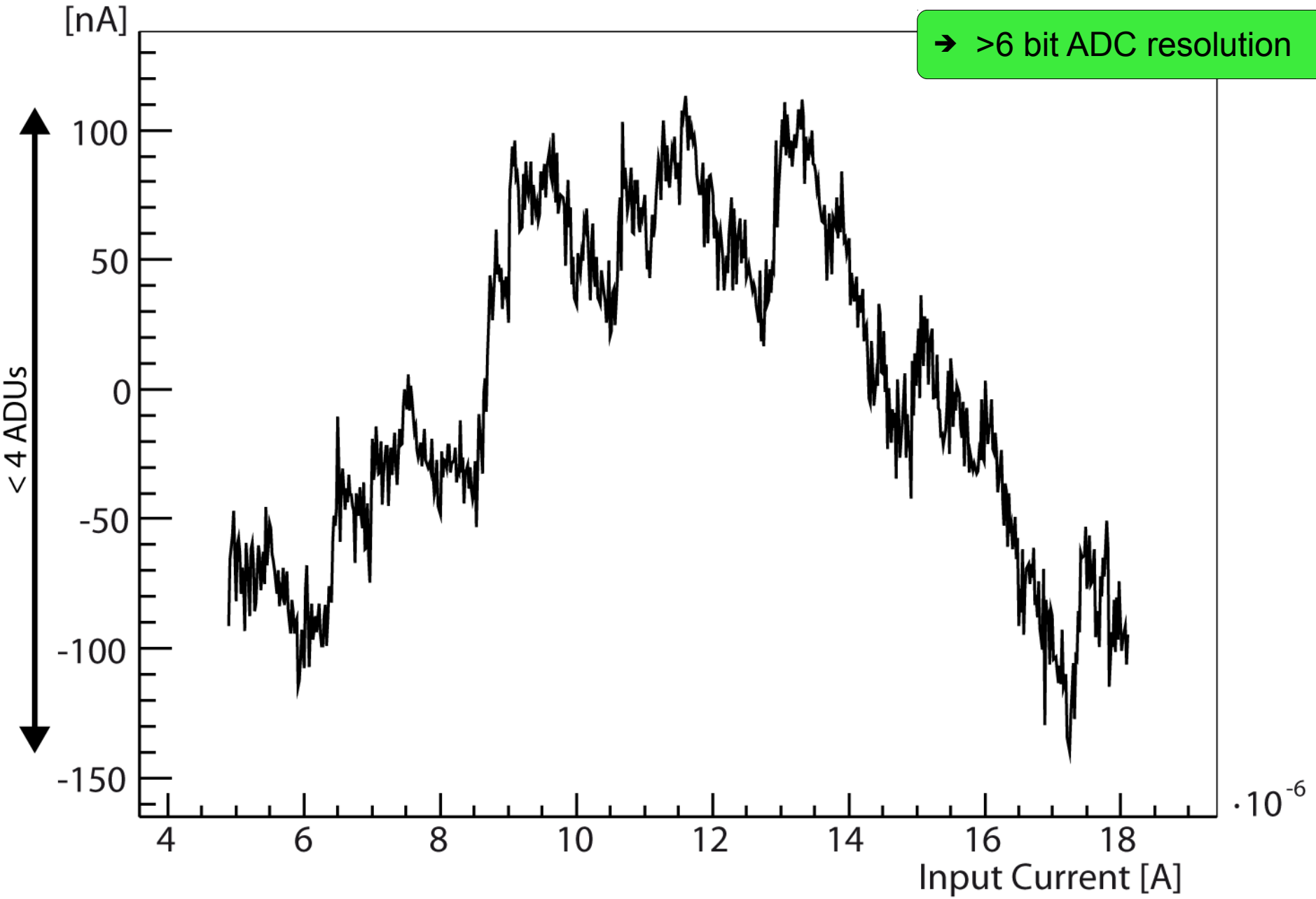
DEPFET Collaboration

EVO-Meeting

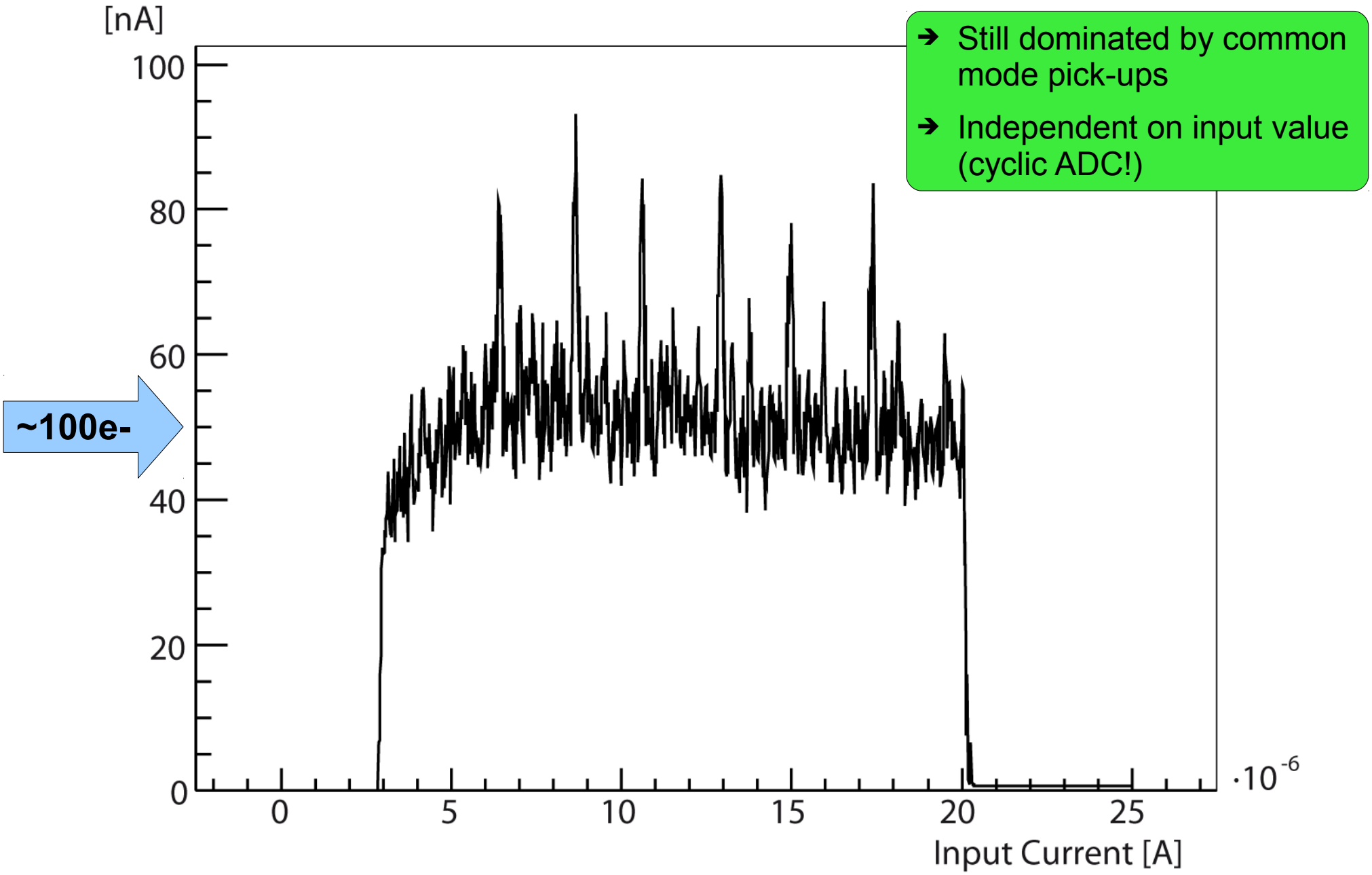
13.10.2010

ADC's Integral Non-Linearity



➔ >6 bit ADC resolution

ADC's Noise (RMS)

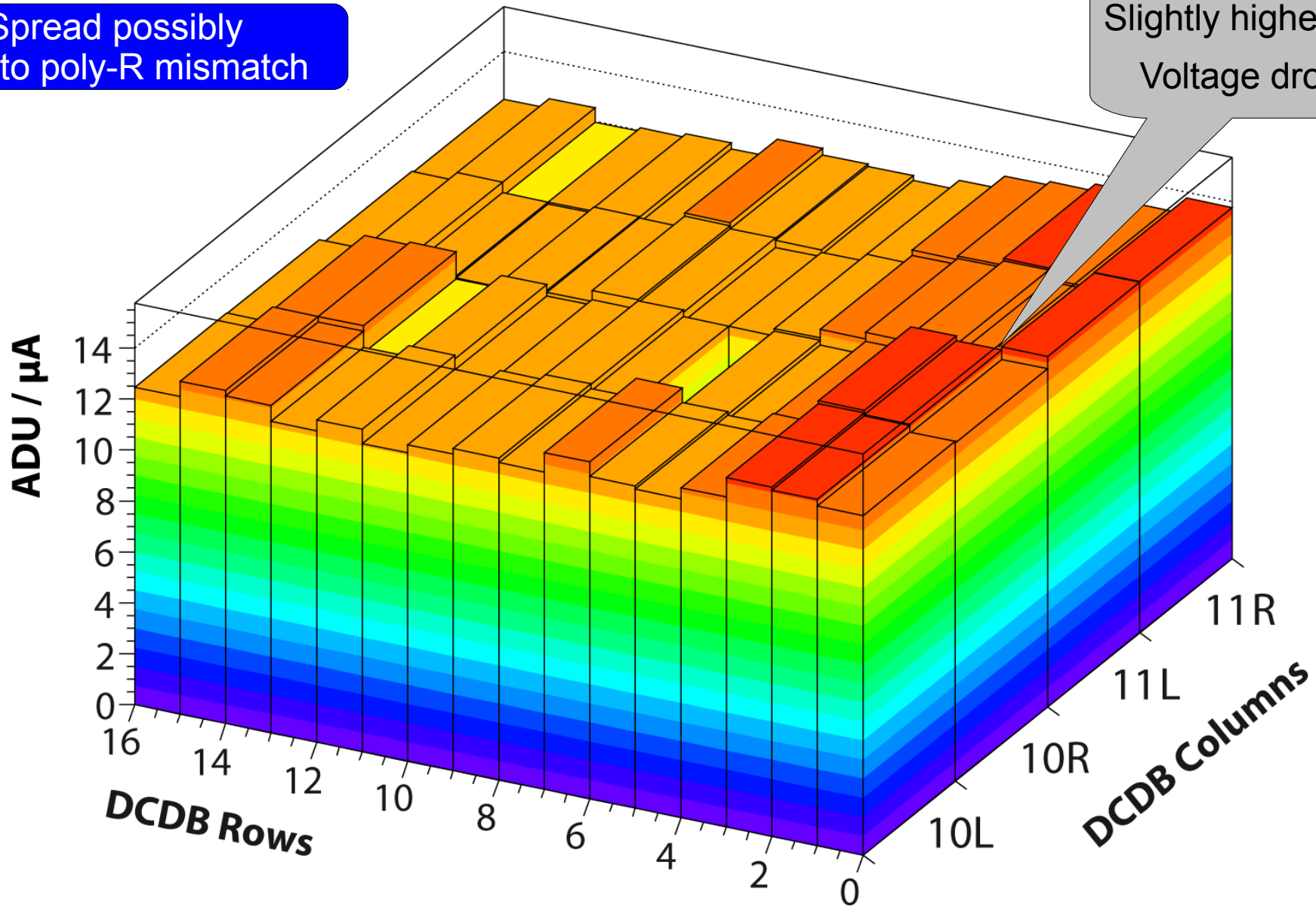


- ➔ Still dominated by common mode pick-ups
- ➔ Independent on input value (cyclic ADC!)

Gain Map

Spread possibly due to poly-R mismatch

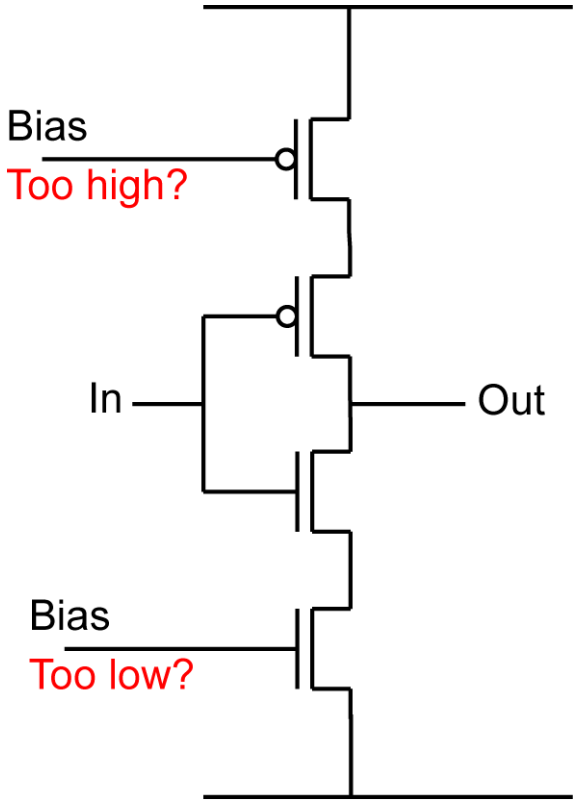
Slightly higher gain. Voltage drop??



DCDB Speed Tests

Measurements show:

- DCDB is operating well with 320ns sampling period (= DEPFET row period)
- 160ns sampling period: Still working ~2-3x noise
- <128ns sampling period: No satisfying operation



Reason:
Bug in an analog delay element for the steering signals of the current memory cells

→ Needs to be fixed in the next chip revision!

DCDB Test Summary

- ✔ DCDB production is finished. The 7th metal layer / bump bond process seems to work
- ✔ Test environment is set up: DCD-RO, bumping, PCB, FPGA firmware, software
- ✔ Power consumption within the expected range
- ✔ JTAG configuration interface is operating
- ✔ JTAG Boundary Scan is operating
- ✔ Synchronous reset network is working properly
- ✔ Digital data conversion and serialization is working
- ✔ ADC's point of operation is found
- ✔ Dynamic offset compensation mechanism is operating

- ✗ Double correlated sampling mode needs externally generated strobe signal
- ✗ There is a gain variation that needs to be understood
- ✗ The minimum sampling period is limited to 320(160)ns due to a bug in a delay element